PROJEK DEVICES

PSR05

STEERING DIODE/TVS ARRAY COMBO

APPLICATIONS

- ✔ Ethernet 10/100 Base T
- ✓ FireWire

05116

- ✓ Wireless Communications
- ✓ USB Interface

IEC COMPATIBILITY (EN61000-4)

✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
✓ 61000-4-4 (EFT): 40A - 5/50ns
✓ 61000-4-5 (Surge): 24A, 8/20µs - Level 2(Line-Gnd) & Level 3(Line-Line)

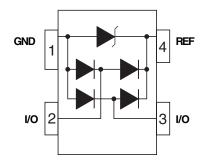
FEATURES

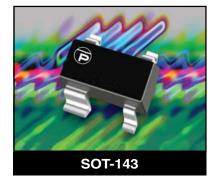
- ✓ 500 Watts Peak Power per Line (tp = 8/20µs)
- ✓ ESD Protection > 25 kilovolts
- ✓ Low Clamping Voltage
- ✔ Unidirectional Configuration
- ✔ Protects 2 I/O Ports & Power Supply
- ✔ Low Capacitance: 10pF
- ✓ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

- ✔ Molded JEDEC SOT-143
- ✔ Weight 9 milligrams (Approximate)
- ✓ Available in Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Pure-Tin Sn, 100: 260-270°C
- \checkmark Consult Factory for Leaded Device Availability
- ✓ Flammability Rating UL 94V-0
- ✔ 8mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code

PIN CONFIGURATION





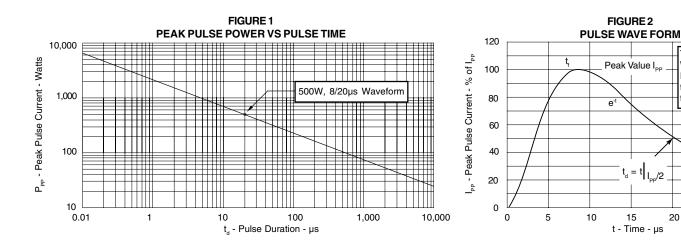
PSR05

DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified									
PARAMETER	SYMBOL	VALUE	UNITS						
Peak Pulse Power (tp = 8/20µs) - See Figure 1	P _{PP}	500	Watts						
Operating Temperature	TL	-55 to 150	C						
Storage Temperature	T _{STG}	-55 to 150	°C						
Peak Forward Voltage - I _F = 1A, 8/20µs	V _F	1.5	Volts						

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified								
PART NUMBER	DEVICE MARKING	RATED STAND-OFF VOLTAGE V _{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA V _(BR) VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ I _p = 1A V _c VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) 8/20µs V _c @ I _{pp} VOLTS	MAXIMUM LEAKAGE CURRENT @ V _{WM} b µA	MAXIMUM CAPACITANCE (See Note 1) (See Fig. 5) (Per Data Line) @OV, 1 MHz C _{J(SD)} pF	
PSR05	5A	5.0	6.0	9.8	20.0V @ 28.0A	5.0	10	

Note 1: As shown in Figure 5, REF 1 is connected to ground, REF 2 is connected to $+V_{cc}$ and input applies to $V_{cc} = 5V$, $V_{sign} = 30mV$, F = 1MHz.



TEST WAVEFORM

= 20µs

20

PARAMETERS t, = 8µs

25

30

PSR05

GRAPHS

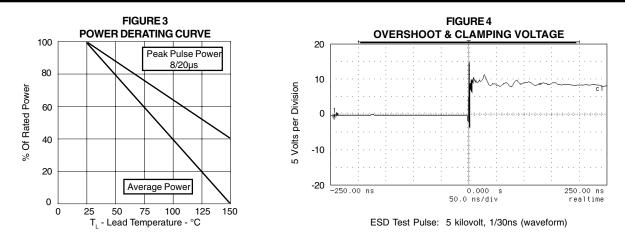
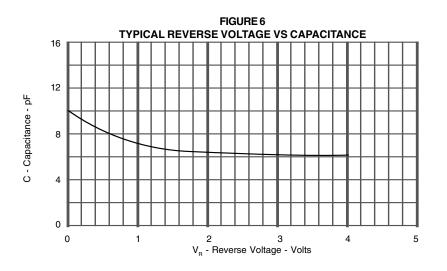


FIGURE 5 INPUT CAPACITANCE CIRCUIT REF2 VSIGN G G REF1



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APPLICATION NOTE

The PSR05 is a low capacitance, bidirectional TVS array that is designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts P_{PP} per line for an 8/20µs waveform and offers ESD protection > 25kV.

COMMON-MODE CONFIGURATION (Figure 1)

Ideal for use in USB applications, two PSR05 devices provides up to two(2) lines of protection(per device) in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Pins 2 and 3 are connected to the datalines.
- ✓ Pin 1 is connected to ground.
- ✓ Pin 4 is connected to the databus.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✔ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

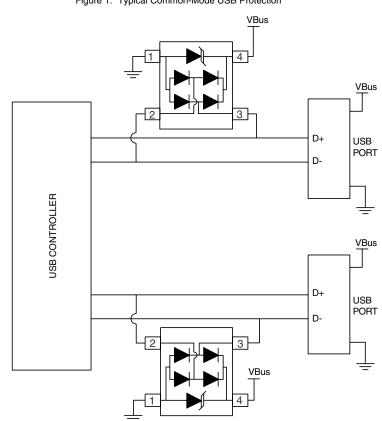
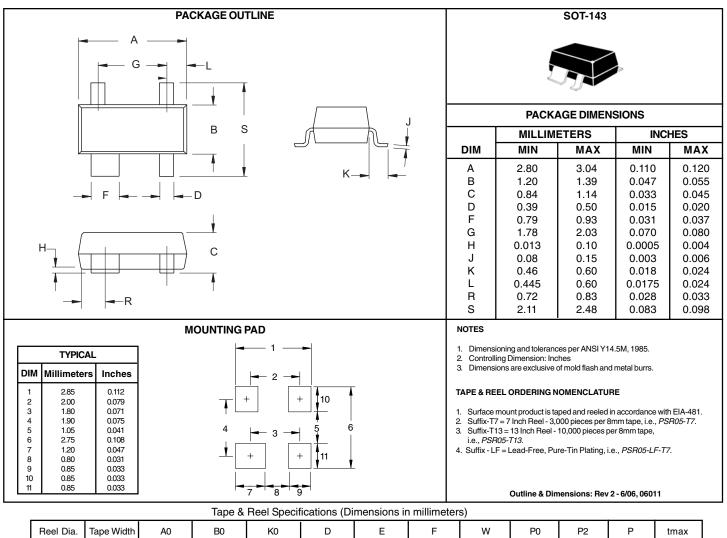


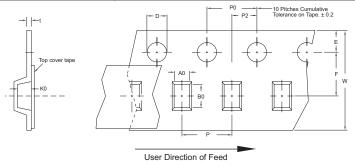
Figure 1. Typical Common-Mode USB Protection

PSR05

SOT-143 PACKAGE OUTLINE & DIMENSIONS



Reel Dia	Tape Width	AO	B0	K0	D	E	F	W	P0	P2	Р	tmax
178mm (7	') 8mm	3.10 ± 0.10	2.70 ± 0.10	1.35 ± 0.10	1.50 ± 0.10	1.75 ± 0.10	3.50 ± 0.05	8.00 ±0.30	4.00 ±0.10	2.00 ±0.05	4.00 ±0.10	0.25



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