普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

DESCRIPTION

PT2579 is a Radio Data System Demodulator IC utilizing CMOS Technology specially designed for radio data system applications. The RDS data signal (RDDA) and the RDS clock signal (RDCL) are provided as outputs for further processing by an ideal decoder / microcontroller. Anti-aliasing Filter (2nd order), 57KHz band pass filter (8th order), reconstruction filter (2nd order), clocked comparator with automatic offset compensation, biphase symbol decoder, differential decoder, and signal quality detector are all built into a single chip having the highest performance and reliability. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

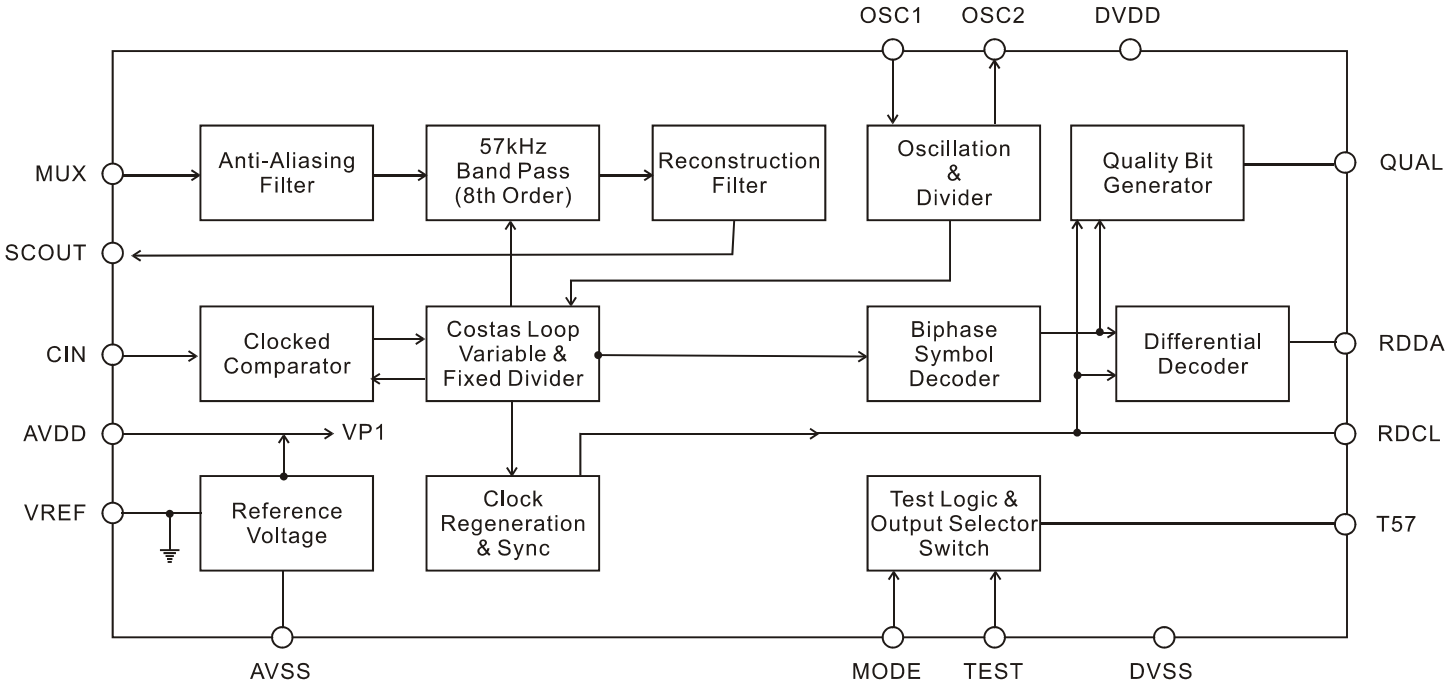
- CMOS technology
- Low power consumption
- Anti-Aliasing filter (2nd Order)
- Reconstruction filter (2nd Order)
- 57KHz Band-Pass filet (8th Order)
- 57KHz carrier regeneration
- Differential decoder
- Signal quality detector
- Subcarrier output
- Selectable 4.332 / 8.664MHz Crystal Oscillator with variable dividers
- Synchronous demodulator for 57KHz Modulated RDS signals
- Clocked comparator with automatic offset compensation
- Clock generation with Lock on Biphase data rate
- Biphase symbol decoder with integrate and dump functions
- Available in 16 pins, DIP or SOP

APPLICATIONS

- Car radio
- Home stereo tuner

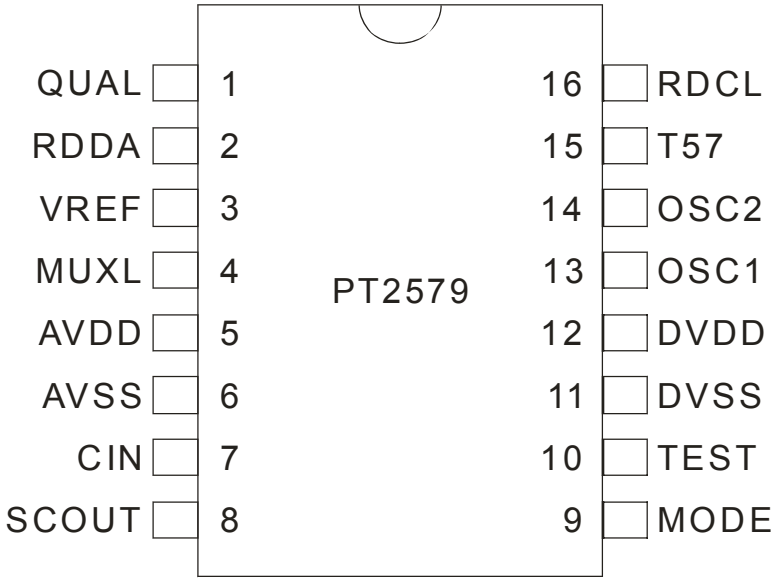
Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

BLOCK DIAGRAM



Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
QUAL	O	Quality indicator output pin	1
RDDA	O	RDS data output pin	2
VREF	-	Reference voltage	3
MUX	I	Multiplex signal input pin	4
AVDD	-	Analog supply voltage (+5V)	5
AVSS	-	Analog ground pin (0V)	6
CIN	I	Subcarrier input pin to the comparator	7
SCOUT	O	Reconstruction filter subcarrier output pin	8
MODE	I	Oscillator mode / test control input pin	9
TEST	I	Test pin	10
DVSS	-	Digital ground pin (0V)	11
DVDD	-	Digital supply voltage (+5V)	12
OSC1	I	Oscillator input pin	13
OSC2	O	Oscillator output pin	14
T57	O	57KHz clock signal output pin	15
RDCL	O	RDS clock output pin	16

FUNCTION DESCRIPTION

PT2579 is a demodulator chip specially designed for radio data system applications. It provides 57KHz bandpass filter and a digital demodulator to regenerate the RDS data stream out of the multiplex signal (MPX). PT2579 consists of the Filter and Digital Sections.

FILTER SECTION

The MUX Signal is band limited by a second order anti-aliasing filter and fed through a 57KHz 8th order bandpass filter with a 3KHz bandwidth. This separates the RDS signals. This filter uses switch capacitor technique and uses a clock frequency of 541.5KHz which is derived from the 4.332/8.664 MHz crystal oscillator. The signal is then fed into the reconstruction filter to smooth the sampled and filtered RDS signal before it is outputted on the SCOUT pin. The signal is AC-coupled to the comparator pin (CIN). The comparator uses a frequency of 228KHz (synchronized by the 57KHz of the demodulator).

DIGITAL SECTION

The Costas Loop Circuit together with the carrier regeneration demodulates the internal coupled digitized signal. The suppressed carrier is recovered from the 2 sidebands (Costas Loop). The demodulated signal is low-pass filtered in such a way that the over all pulse shape (transmitter and receiver) approaches a cosinusoidal form in conjunction with the following integrate and dump circuit.

The data spectrum shaping is divided into two equal parts and handled in the transmitter and in the receiver. Ideally, the data filtering should be equal in both of these parts. The overall data channel spectrum shaping of the transmitter and the receiver is approximately 100% roll off.

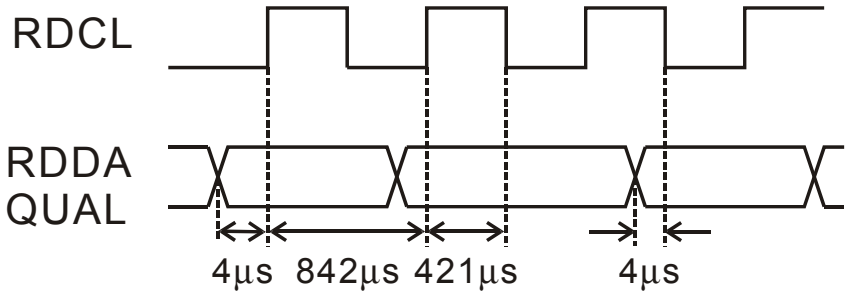
Theintegrate and dump circuit performs anintegration over a clock period. This results in a demodulation and valid RDS signal in form of biphase symbols being outputted from the integrate and dump circuit. The final stages of the RDS data processing are the biphase symbol decoding and the differential decoding. After synchronization by the data clock RDCL, data appears on the RDDA output. The output of the biphase symbol decoder is evaluated by a special circuit to provide an indication of good data (QUAL=HIGH) or corrupt data (QUAL=LOW).

TIMING

The fixed and variable dividers are applied to the 4.332/8.664MHz crystal oscillator to generate the 1.1875KHz RDS Clock – RDCL. The RDCL is synchronized with the incoming data. No matter what clock edge is considered, the data will be valid for a period of 399 us after clock transition. The data change timing is 4μs before a clock change. Which clock transition (i.e. positive or negative going clock), the data change occurs in, depends on the lock conditions and is arbitrary (bit slip).

When the reception is poor, it is possible that faults in phase occur, then the clock signal stays uninterrupted and data is constant for 1.5 clock periods. Normally, faults in phase do not occur in a cyclic manner. If however, the faults in the phase occur in this way, the minimum spacing between two possible faults in phase depends on the data being transmitted. The minimum spacing cannot be less than 16 clock period. The quality bit changes only at the time of a data change.

The diagram below shows the RDS timing waveform which includes a phase jump.



Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Min.	Max.	Unit
Analog supply voltage	AV_{DD}	AV_{DD}	0	6	V
Digital supply voltage	DV_{DD}	DV_{DD}	0	6	V
Voltage on all pins except GND	Vn		-0.5	V_{DDX}+0.5	V
Operating temperature	Topr		-40	+85	℃
Storage temperature	Tstg		-65	+150	℃

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, AV_{DD}=DV_{DD}=5V, Ta=25℃)

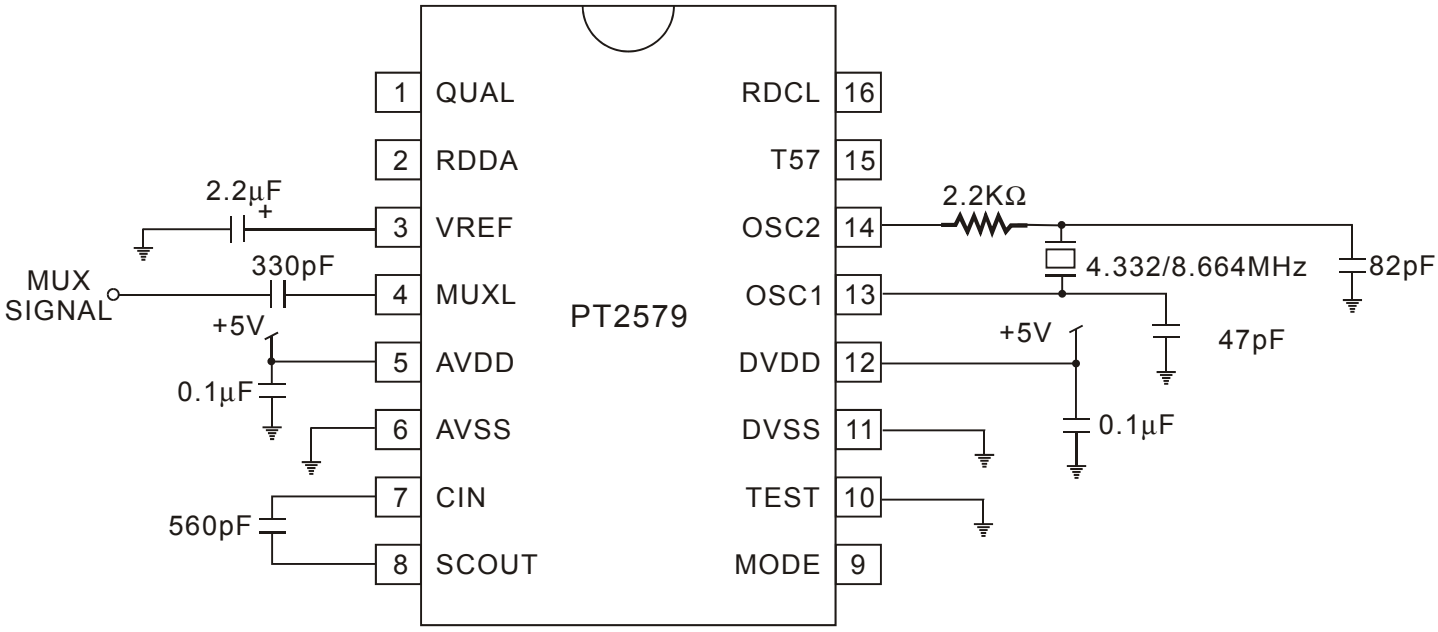
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog supply voltage	AV_{DD}	AV_{DD}	3.3	5.0	5.5	V
Digital supply voltage	DV_{DD}	DV_{DD}	3.3	5.0	5.5	V
Total supply current	Itot	I5 + I12	-	6	-	mA
Reference voltage	Vref	VREF, AV_{DD}=5V	-	2.5	-	V
MPX Input (Signal before the Capacitor on Pin 4)						
RDS amplitude (RMS value)	$V_{iMPX(rms)}$	f=+1.2KHz RDS f=+3.5KHz ARI (see Note)	1	-	-	mV
Maximum input signal capability (peak to peak value)	$V_{iMPX(p-p)}$	f=57±2KHz	200	-	-	mV
		f<50KHz	1.4	-	-	V
		f<15KHz	2.8	-	-	V
		f>70KHz	3.5	-	-	V
Input impedance	R4-6	f=0 to 100KHz	40	-	-	KΩ
Signal gain	G8-4	f=57KHz	17	20	23	dB
57KHz Band-Pass Filter						
Center frequency	fc	Ta=-40 to +85℃	56.5	57.0	57.5	KHz
-3dB bandwidth	B	-	2.5	3.0	3.5	KHz
Stop band gain	G	f=±7KHz	31	-	-	dB
		f<45KHz	40	-	-	dB
		f<20KHz	50	-	-	dB
		f>70KHz	40	-	-	dB
Output resistance (pin 8)	$R_{o\ (8)}$	f=57KHz	-	26	-	Ω
Comparator Input (Pin 7)						
Minimum input level (RMS value)	$V_{i(rms)}$	f=57KHz	-	1	10	mV
Input resistance	R_i	-	70	110	150	KΩ
Oscillator Input (Pin 13)						
High level input voltage	V_{IH}	DV_{DD}=5.0V	4.0	-	-	V
Low level input Voltage	V_{IL}	DV_{DD}=5.0V	-	-	1.0	V
Input current	I_I	DV_{DD}=5.5V	-	-	±1	μA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital Demodulator and Outputs – QUAL, RDDA, T57, OSC2, RDCL						
High level output voltage	V_{OH}	I_Q=-20μA, DV_{DD}=4.5V	4.4	-	-	V
Low level output voltage	V_{OL}	I_Q=3.2mA, DV_{DD}=5.5V	-	-	0.4	V
Nominal clock frequency	f_{RDCL}	RDCL	-	1187.5	-	Hz
RDCL jitter	t_{RDCL}	-	-	-	18	μs
Nominal subcarrier frequency	fT57	T57 (see Note 1)	-	57.0	-	KHz
Output current	I_O	OSC2 DV_{DD}=4.5V, V_{14}=0.4V	1.5	-	-	mA
		OSC2 DV_{DD}=4.5V, V_{14}=4.1V	-1.6	-	-	mA
		QUAL, RDDA, T57, RDCL DV_{DD}=4.5V, V_{14}=0.4V	5.9	-	-	mA
		QUAL, RDDA, T57, RDCL DV_{DD}=4.5V, V_{14}=4.1V	-5.3	-	-	mA
4.332 MHz Crystal Parameter						
Crystal frequency	f0	-	-	4.332	-	MHz
Maximum permitted tolerance	fmax		-	±50	-	10^{-6}
f0 adjustment tolerance	f0	Ta=25℃	-	-	±20	10^{-6}
		Ta=-40 to +85℃	-	-	±25	10^{-6}
Load capacitance	CL		-	30	-	pF
Resonance resistance	Rxtal		-	-	60	Ω
8.664 MHz Crystal						
Crystal frequency	f0	-	-	8.664	-	MHz
Maximum permitted tolerance	fmax		-	±50	-	10^{-6}
f0 adjustment tolerance	f0	Ta=25℃	-	-	±30	10^{-6}
		Ta=-40 to +85 ℃	-	-	±30	10^{-6}
Load capacitance	CL		-	30	-	pF
Resonance resistance	Rxtal		-	-	60	Ω

Note:
The signal T57 has a phase lead of 123° (±180°) relative to ARI carrier at output SCOUT.

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

APPLICATION CIRCUIT



Note:
Two crystal frequencies may be used via the MODE pin. Please refer to the table below.
For the 4.332MHz Crystal, it is recommended to use TXC 6A04300098 or a component with the same specifications.

MODE Pin State	Crystal Clock Frequency (MHz)
LOW	4.332
HIGH	8.664

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

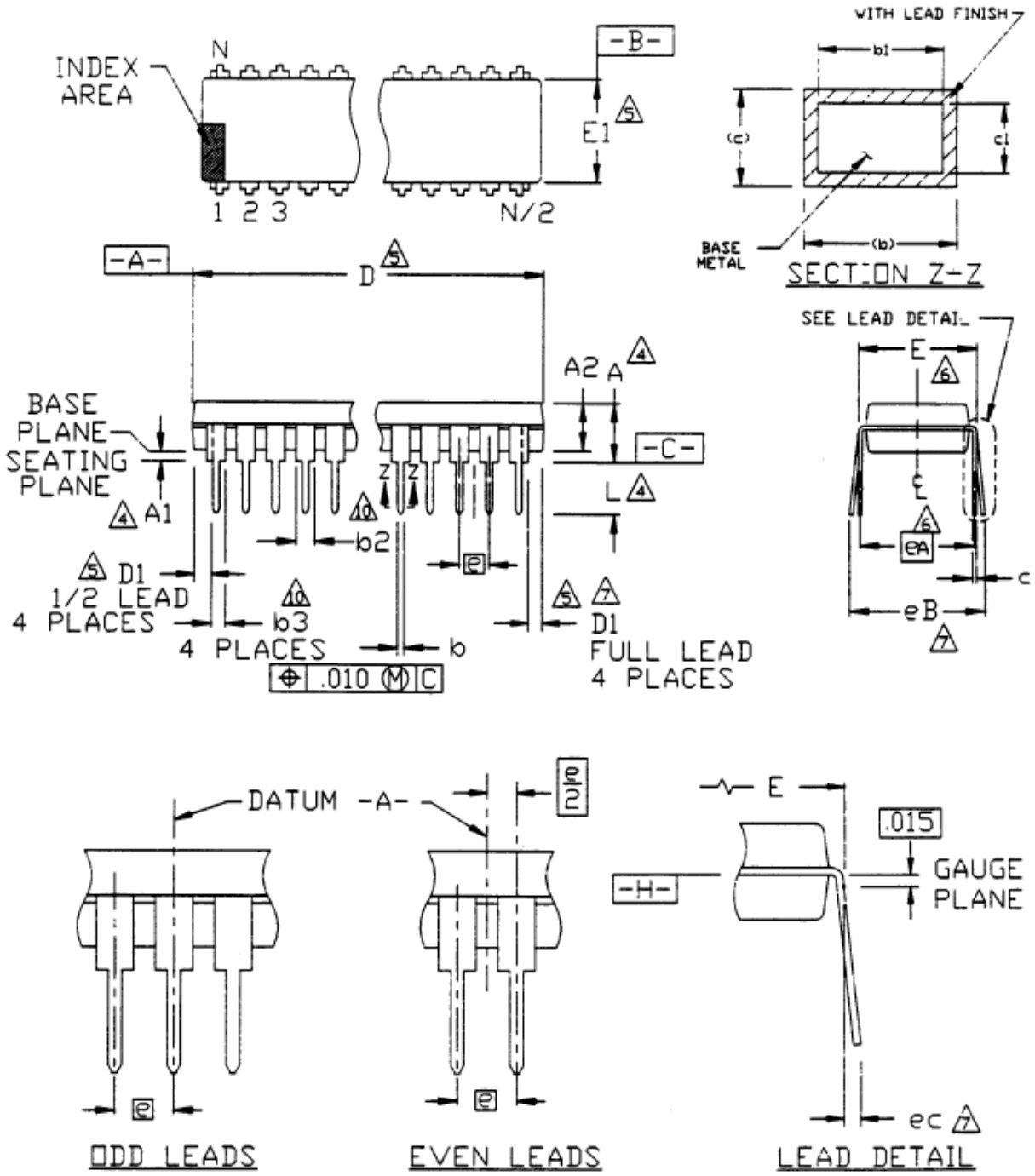
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2579	16 pins, DIP, 300mil	PT2579
PT2579-S	16 pins, SOP, 300mil	PT2579-S
PT2579-SN	16 pins, SOP, 150mil	PT2579-SN
PT2579-X	16 pins, SSOP, 150mil	PT2579-X

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

PACKAGE INFORMATION

16 PINS, DIP, 300MIL



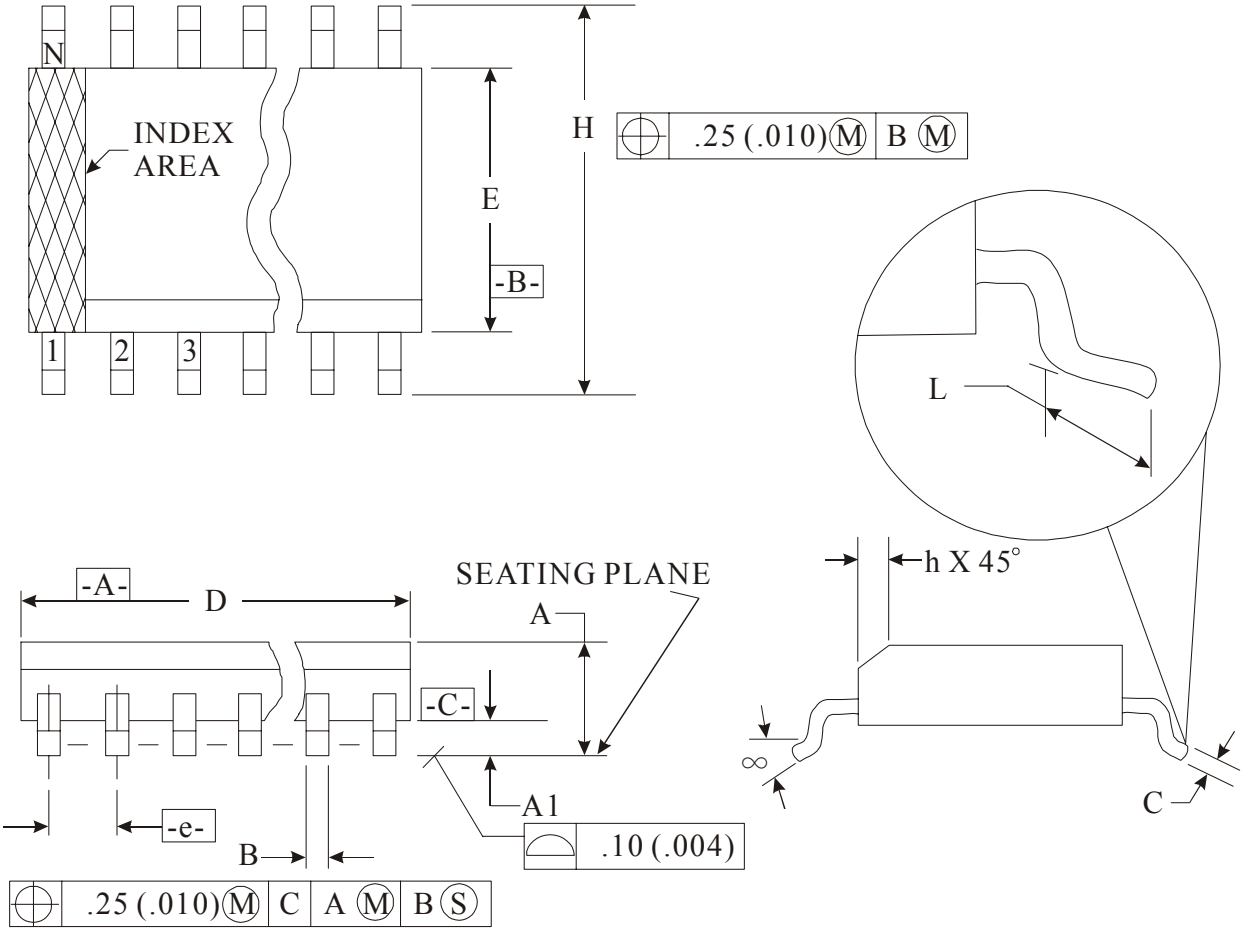
Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 bsc	
eA		0.300 bsc	
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c-. “eB” and “eC” are measured at the lead tips with the loads unconstrained.
6. “N” is the number of terminal positions. (N=16)
7. Pointed or rounded lead tips are preferred to ease insertion.
8. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
9. Distance between leads including Dambar protrusions to be 0.005 inch minimum.
10. Datum plane -H- coincident with the bottom of lead, where lead exits body.
11. Refer to JEDEC MS-001 Variation AB.

JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

16 PINS, SOP, 300MIL



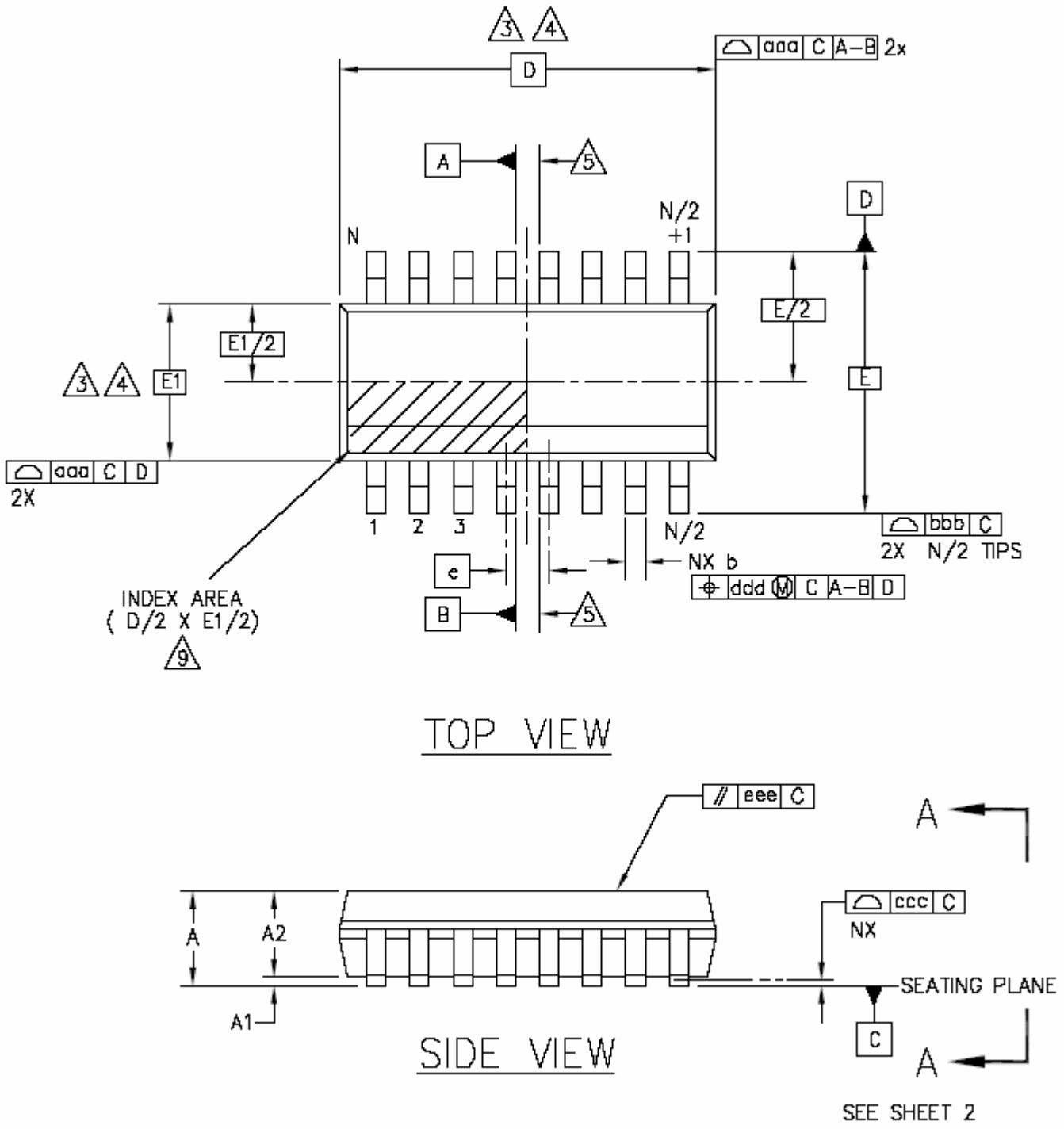
Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27 BSC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0o	8o

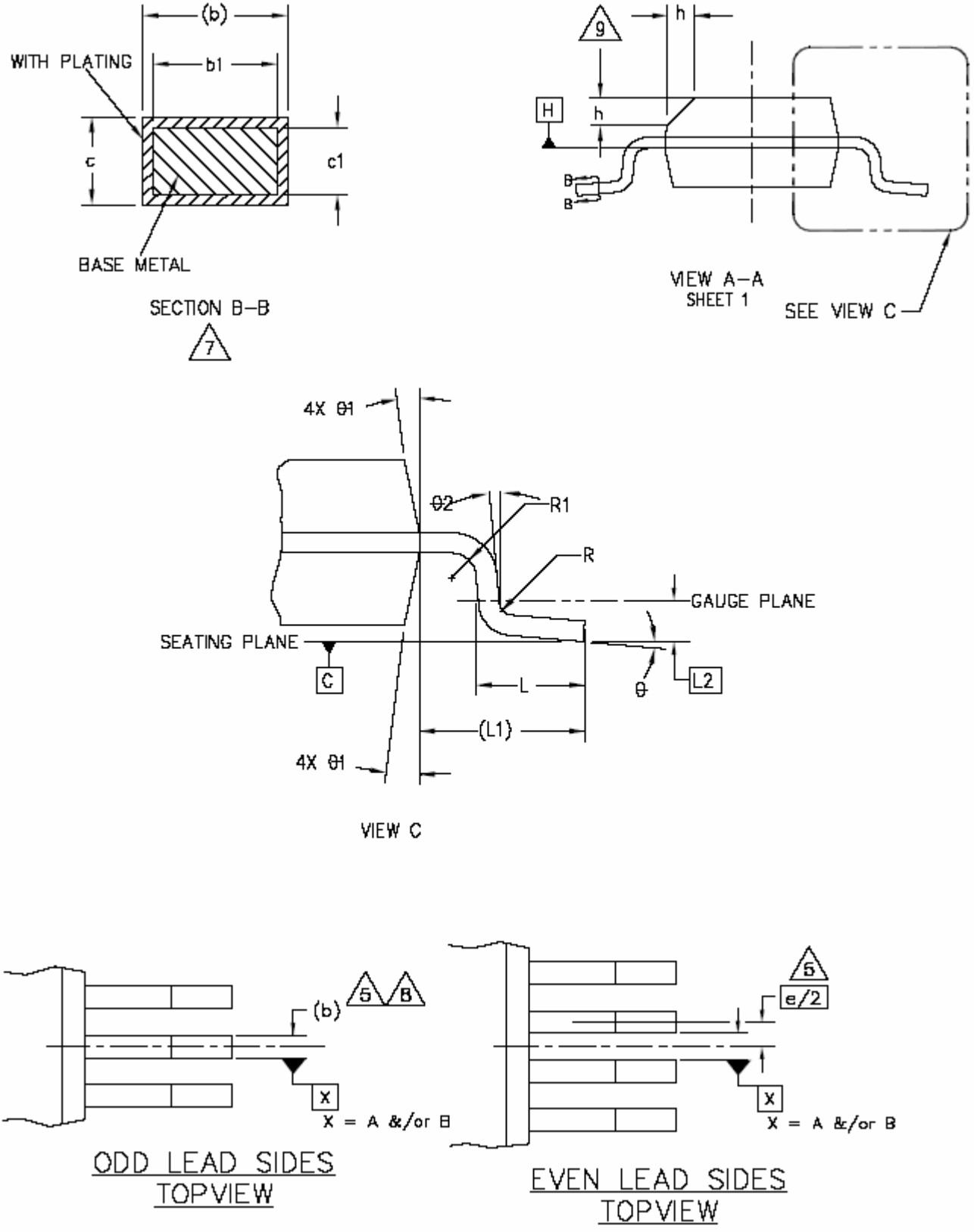
Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=16)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension : MILLIMETER.
9. Refer to JEDEC MS-013, Variation AA.

JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

16 PINS, SOP, 150MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
5
B
(b)
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

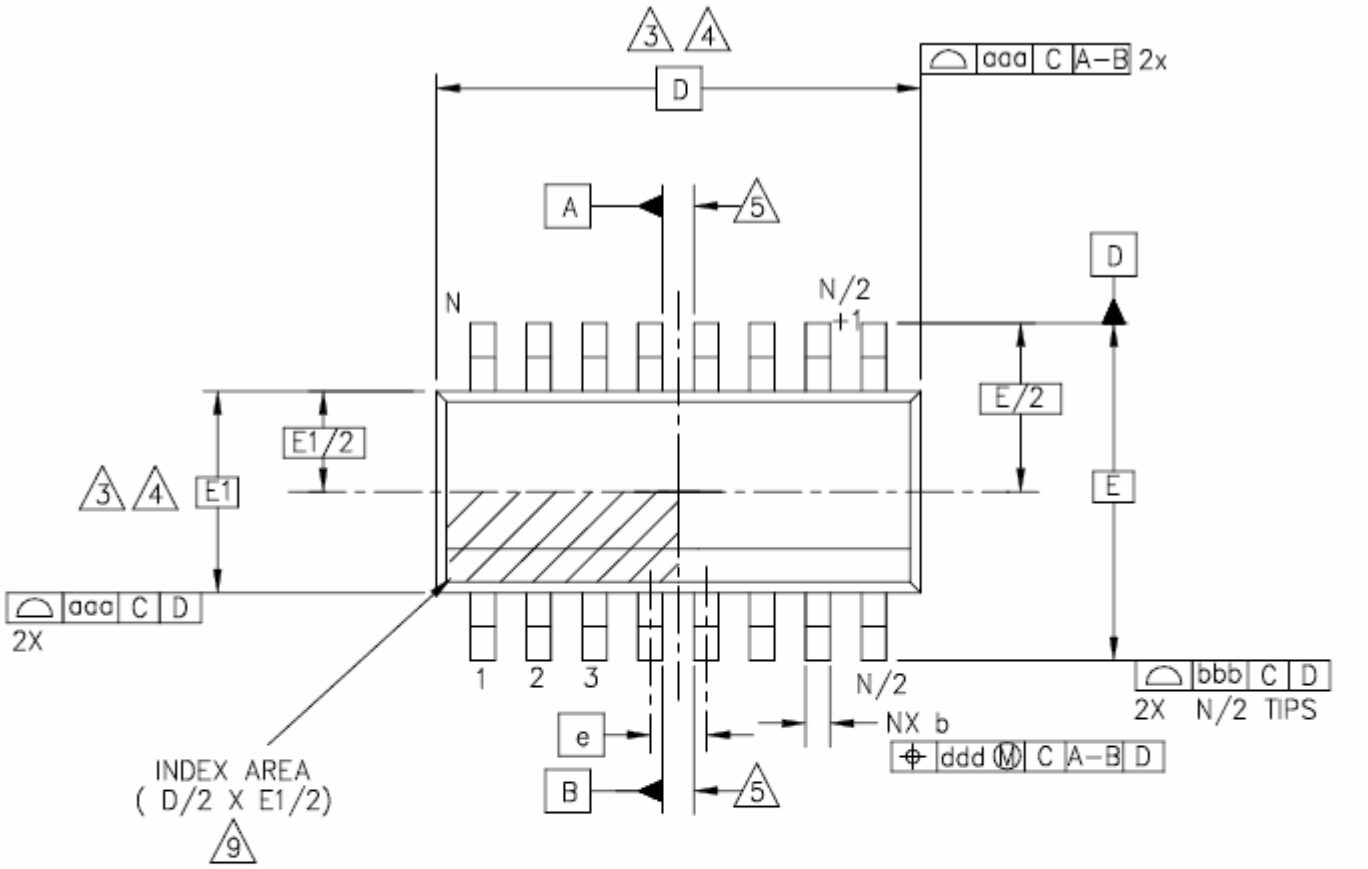
Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Note:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=16)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC.

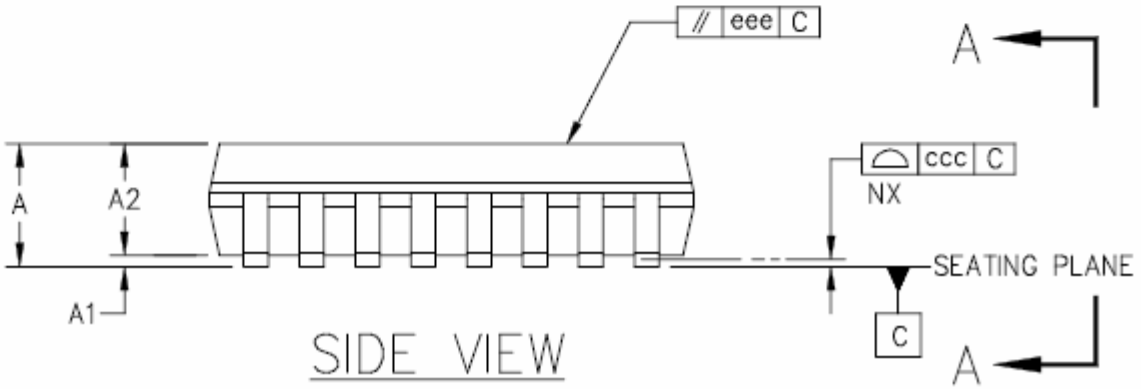
JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.

Tel: 886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

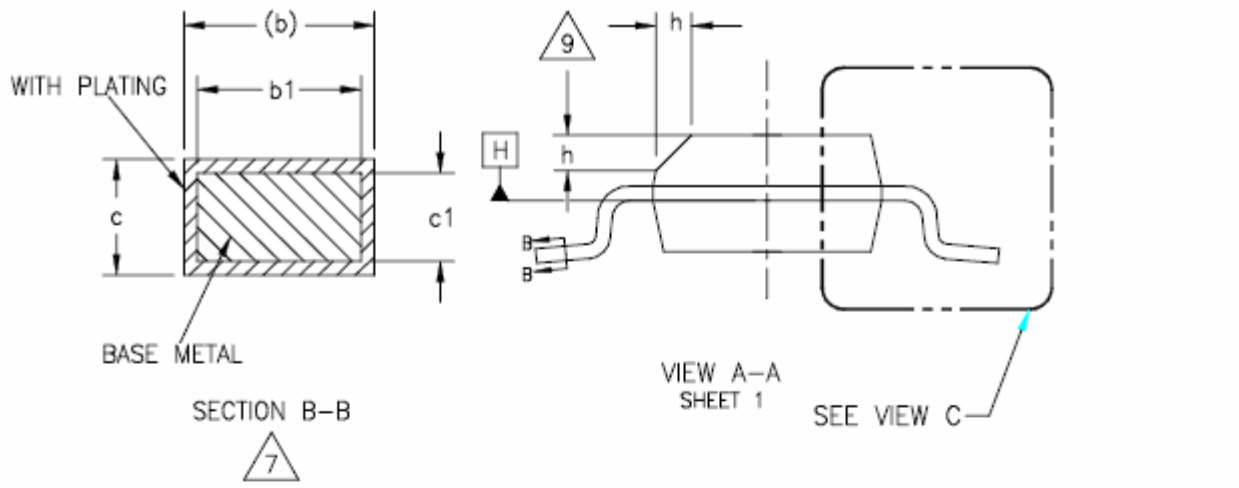
16 PINS, SSOP, 150MIL

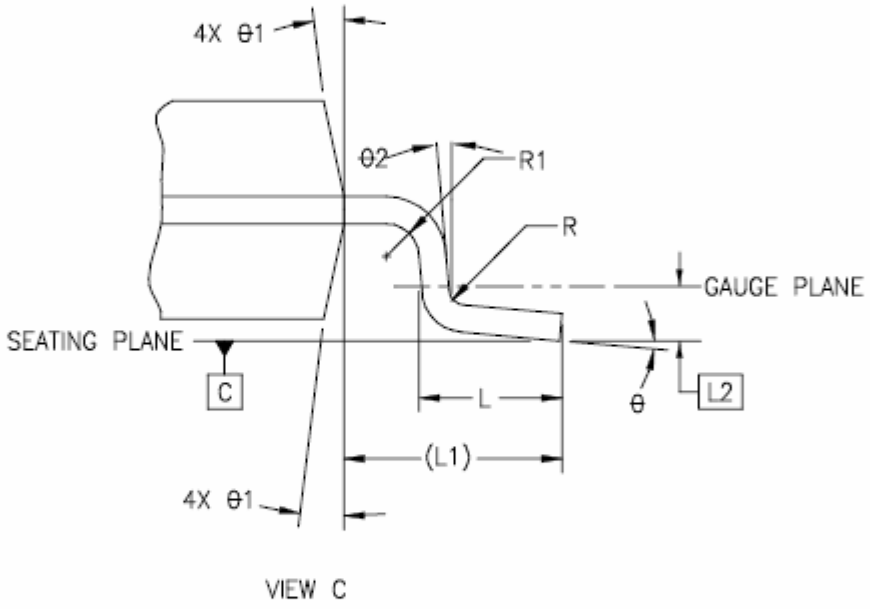


TOP VIEW

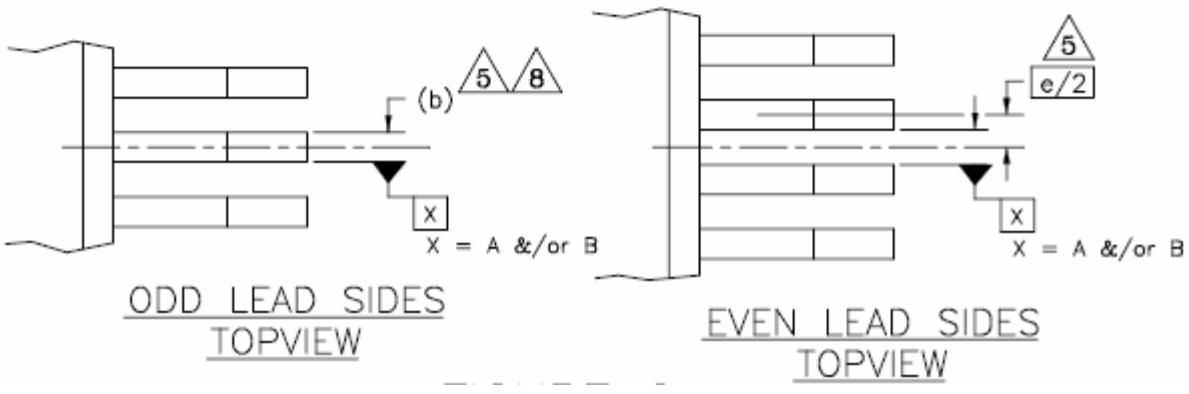


SIDE VIEW


(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B-B
7
9
h
H
h
B
B
VIEW A-A
SHEET 1
SEE VIEW C


4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1

VIEW C


(b)
5
8
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Nom.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
b	0.008	-	0.012
b1	0.008	0.010	0.011
c	0.006	-	0.010
c1	0.006	0.008	0.009
D	0.193 BSC		
E	0.236 BSC		
E1	0.154 BSC		
e	0.025 BAS		
L	0.016	-	0.050
L1	0.041 REF		
L2	0.010 BAS		
R	0.003	-	-
R1	0.003	-	-
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-
aaa	0.004		
bbb	0.008		
ccc	0.004		
ddd	0.007		
eee	0.004		

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimensions in inches (angles in degrees)
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006” per end. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed “0.006” per side. D1 and E1 dimensions are determined at dutum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic.
5. Datums A and B to be determined at datum H.
6. N is the maximum number of terminal position. (N=16)
7. The dimensions apply to the flat section of the lead between 0.004 to 0.010 inches from the lead tip.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.004” total in excess of b dimension at maximum material condition. The dambar can not be located on the lower radius of the foot.
9. Refer to JEDEC MO-137 variation AB.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION