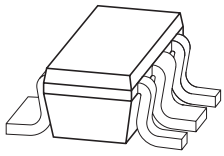
GaAs MMIC

CGY 98

Data Sheet

- Broadband power amplifier (800 … 2000 MHz)
- GSM, AMPS or PCN
- Operating voltage range: 2.7 to 5.0 V
- P_{OUT} = 35.0 dBm at V_D = 3.5 V
- Overall power added efficiency 55%
- Easy external matching

ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!



SCT 595

Type	**Marking**	**Ordering Code** (taped)	**Package**
CGY 98	G8s	Q62702-G0079	SCT-595

Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Positive supply voltage	V_D	6	V
Supply current stage 1	I_D	0.6	A
Supply current stage 2	I_D	1.8	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	– 55 … + 150	°C
Total power dissipation ($T_S \leq 70$ °C) T_S: Temperature at soldering point	P_{tot}	2.0	W
Pulse peak power (dissipated) t_{ON} (pulsed mode) ≤ 2 ms	P_{Pulse}	4.5	W
t_{ON} (pulsed mode) ≥ 2 ms < 10 ms	P_{Pulse}	2.5	W
t_{ON} (switching mode) ≥ 10 ms and if accumulated number of on/of switching cycles > 1×10^5	P_{Pulse}	1.6	W

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel-soldering point	R_{thChS}	40	K/W

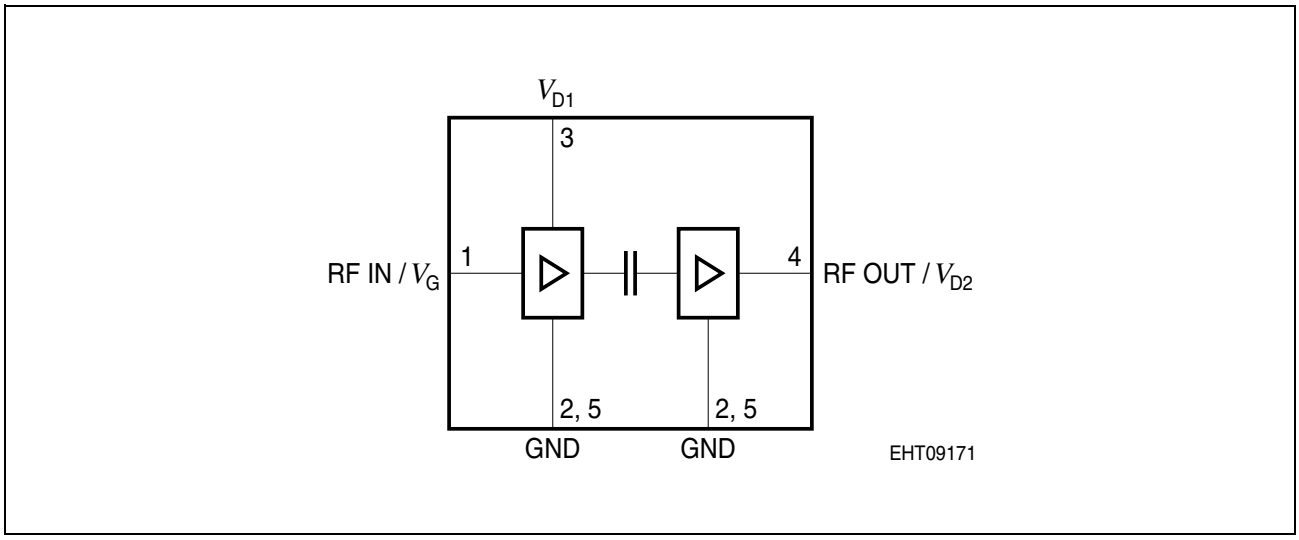


Figure 1 Functional Block Diagram

Pin Configuration

Pin No.	Name	Configuration
1	RF IN/V_G	RF input power and Gate voltage
2	GND	RF and DC ground
3	V_{D1}	Pos. drain voltage 1st stage
4	RF OUT/V_{D2}	RF output power / pos. drain voltage 2nd stage
5	GND	RF and DC ground

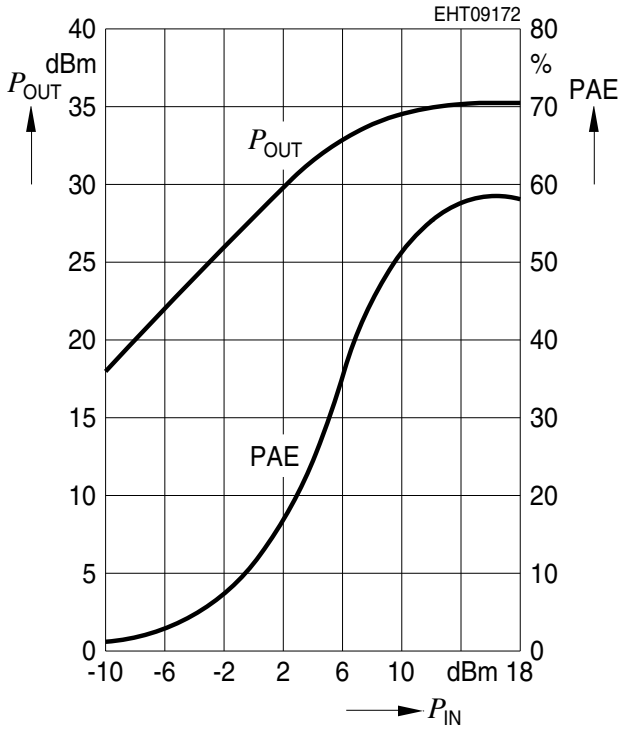
GSM-Operation

Electrical Characteristics on GSM Application Board

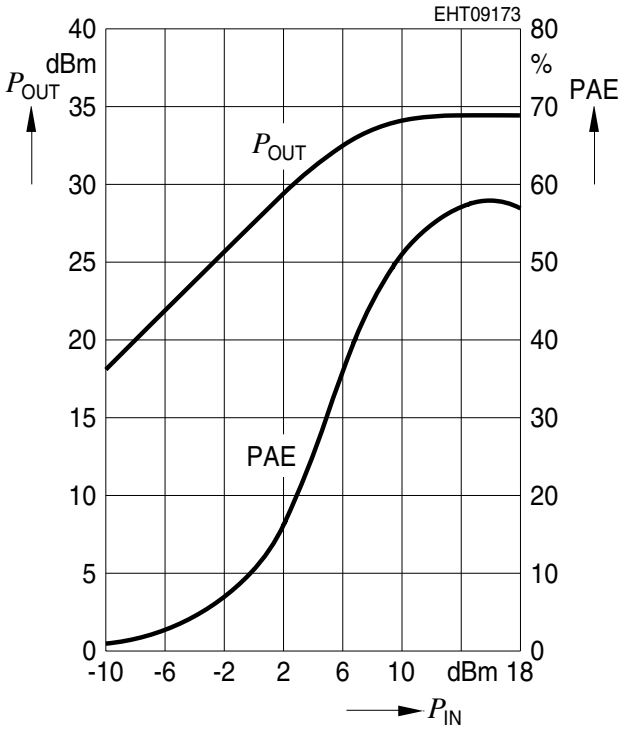
T_A = 25 °C, Z_S = Z_L = 50 Ω, duty cycle 12.5%, t_{ON} = 577 µs
unless otherwise specified

Parameters	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Frequency range	f	880	–	915	MHz	–
Supply current	I_{DD}	–	1.6	–	A	V_D = 3.5 V, P_{IN} = + 15 dBm
Power gain	G	–	20	–	dB	V_D = 3.5 V, P_{IN} = + 15 dBm
Output Power	P_O	–	33.2	–	dBm	V_D = 2.8 V, P_{IN} = + 15 dBm
Output Power	P_O	–	34.4	–	dBm	V_D = 3.2 V, P_{IN} = + 15 dBm
Output Power	P_O	–	35.0	–	dBm	V_D = 3.5 V, P_{IN} = + 15 dBm
Overall Power added Efficiency	PAE	–	55	–	%	V_D = 3.5 V, P_{IN} = + 15 dBm
Harmonics $2f_0$ $3f_0$	– –	– –	– 36 – 36	– –	dBc	–
Input VSWR	–	–	2:1	–	–	V_D = 3.5 V or V_D = 4.8 V
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 10 dBm, $V_D \leq$ 4.6 V, Z_S = 50 Ω, Load VSWR = 20:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level			–	P_{IN} = 10 dBm, V_D = 4.6 V, Z_S = 50 Ω, Load VSWR = 5:1 for all phase

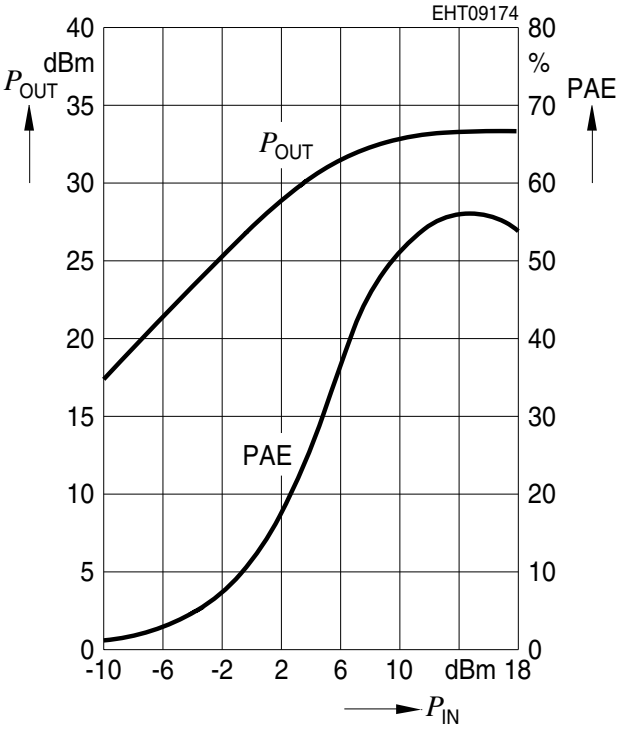
Output Power and PAE vs. Input Power
V_D = 3.5 V, V_G = – 1.5 V, f = 900 MHz



Output Power and PAE vs. Input Power
V_D = 3.2 V, V_G = – 1.5 V, f = 900 MHz

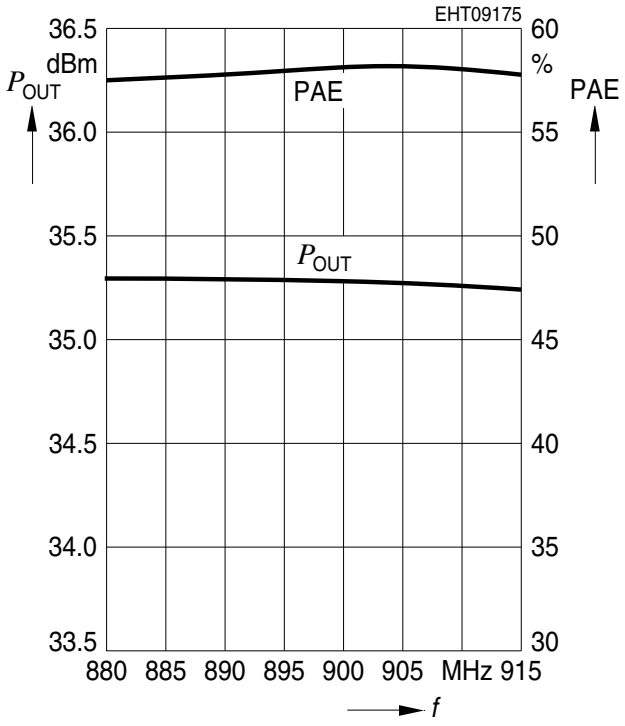


Output Power and PAE vs. Input Power
V_D = 2.8 V, V_G = – 1.5 V, f = 900 MHz



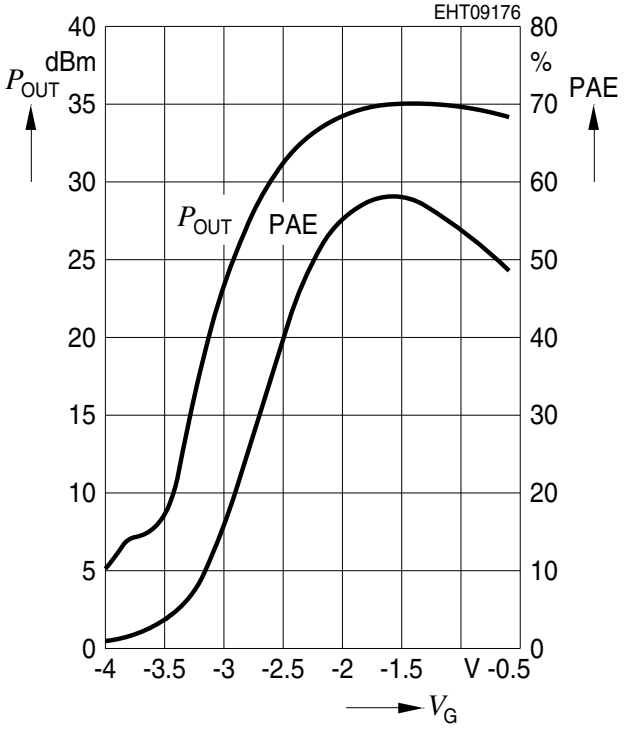
Output Power and PAE vs. Frequency

V_G = – 1.5 V, P_{IN} = 15 dBm, V_D = 3.5 V



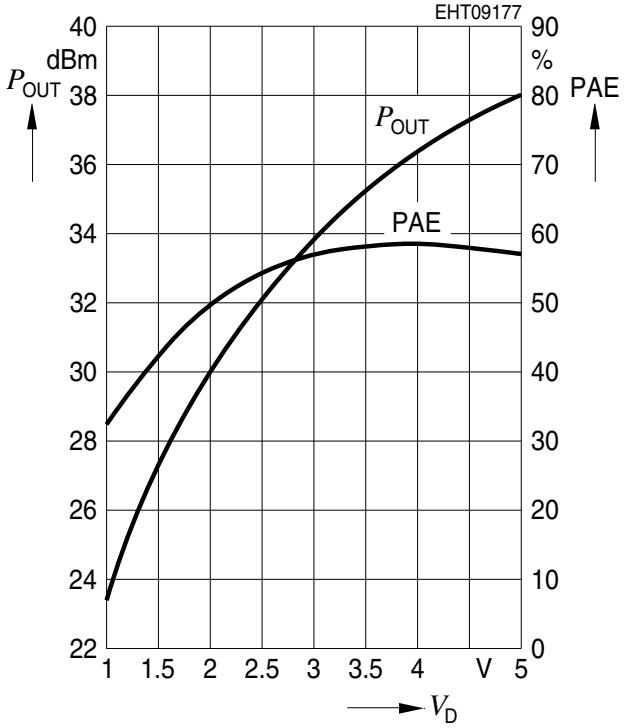
Output Power and PAE vs. V_G

V_D = 3.5 V, P_{IN} = 15 dBm, f = 900 MHz



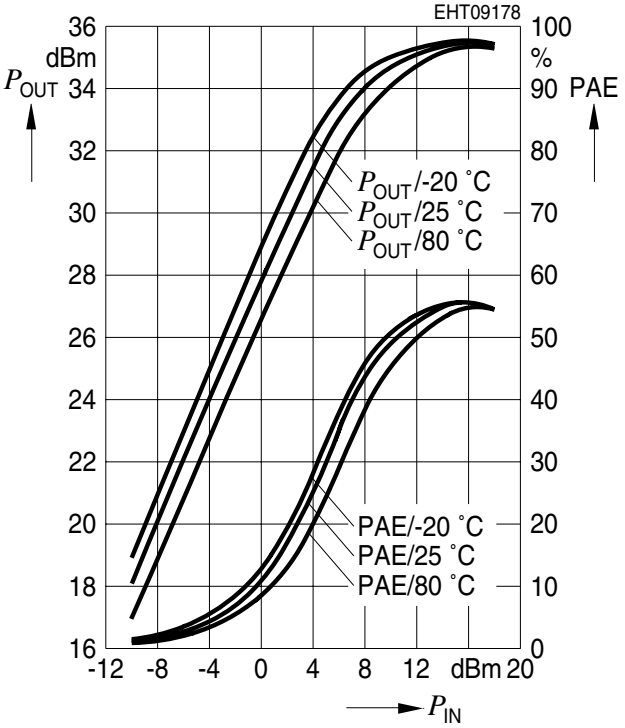
Output Power and PAE vs. V_D

V_G = – 1.5 V, P_{IN} = 15 dBm, f = 900 MHz



Temperature Characteristics GSM

V_D = 3.5 V, f = 900 MHz, V_G = – 1.5 V



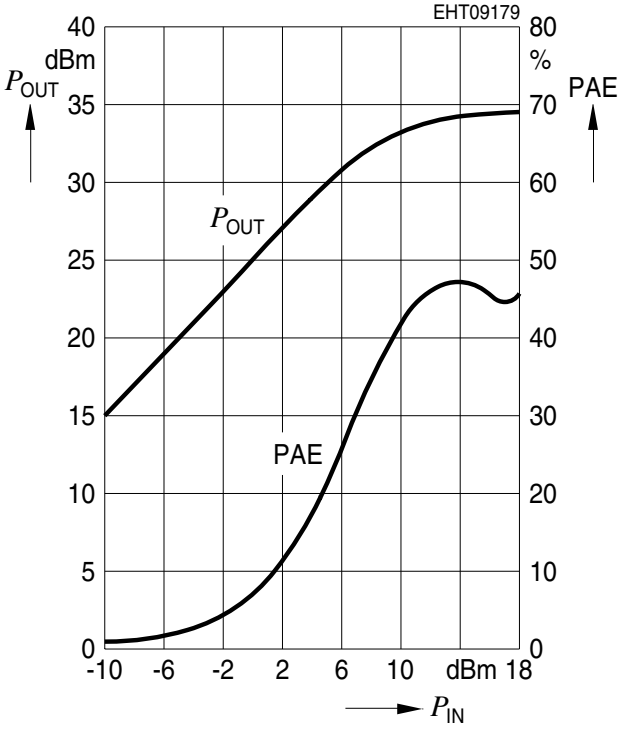
PCN(DCS1800)-Operation

Electrical Characteristics on PCN Application Board

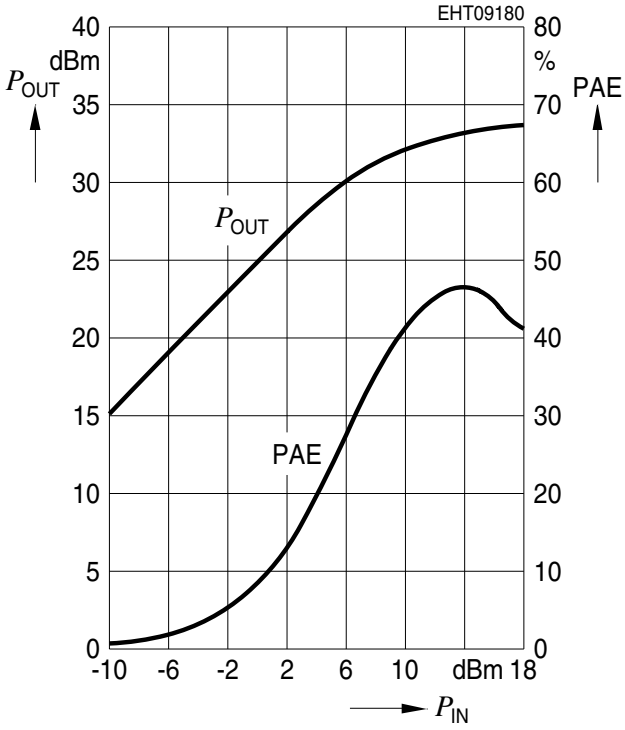
T_A = 25 °C, Z_S = Z_L = 50 Ω, duty cycle 12.5%, t_{ON} = 577 µs
unless otherwise specified

Parameters	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Frequency range	f	1710	–	1785	MHz	–
Supply current	I_{DD}	–	1.6	–	A	V_D = 3.5 V, P_{IN} = + 15 dBm
Power gain	G	–	19	–	dB	V_D = 3.5 V, P_{IN} = + 15 dBm
Output Power	P_O	–	32.1	–	dBm	V_D = 2.8 V, P_{IN} = + 15 dBm
Output Power	P_O	–	33.4	–	dBm	V_D = 3.2 V, P_{IN} = + 15 dBm
Output Power	P_O	–	34.0	–	dBm	V_D = 3.5 V, P_{IN} = + 15 dBm
Overall Power added Efficiency	PAE	–	45	–	%	V_D = 3.5 V, P_{IN} = + 15 dBm
Harmonics $2f_0$ $3f_0$	– –	– –	– 36 – 36	– –	dBc	–
Input VSWR	–	–	2:1	–	–	V_D = 3.5 V or V_D = 4.8 V
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 10 dBm, $V_D \leq$ 4.6 V, Z_S = 50 Ω, Load VSWR = 20:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level			–	P_{IN} = 10 dBm, V_D = 4.6 V, Z_S = 50 Ω, Load VSWR = 5:1 for all phase

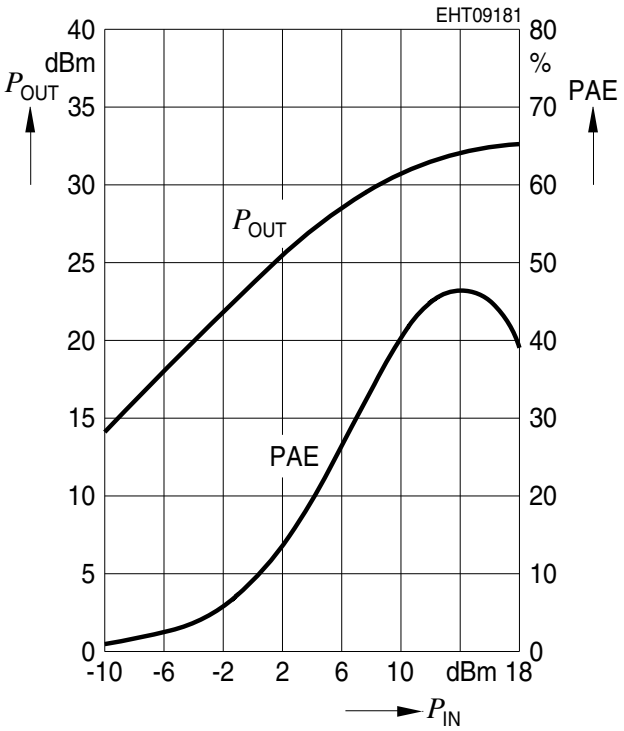
Output Power and PAE vs. Input Power
V_D = 3.5 V, V_G = – 1.7 V, f = 1750 MHz



Output Power and PAE vs. Input Power
V_D = 3.2 V, V_G = – 1.8 V, f = 1750 MHz

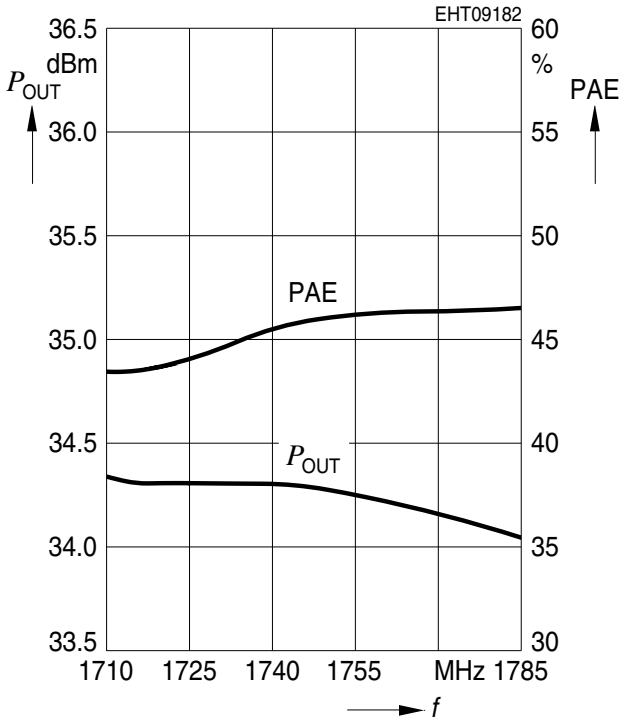


Output Power and PAE vs. Input Power
V_D = 2.8 V, V_G = – 1.9 V, f = 1750 MHz



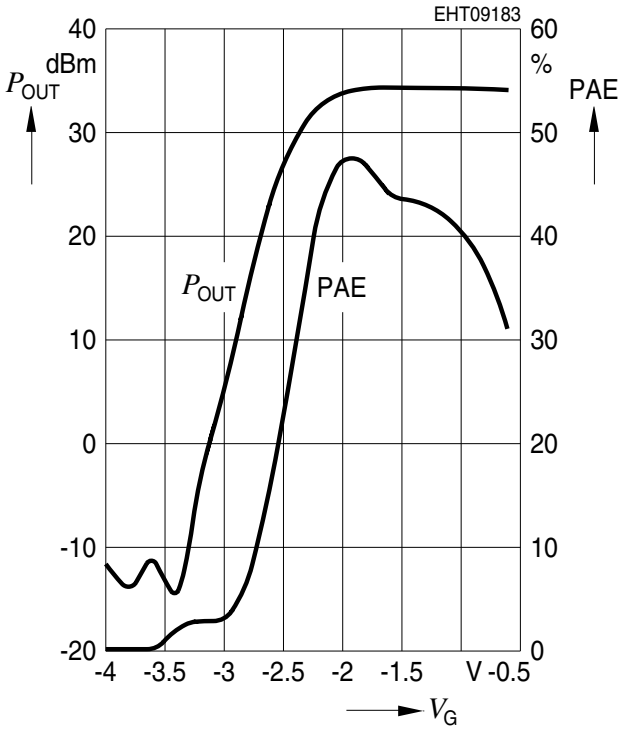
Output Power and PAE vs. Frequency

V_G = – 1.7 V, P_{IN} = 15 dBm, V_D = 3.5 V



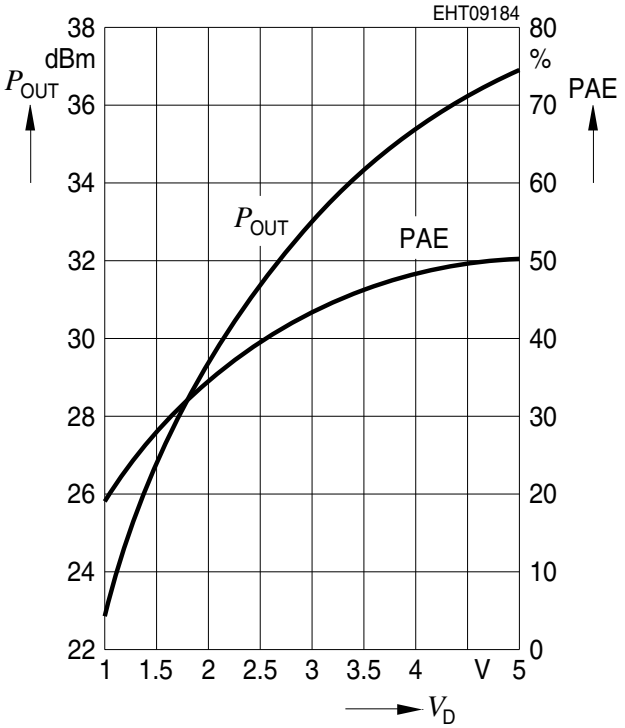
Output Power and PAE vs. V_G

V_D = 3.5 V, P_{IN} = 15 dBm, f = 1750 MHz



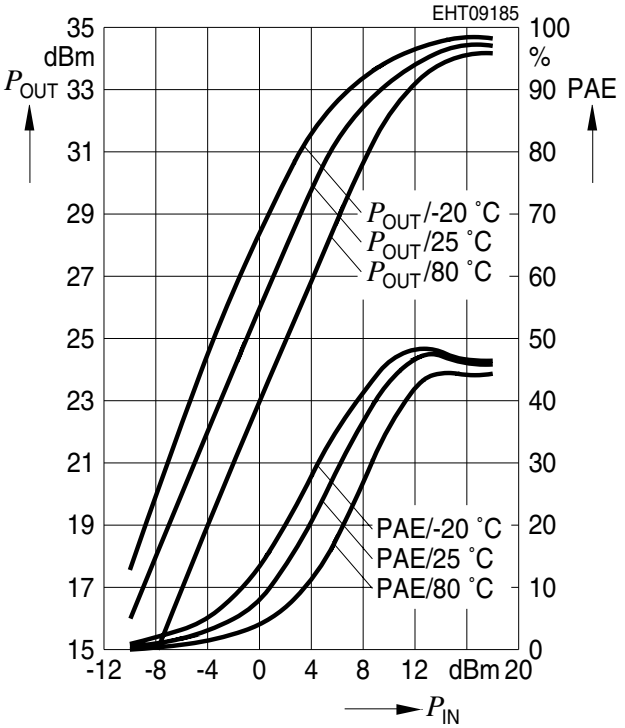
Output Power and PAE vs. V_D

V_G = – 1.7 V, P_{IN} = 15 dBm,
f = 1750 MHz



Temperature Characteristics PCN

V_D = 3.5 V, f = 1750 MHz, V_G = – 1.7 V



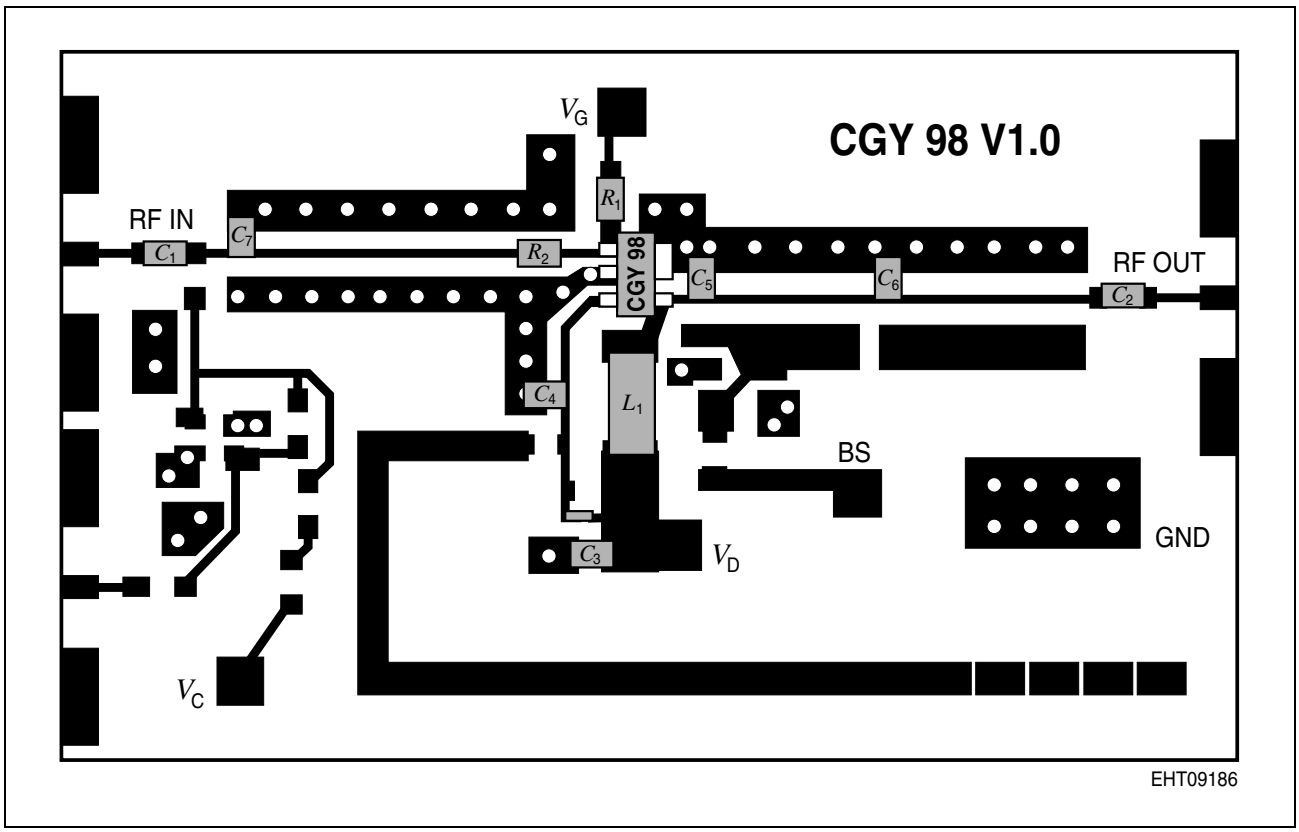


Figure 2 CGY 98 GSM Application Board

Board material: FR4 / 0.2 mm; Boardsize: 49 mm × 30 mm

Part List

Element	Value	Part Type	Element	Value	Part Type
L_1	33 nH	[1]	C_5	12 pF	0603[2]
C_1	1 nF	0603	C_6	6.8 pF	0603[2]
C_2	1 nF	0603	C_7	6.8 pF	0603
C_3	100 nF	0603	R_1	150 Ω	0603
C_4	1 nF	0603	R_2	6.8 Ω	0603

[1] 33 nH SMD-Inductor for drain3: Part number BV1250
distributed by Horst David GmbH, 85375 Neufarn, Germany,
Phone-No. +49-8165/9548-0, Fax-No. +49-8165/9548-28

[2] For maximum efficiency use high quality capacitors for the output matching: Part-number ACCU-P0603
distributed by AVX GmbH, 85757 Karlsfeld, Germany, Phone-No. +49-8131/9004-0

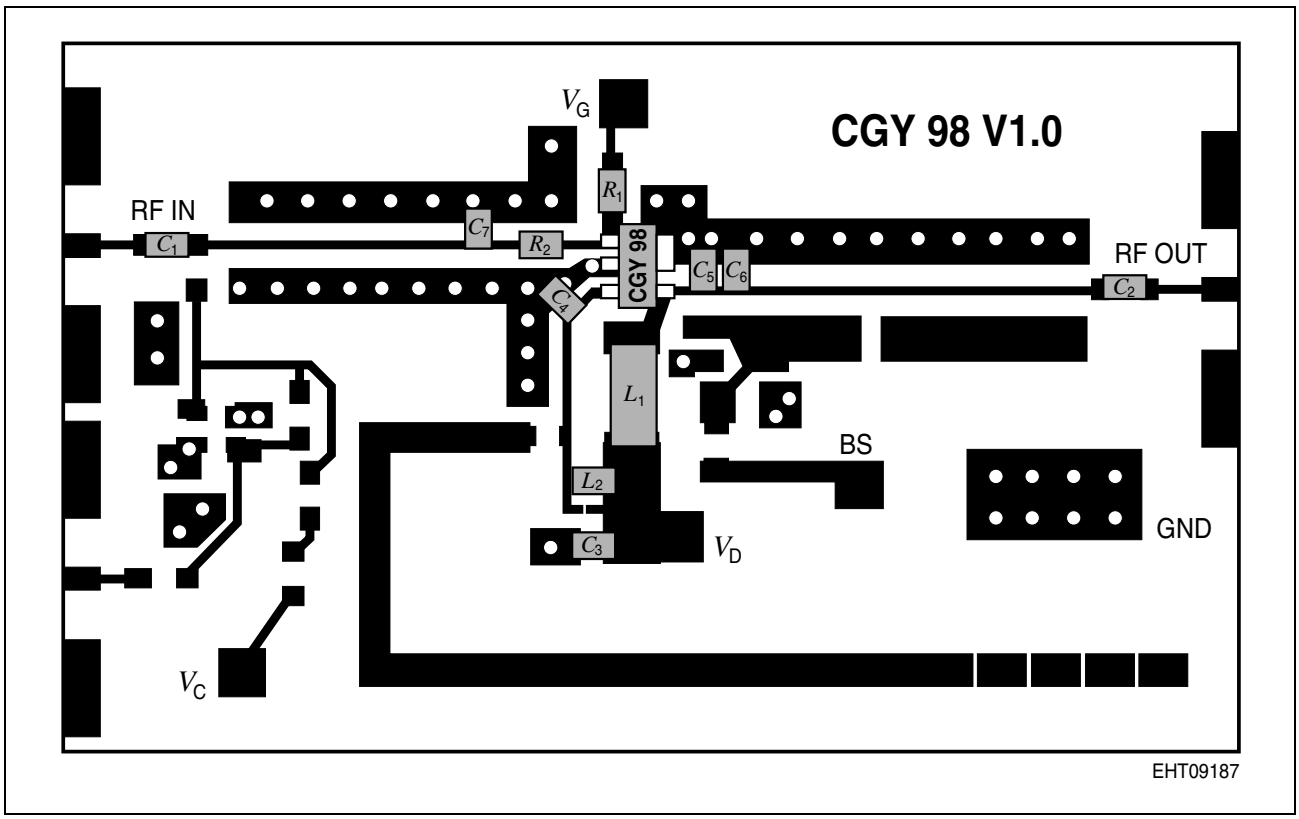


Figure 3 CGY 98 PCN Application Board

Board material: FR4 / 0.2 mm; Boardsize: 4.9 mm × 3.0 mm

Part List

Element	Value	Part Type	Element	Value	Part Type
L_1	33 nH	[1]	C_5	3 pF	0603[2]
L_2	33 nH	TOKO 0603 - LL 1608	C_6	3 pF	0603[2]
C_1	1 nF	0603	C_7	5.5 pF	0603
C_2	1 nF	0603	R_1	150 Ω	0603
C_3	100 nF	0603			
C_4	8 pF	0402			

[1] 33 nH SMD-Inductor for drain3: Part number BV1250
distributed by Horst David GmbH, 85375 Neufarn, Germany,
Phone-No. +49-8165/9548-0, Fax-No. +49-8165/9548-28

[2] For maximum efficiency use high quality capacitors for the output matching: Part-number ACCU-P0603
distributed by AVX GmbH, 85757 Karlsfeld, Germany, Phone-No. +49-8131/9004-0

Determination of Permissible Total Power Dissipation for Continuous and Pulse Operation

The dissipated power is the power which remains in the chip and heats the device. It does not contain RF signals which are coupled out consistently.

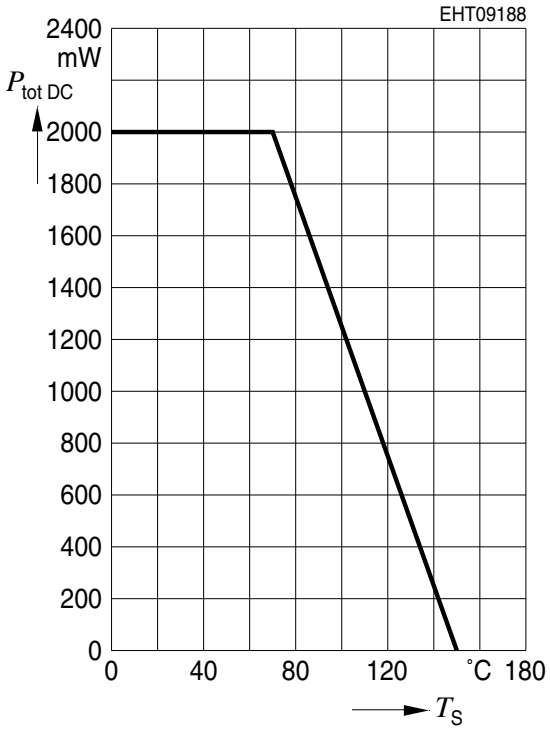
a) Continuous Wave / DC Operation

For the determination of the permissible total power dissipation $P_{tot\text{-}DC}$ from the diagram below it is necessary to obtain the temperature of the soldering point T_S first. There are two cases:

- When R_{thSA} (soldering point to ambient) is not known: Measure T_S with a temperature sensor at the leads were the heat is transferred from the device to the board (normally at the widest source or ground lead for GaAs). Use a small sensor of low heat transport, for example a thermoelement (< 1 mm) with thin wires or a temperature indicating paper while the device is operating.
- When R_{thSA} is already known:

  $T_S = P_{Diss} \times R_{thSA} + T_A$

Permissible Total Power Dissipation in DC Operation



Temperature of soldering point, T_S

b) Pulsed Operation

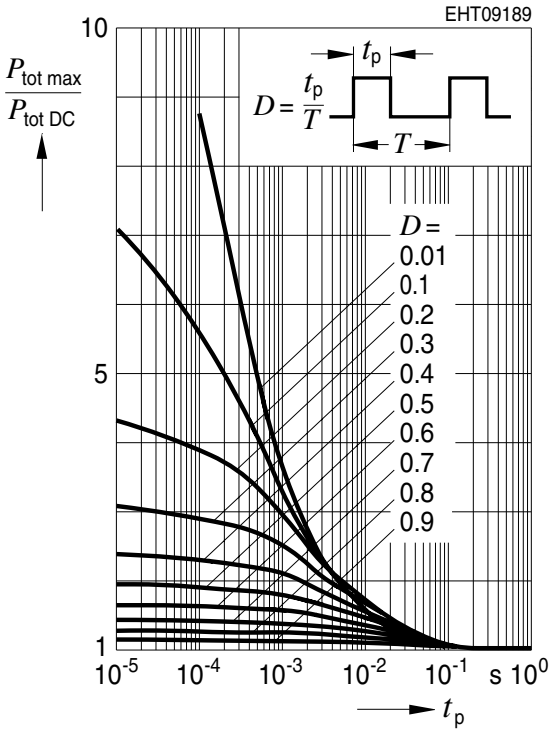
For the calculation of the permissible pulse load $P_{\text{tot-max}}$ the following formula is applicable:

$P_{\text{tot-max}} = P_{\text{tot-DC}} \times \text{Pulse Factor} = P_{\text{tot-DC}} \times (P_{\text{tot-max}}/P_{\text{tot-DC}})$

Use the values for $P_{\text{tot-DC}}$ as derived from the above diagram and for the Pulse Factor = $P_{\text{tot-max}}/P_{\text{tot-DC}}$ from the following diagram to get a specific value.

Pulse Factor

$P_{\text{tot-max}}/P_{\text{tot-DC}} = f(t_p)$



$P_{\text{tot-max}}$ should not exceed the absolute maximum rating for the dissipated power

P_{Pulse} = “Pulse peak power”

Reliability Considerations

The above procedure yields the upper limit for the power dissipation for continuous wave (cw) and pulse applications which corresponds to the maximum allowed channel temperature. For best reliability keep the channel temperature low. The following formula allows to track the individual contributions which determine the channel temperature.

T_{Ch} =	(P_{Diss}/Pulse Factor ×	R_{thChS}) +	T_S
Channel temperature (= junction temperature)	Power dissipated in the chip, divided by the applicable pulse factor (= 1 for DC and CW). It does not contain decoupled RF- power	R_{th} of device from channel to soldering point	Temperature of soldering point, measured or calculated

Soldering Recommendation

- Foot Print — Drawing C63060-A2120-A001-01-0027
- Soldering — Wave soldering: unsuitable
  Reflow soldering: suitable, max. 3 times
  (IR or VPR)

  Soldering profile:

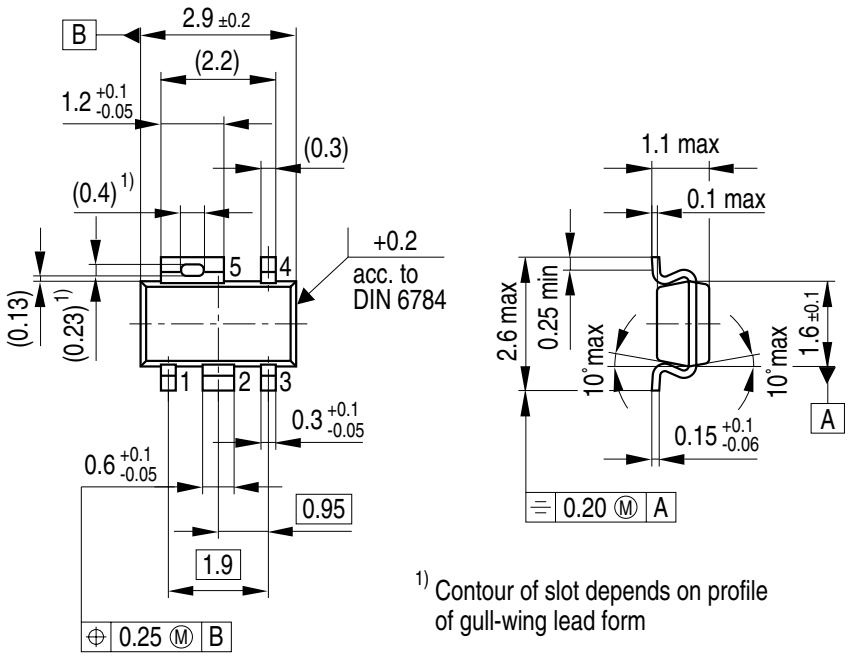
Ramp-up preheating	Temperature gradient:	max. + 2 K/s
	Time at 100 - 150 °C:	min. 90 s
Ramp-up peak	Temperature gradient:	max. + 6 K/s
Exposure to molten solder	Above 183 °C	max. 150 s
Typ. solder temperature	Typ. 215 - 245 °C	max. 30 s
Peak temperature	Max. peak 260 °C	max. 10 s
Ramp-down	Temperature gradient:	min. – 6 °C/s

  (see also soldering standard profile of data book “Package information”)

  Comments: Slow ramp-up, long preheating phase and low max. temperature recommended
- Solder Paste Thickness — 150 - 200 µm
- Control of Soldering (voids) — - Visual inspection
  - Cross sectioning
  - Measurement of case temperature / thermal resistance case to ambient
- JEDEC A-112A — Level 1 storage floor life at 30 °C / 90% unlimited
- IPC-9501 (IPC-4202) — Level 111 storage floor life at 30 °C / 60% unlimited
  IR/Convection; max. 245 °C; < 6 K/s

Package Outlines

SCT-595
(Special Package)



1) Contour of slot depends on profile of gull-wing lead form

GPW05997

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm