



# Wireless Components

7 x 5 Video Matrix Switch

TDA 6920 Version 1.0

Specification August 1999

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## Product Info

### General Description

The TDA 6920 switches 7 video input sources to 5 outputs. Each output can be switched to only one input, but one input can be switched to all outputs. The C-input may be combined with one CVBS input as Y for Y+C (S-VHS) operation. Y+C operation is selected by bus.

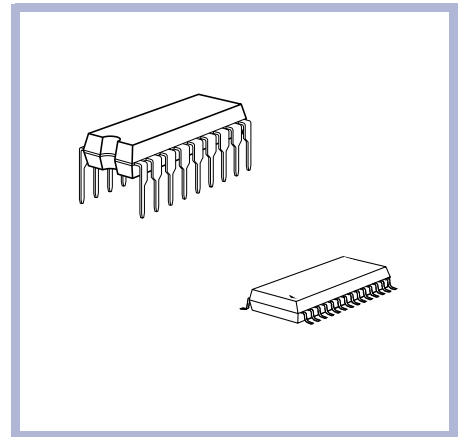
### Features

- Fast I<sup>2</sup>C-BUS controlled (max. 400 kHz)
- Cascadable (2 bus addresses)
- 7 CVBS inputs, 5 outputs  
3 inputs with clamp disable by bus
- 1 input selectable as Y-input (S-VHS)
- 1 additional C-input (S-VHS)
- Y+C operation for S-VHS selected by bus
- Fully ESD protected
- -60 dB max. crosstalk at 5 MHz (P-DSO-28 only)

### Application

- Television sets
- Satellite receivers

### Package



- Low operating voltage of 7.5 V
- 5V operation is possible with reduced output signals of max. 2 V<sub>pp</sub>
- 15 MHz minimum bandwidth
- Noise insensitive clamping inputs
- low impedance off condition separate for each output
- Video mixing desks

### Ordering Information

Type	Ordering Code	Package
TDA 6920	Q67000-A5200 GEG	P-DIP-18
TDA 6920X	Q67007-A5225 GEG	P-DSO-28

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# 2 Product Description

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## 2.1 Overview

The TDA 6920 switches 7 video input sources to 5 outputs. Each output can be switched to only one input, but one input can be switched to all outputs. The C-input may be combined with one CVBS input as Y for Y+C (S-VHS) operation. Y+C operation is selected by bus.

## 2.2 Features

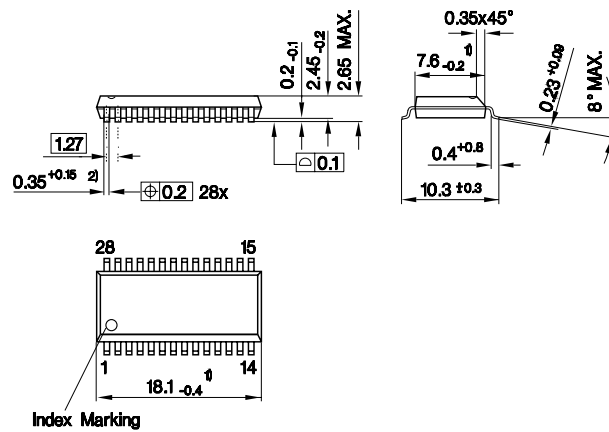
- Fast I<sup>2</sup>C-BUS controlled (max. 400 kHz)
- Cascadable (2 bus addresses)
- 7 CVBS inputs, 5 outputs, 3 inputs with clamp disable by bus
- 1 input selectable as Y-input (S-VHS)
- 1 additional C-input (S-VHS)
- Y+C operation for S-VHS, selected by bus
- Fully ESD protected
- -60 dB max. crosstalk at 5 MHz (P-DSO-28 only)
- Low operating voltage of 7.5 V
- 5V operation is possible with reduced output signals of max. 2 V<sub>pp</sub>
- 15 MHz minimum bandwidth
- Noise insensitive clamping inputs
- low impedance off condition, separate for each output

## 2.3 Application

- Television sets
- Satellite receivers
- Video mixing desks

## 2.4 Package Outlines

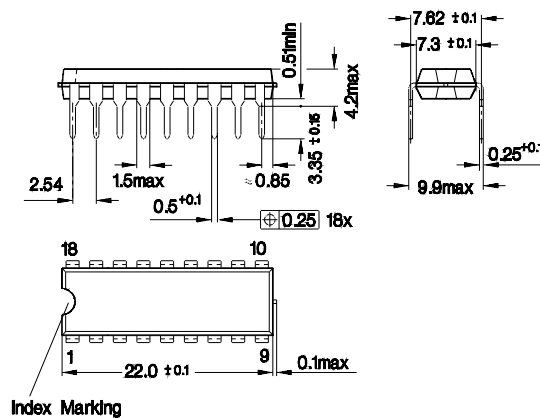
### P-DSO-28



Index Marking

- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion of 0.05 max. per side

### P-DIP-18



Index Marking

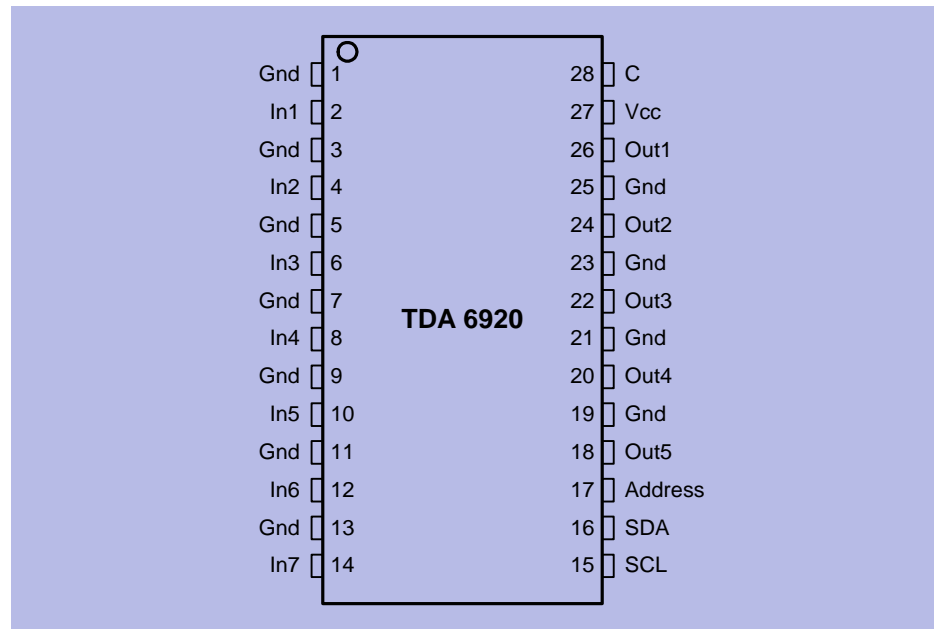
# 3 Functional Description

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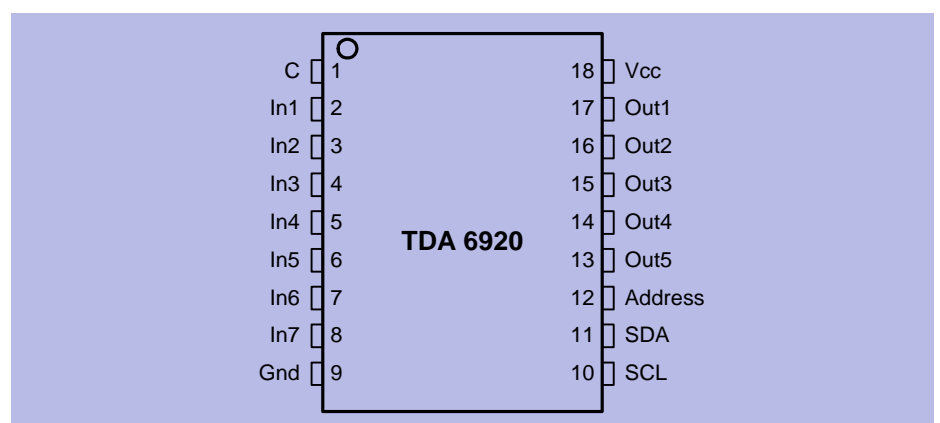


### 3.1 Pin Configuration



Pin\_config\_1.wmf

Figure 3-1 Pin Configuration P-DSO-28



Pin\_config\_2.wmf

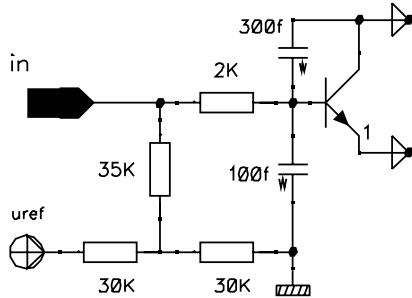
Figure 3-2 Pin Configuration P-DIP-18

### 3.2 Pin Definition and Function

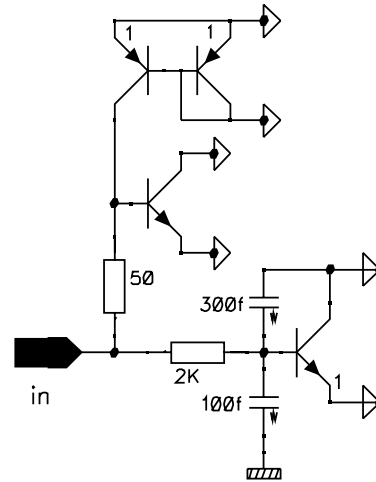
**Table 3-1 Pin Definition and Function**

Symbol	Pin		Function
	P-DIP-18	P-DIP-28	
GND	-	1	Signal + power supply ground
IN1	2	2	CVBS input 1
GND	-	3	Signal + power supply ground
IN2	3	4	CVBS input 2
GND	-	5	Signal + power supply ground
IN3	4	6	CVBS input 3
GND	-	7	Signal + power supply ground
IN4	5	8	CVBS input 4
GND	-	9	Signal + power supply ground
IN5	6	10	CVBS input 5
V ref3	-	11	Reference Voltage for external use
IN6	7	12	CVBS input 6
GND	9	13	Power supply ground
IN7	8	14	CVBS input 7
SCL	10	15	I <sup>2</sup> C-Bus clock
SDA	11	16	I <sup>2</sup> C-Bus data
Address	12	17	Address selection
OUT5	13	18	CVBS output 5
GND	-	19	Signal + power supply ground
OUT4	14	20	CVBS output 4
GND	-	21	Signal + power supply ground
OUT3	15	22	CVBS output 3
GND	-	23	Signal + power supply ground
OUT2	16	24	CVBS output 2
GND	-	25	Signal + power supply ground
OUT1	17	26	CVBS output 1
VCC	18	27	Positive power supply voltage
C	1	28	Separate color adding input for input 1

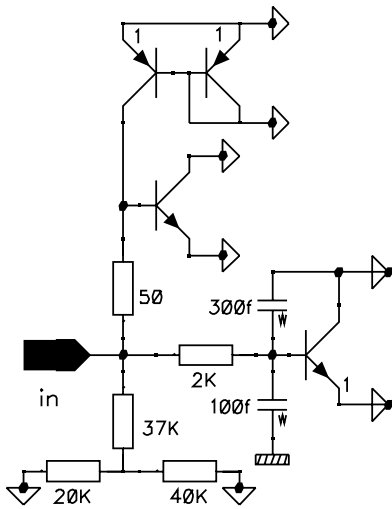
### 3.3 Pin Description



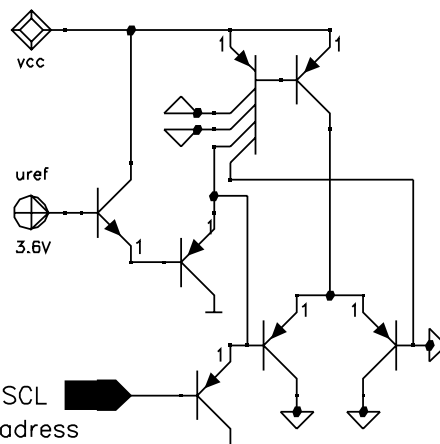
C ( color input )



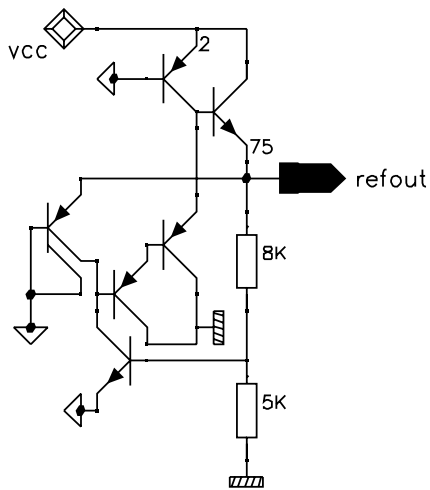
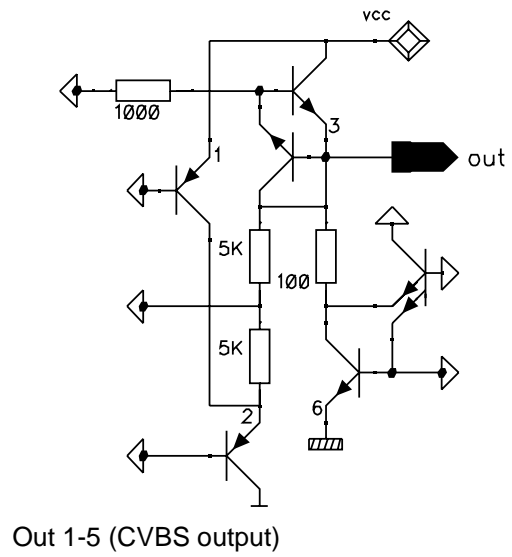
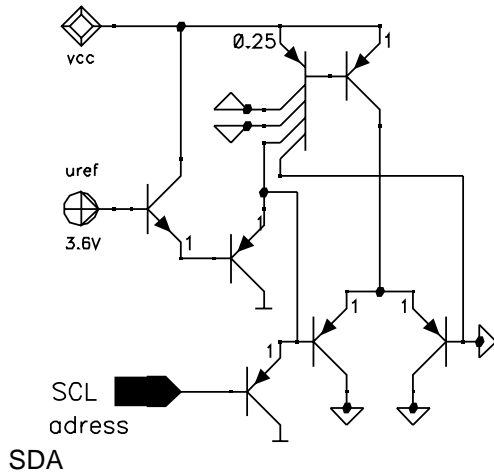
In 2,5,6,7 ( CVBS input )



In 2,3,4 ( CVBS input )



SCL , Address



Vref (S=-28 only)

### 3.4 Functional Description

The main function of the IC is to switch 7 input video sources to 5 outputs.

Each output can be switched to only one input.

It is possible to have the same input connected to several outputs.

3 of the inputs can be used as non-clamping-input, switching is controlled by bus.

The clamping function of the other 4 inputs can be switched off by external resistor divider.

All switching possibilities are controlled by the I<sup>2</sup>C-BUS.

All outputs can be switched to low impedance off condition by the I<sup>2</sup>C-BUS.

Driving 75 Ω load requires external transistors.

The recommended coupling capacitor at each input is 47 nF.

Each clamping input requires a 75 Ω (max. 500 Ω) termination resistor.

Operation without or with a termination resistor greater than 500 Ω causes malfunction of the new high performance clamping circuit.

Unused input's should be directly grounded.

6 x 8 bits are necessary to determine one complete configuration change (1 addressbyte, 5 databytes).

Minimum configuration change for 1 output needs 2 x 8 bit (1 addressbyte, 1 databyte).

Power on reset state: all 5 outputs switched to input 1, all inputs clamped, Y+C off.

### 3.5 Block Diagram (P-DSO-28)

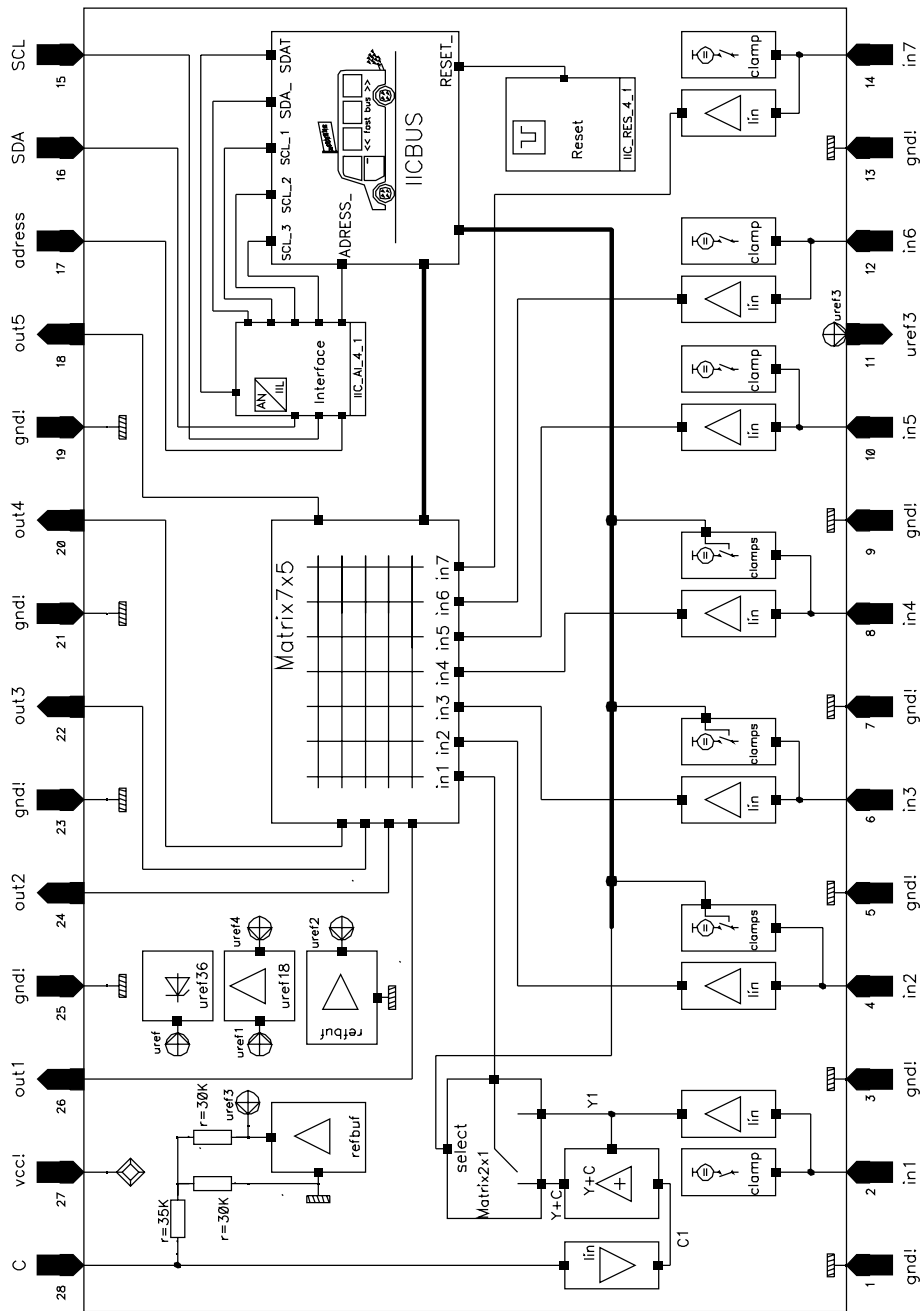


Figure 3-3 Block Diagram (P-DSO-28)

# 4 Applications

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## 4.1 Circuits

### 4.1.1 Application Circuit P-DSO-28

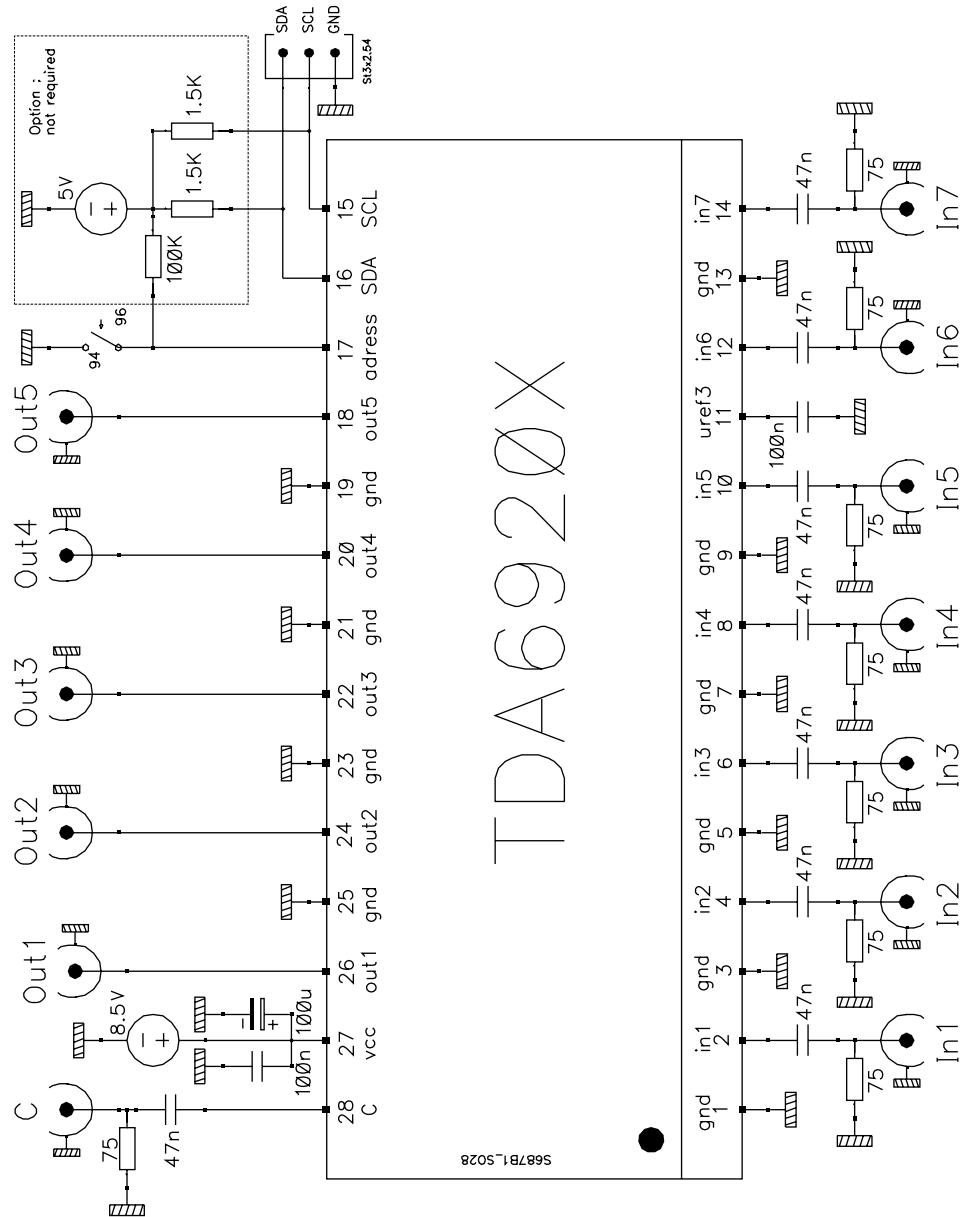


Figure 4-1 Application Circuit P-DSO-28 (clamping inputs)



4.1.2 Application Circuit P-DSO-28

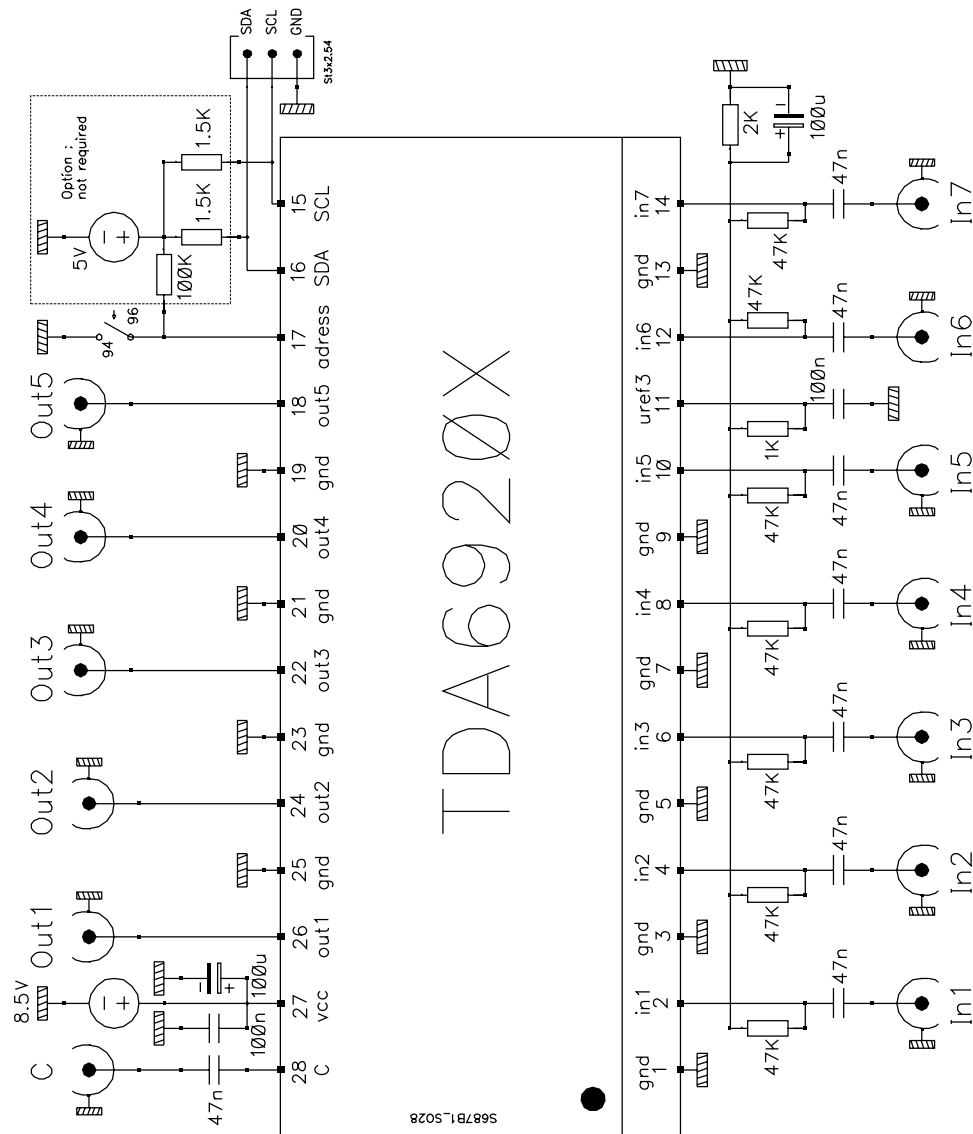


Figure 4-2 Application Circuit P-DSO-28  
(no clamping inputs with clamping override)

### 4.1.3 Application Circuit P-DIP-18

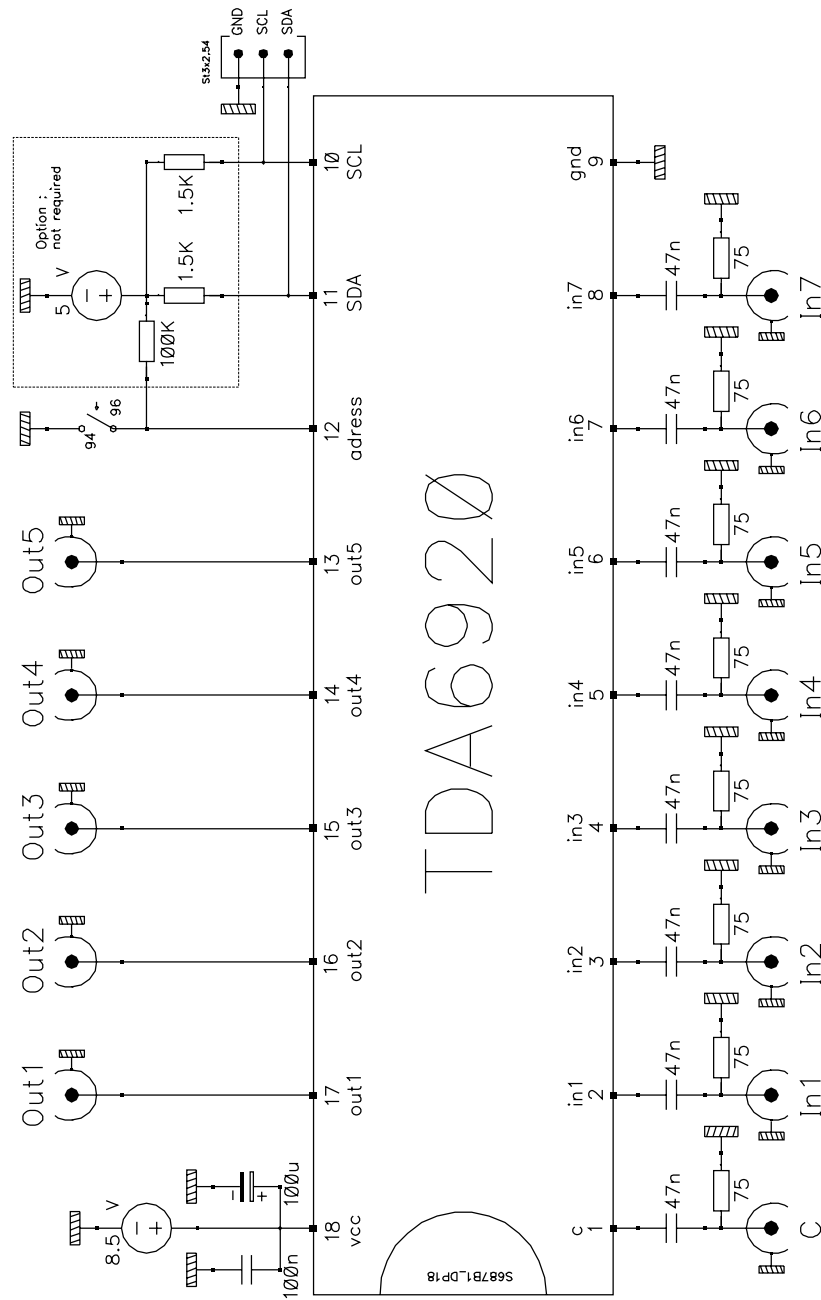


Figure 4-3 Application Circuit P-DIP-18

# 5 Reference

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## 5.1 Electrical Data

### 5.1.1 Absolute Maximum Ratings



#### WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

**Table 5-1 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Supply voltage ( $V_{CC}$ )	$V_{CC}$	0	14	V	
Reference voltage ( SO-28 only )	$V_{ref3}$	0	5	V	
Reference current ( $R_{Lmin} = 1k\Omega$ )	$I_{ref3}$		3.5	mA	
Output voltage	$V_{out1-out5}$	0	$V_{CC}$	V	
Output current ( $R_{Lmin} = 500\Omega$ )	$I_{out1-out5}$		5	mA	
Input voltage	$V_C$	0	$V_{CC}$	V	
Input voltage	$V_{In1-In7}$	0	$V_{CC}$	V	
SCL, SDA, address input voltage	$V_{SDA, SCL, Address}$	0	$V_{CC}$	V	
ESD-voltage all pins HBM ( $R=1.5k\Omega$ , $C=100pF$ )	$V_{ESD}$	-6	6	kV	
Junction temperature	$T_j$		150	$^{\circ}C$	
Storage temperatue	$T_{stg}$	- 40	125	$^{\circ}C$	
Thermal resistance ( system - air)	$T_{thSA}$		75	K/W	

All voltage values are referenced to ground, if not stated otherwise.

### 5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

**Table 5-2 Operating Range**

Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
		min	max				
Supply voltage	$V_{CC}$	7.5	13.2	V			
Absolut minimum supply voltage (only usable with reduced output signals of max. 2V <sub>pp</sub> )	$V_{CC}$	4.5		V			
Reference voltage ( SO-28 only )	$V_{ref3}$	3.3	3.9	V			
Video-input frequency range - 3 dB	$f_{in\ In1-In7,C}$	0	20	MHz			
Video-input AC-voltage ( color )	$V_C$		1.0	V <sub>pp</sub>			
Video-input AC-voltage ( Y, CVBS )	$V_{In1-In7}$		1.7	V <sub>pp</sub>			
Video-output AC-voltage	$V_{out1-out5}$		3.4	V <sub>pp</sub>			
Input DC-voltage	$V_C$	1.3	2.3	V			
Input DC-voltage ( clamping )	$V_{In1-In7}$	1.8	3.5	V			
Input DC-voltage ( non clamping )	$V_{In2,3,4}$	1.5	3.2	V			
Input Source-Impedance (clamping)	$R_{i\ In1-In7}$	0	500	$\Omega$			
I <sup>2</sup> C bus clock	$f_{in\ SDA, SCL}$	0	500	kHz			
Ambient temperature during operation	$T_A$	-10	85	°C			

All voltage values are referenced to ground, if not stated otherwise.

### 5.1.3 AC/DC Characteristics

**Table 5-3 AC/DC Characteristics with  $T_A = 25\ ^\circ\text{C}$ ,  $V_{CC} = 8.5\ \text{V}$**

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Total current consumption	$I_{VCC}$		42	58	mA	$R_L = \infty$		
Reference voltage (SO-28 only)	$V_{ref3}$	3.4	3.6	3.8	V	$R_L = \infty$		
Output DC-voltage (clamping)	$V_{out1-out5}$		1.8		V	$V_{C,In1-In7} = 0\ V_{pp}$		
Output DC-voltage (output off)	$V_{out1-out5}$		0.8		V	$V_{C,In1-In7} = 0\ V_{pp}$		
Output current	$I_{out1-out5}$	0.5	1.0	2.0	mA	$V_{out} = 2V, I_n = 0\ V_{pp}$		
Input DC-voltage	$V_C$		1.8		V	$V_C = 0\ V_{pp}$		

**Table 5-4 AC/DC Characteristics with  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 8.5\text{ V}$  (continued)**

	Symbol	Limit Values			Unit	Test Conditions	Item
		min	typ	max			
Input DC-voltage ( clamping )	$V_{In1-In7}$		1.8		V	$V_{In1-In7} = 0 V_{pp}$	
Input current ( clamping )	$I_{In1-In7}$		0.33	1	$\mu\text{A}$	$V_{In1-In7} = 0 V_{pp}$	
Input DC-voltage ( for ext. clamping override )	$V_{In1-In7}$		2.4		V	$V_{In1-In7} = 0 V_{pp}$	
Input DC-voltage (non-clamping, Bus controlled)	$V_{In2,3,4}$		2.4		V	$V_{In2,3,4} = 0 V_{pp}$	
Input current ( SCL, SDA, address)	$I_{SDA, SCL}$ $I_{Address}$		0.1	0.4	$\mu\text{A}$	$V_{SDA, SCL} = 0\text{ V}$ $V_{Address} = 0\text{ V}$	
Output current ( SDA )	$I_{SDA}$	6			mA	$V_{SDA} = 0.6\text{ V}$	
Output voltage low ( SDA )	$V_{SDA}$ $V_{SDA}$	0 0	0.2 0.3	0.4 0.6	V V	$I_{SDA} = 3\text{ mA sink}$ $I_{SDA} = 6\text{ mA sink}$	
SCL,SDA, address (96 hex) : high	$V_{SDA, SCL}$ $V_{Address}$	3.0		$V_{CC}$	V		
SCL,SDA, address (94 hex) : low	$V_{SDA, SCL}$ $V_{Address}$	0		1.5	V		
SCL,SDA,address ( hysteresis )	$V_{SDA, SCL}$ $V_{Address}$	0.2		1	V	dependant on input frequency	
Video bandwidth	$P_{out/in}$	15	20		MHz	-3dB point	
Video gain	$V_{out}/V_{in}$	1.9	2.0	2.1			
Crosstalk ( 0 - 5 MHz ) SO-28	A		-65	-60	dB	inputs $75\Omega$ to gnd	
Crosstalk ( 0 - 5 MHz ) SO-28	A		-55	-50	dB	inputs $500\Omega$ to gnd	
Crosstalk ( 0 - 5 MHz ) DIP-18	A		-62	-57	dB	inputs $75\Omega$ to gnd	
Crosstalk ( 0 - 5 MHz ) DIP-18	A		-45	-40	dB	inputs $500\Omega$ to gnd	
Input AC-voltage	$V_C$		0.75	1	$V_{pp}$	sinus	
Input AC-voltage	$V_{In1-In7}$		1	1.5	$V_{pp}$	clamped	
Input AC-voltage ( sinus )	$V_{In2,3,4}$		1	1.5	$V_{pp}$	non clamped	
Output AC-voltage	$V_{out1-out5}$		2	3	$V_{pp}$		
I <sup>2</sup> C bus clock	$f_{in\ SDA, SCL}$		400	500	kHz		
Output linearity	$DG_{out1-out5}$		0.2	1	%	$R_L = \infty$	
Input resistance ( non-clamping )	$R_{C,In2,3,4}$	40	50		$k\Omega$		
Input Source-Impedance ( clamping )	$R_{In1-In7}$	0	75	500	$\Omega$		
Input Coupling-Capacitor ( clamping )	$C_{In1-In7}$		47 10		nF $\mu\text{F}$	CVBS-signal >20Hz Audiosignal	
Output dyn. impedance	$R_{out1-out5}$		50	75	$\Omega$		

## 5.2 Address selection (fast I<sup>2</sup>C-Bus)

1st byte of transmission (8 bit)

Table 5-5			
HEX	binary		address pin
	MSB	LSB	
9 6	1 0 0 1	0 1 1 0	VCC (min. 3V)
9 4	1 0 0 1	0 1 0 0	GND

## 5.3 Data selection ( fast I<sup>2</sup>C-BUS )

2nd byte of transmission (8 bit)

Table 5-6 Output selection (3bit, 7bit must always be 0)			
b7 b6*	b5 b4 b3	b2 b1 b0*	selected output
0 x	0 0 0	x x x	- not used
0 x	0 0 1	x x x	out1
0 x	0 1 0	x x x	out2
0 x	0 1 1	x x x	out3
0 x	1 0 0	x x x	out4
0 x	1 0 1	x x x	out5
0 x	1 1 0	x x x	- not used
0 x	1 1 1	x x x	- not used

\* ....X = don' t care

Table 5-7 Input selection clamped (3 bit, bit7 must always be 0)			
b7 b6	b5 b4 b3*	b2 b1 b0	selected output
0 x	x x x	0 0 0	output off condition
0 0	x x x	0 0 1	in1
0 0	x x x	0 1 0	in2
0 0	x x x	0 1 1	in3
0 0	x x x	1 0 0	in4
0 x	x x x	1 0 1	in5
0 x	x x x	1 1 0	in6
0 x	x x x	1 1 1	in7

\* ....X = don' t care

## 5.4 Data Mode Selections (fast I2C-Bus) continued

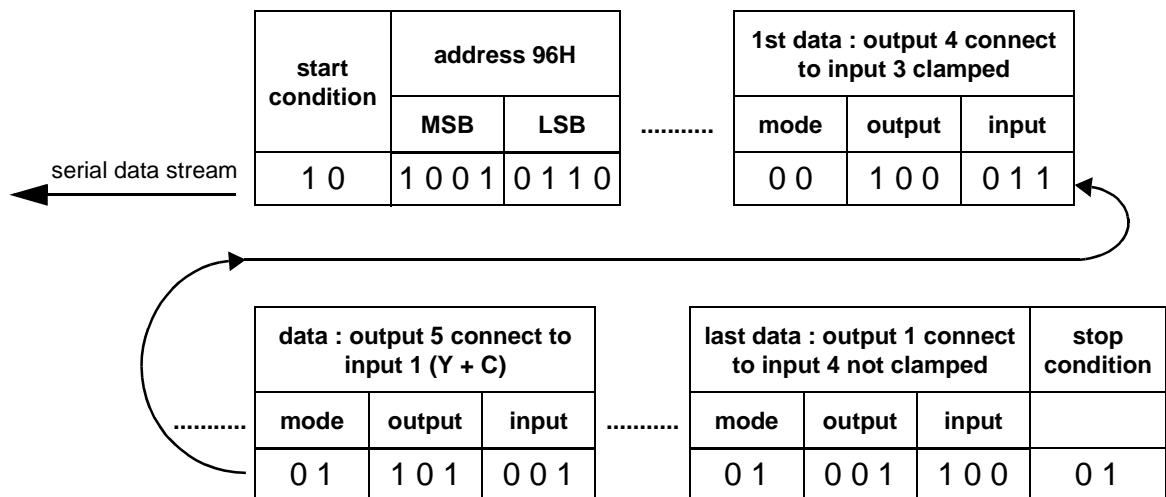
2nd byte of transmission ( 8 bit )

Table 5-8 Input selection non clamped / Y+C (Y:always clamped; C:non clamped) ; (3 bit, bit 7 should always be 0)			
b7 b6	b5 b4 b3*	b2 b1 b0	selected input
0 0	x x x	0 0 1	in1, (Y+C) off
0 0	x x x	0 1 0	in2, clamp on
0 0	x x x	0 1 1	in3, clamp on
0 0	x x x	1 0 0	in4, clamp on
0 1	x x x	0 0 1	in1, (Y+C) on
0 1	x x x	0 1 0	in2, clamp off
0 1	x x x	0 1 1	in3, clamp off
0 1	x x x	1 0 0	in4, clamp off

\* ....X = don' t care (if only input operation mode change is requested, b5, b4, b3 should be 0, 0, 0 : no output configuration is changed.)

## 5.5 BUS Protocol ( fast I<sup>2</sup>C-BUS )

Programming Example : SDA sequence





### 5.6 Test Circuits

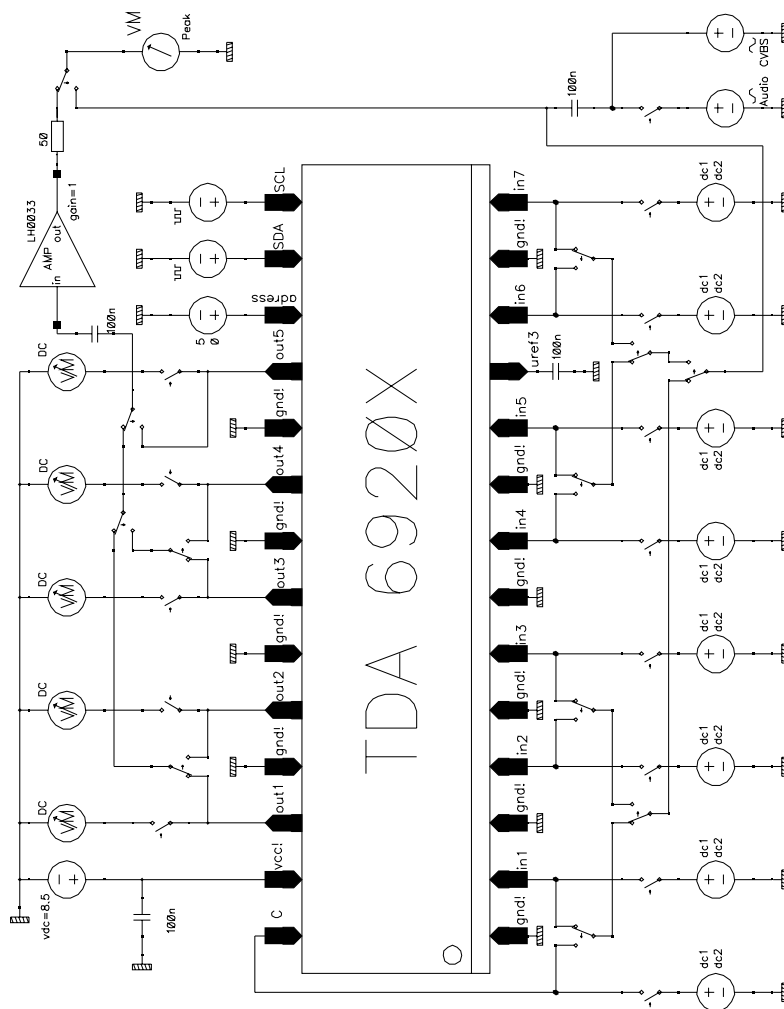


Figure 5-1 Test circuit P-DSO-28

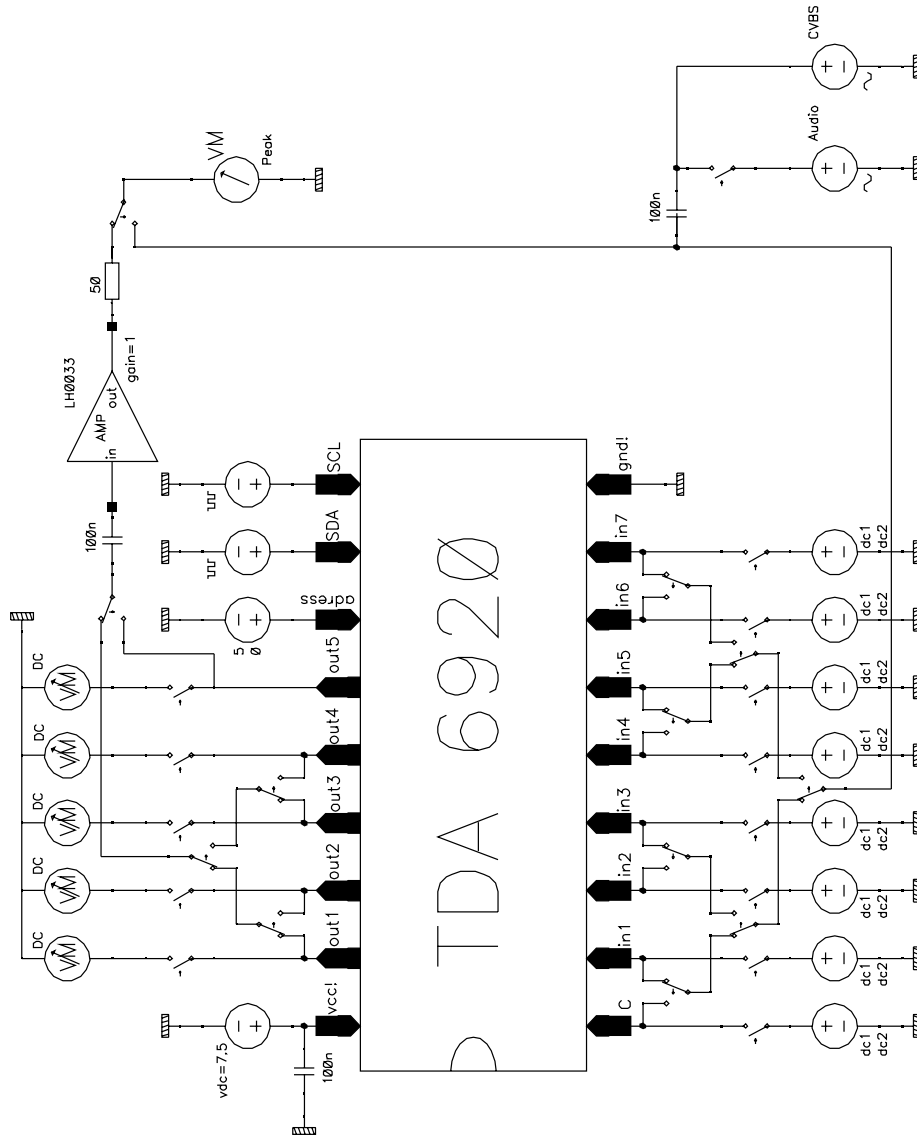
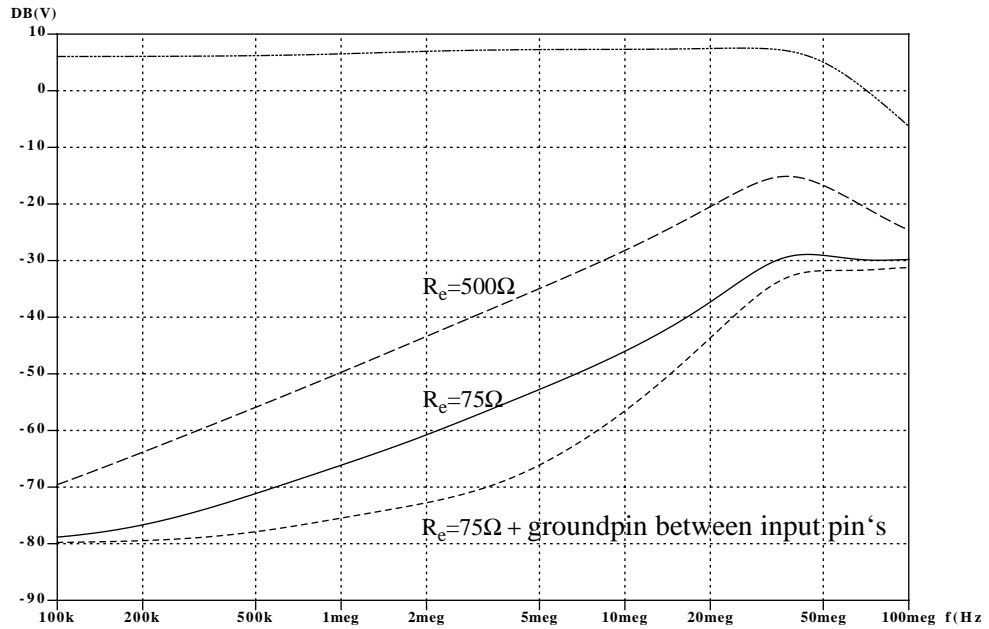


Figure 5-2 Test circuit P-DIP-18

## 5.7 Electrical Diagramms

Typical frequency response and crosstalk (simulated) for P-DSO-28 package



- Conditions:  $V_{CC} = 8.5V$  , all outputs selected to one different input;
- response: the measured output has max. signal on the selected input;
- crosstalk : the measured output has no signal on the selected input, another input has max. signal.