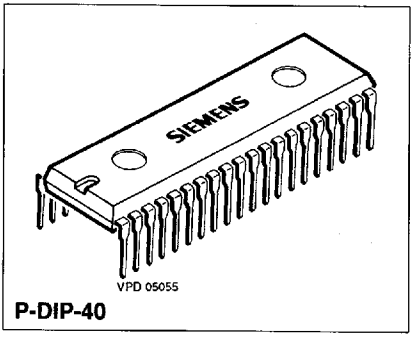
Video Processor

SDA 5248

Preliminary Data

MOS IC

Features



P-DIP-40

- I^2C bus interface with complete direct access to the memory area.
- Uses 64 Kx4 and 256 Kx4 dynamic RAM's
- Can store 32 or 128 teletext pages and acquire 4 pages simultaneously
- Optional assignment of the 4 acquisition circuits and bank select of the 128 memory areas via the 8 page memory pointers
- Suitable for TOP Text
- Access page display via page memory pointers
- I^2C bus interface with complete direct access to the memory area
- Memory clear function for 8 pages after power-on
- Memory clear function via I^2C bus for all pages
- Internal 24-MHz PLL for memory tuning
- 2 free programmable circuit outputs
- 12x10 dot matrix for characters and graphic
- Extra display row for status messages
- Acquisition during the vertical blanking interval or for cable text during all lines
- 60-Hz recognition and display without additional hardware
- Field detection for non-interlace display
- STATUS information for asynchronous operation
- Forced synchronization possibility to the CBVS signal either by inferior signal quality
- East European character set SDA 5248C2
- West European character set SDA 5248C1

Type	Ordering Code	Package
SDA 5248C1	Q67100-H5074	P-DIP-40
SDA 5248C2	Q67100-H5052	P-DIP-40

The SDA 5248 multipage text is a derivate of the SDA 5243 including some additional functional blocks. Using this device it is possible tp process up to 128 pages stored in an external DRAM. The relation between the 4 acquisition circuits available and the addresses of the page memory can be handled much more flexible than before.

In the SDA 5248 chip there is now a version of our teletext processors available that can manage up to 128 pages of teletext in an external dynamic RAM. SDA 5248 is upward compatible in software with SDA 5243 and can be operated in the same hardware environment as the latter and with the same SDA 5231-2 data slicer. The pinning differs only where the memory interface is concerned. SDA 5248 offers extra features however:

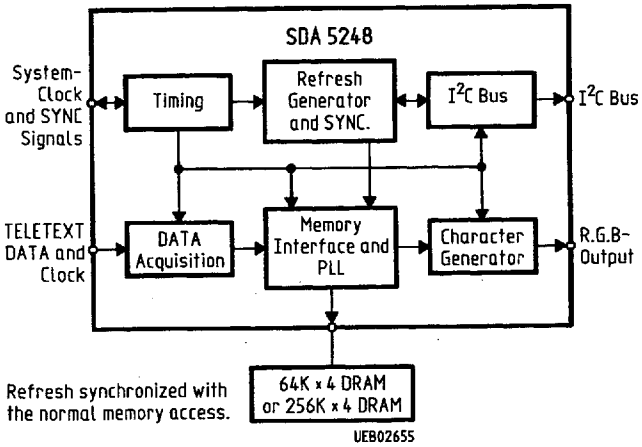
- For memory it only requires a dynamic RAM in x4 organization: 64 K x 4 dynamic RAMs can be used for 32 teletext pages or 256 K x 4 for 128 pages. The control signals of the memory interface are all derived from the 24-MHz timing, which is generated by an internal PLL. The extra external circuitry necessary for this consists of an RC filter and the wiring of the analog power supply.
- There is no longer firm assignment of memory address and search circuit in SDA 5248. Each of the four search circuits, independently of one another, can be assigned one of 128 memory addresses. This makes management of the pages that have already been found very much more flexible. There is no waiting for the reception of four complete teletext pages an the reprogramming of the memory-bank selection, which is only then possible, and the selection of four new teletext pages, as is the case with SDA 5243. As soon as a complete teletext page has been received, a new memory area can be selected for the search circuit and a new teletext page programmed. In this way 128 pages can be read in more efficiently or part of the sent teletext pages stored faster. There are substantial advantages here, especially for use in TOP. Sufficient block, group and information pages can be found and loaded faster. So this does away with the long waiting times until the TV viewer sees the teletext pages.
- Two switching outputs, programmable on the I^2C bus, can be used to control external functions.

The Teletext Processor SDA 5248 contains six function blocks **(see block diagram)**:

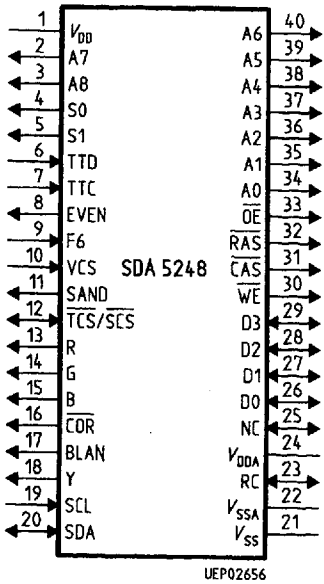
- Control with timing and system clock
- Data acquisition
- Memory interface with 24-MHz PLL
- Character generator
- I^2C bus
- Refresh generator and synchronization

Teletext data and clock signals from the data slicer SDA 5231-2 are transferred to the TTX processor SDA 5248 via pins TTD and TTC. The required data are selected in the acquisition section and stored in the external RAM via the memory interface. The data read from the RAM passes through the memory interface to the character generator, where they are transformed into corresponding R, G, B signals for the video output stages. Further output signals produced include a blanking signal BLAN, a contrast reducing signal $\overline{COR}$ and a text signal Y for an external printer. 23 registers can be written and 1 register can be written and read over the I^2C bus **(diagram 5, 6 and 7)**.

Block Diagram
Teletext Processor with DRAM Interface



Pin Configuration
(top view)



UEP02656

Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	V_{DD}	+5 V	
2	A7	RAM Address	Operation with dynamic memories with 4-bit organization
3	A8	RAM Address	When connection of 256 Kx4
4	SO	Switching Signal	Free programming switching signal
5	S1	Switching Signal	Free programming switching signal
6	TTD	Teletext Data	From data slicer SDA 5231
7	TTC	Teletext Clock	6.9375 MHz from data slicer SDA 5231
8	EVEN	EVEN Field	Field recognition output
9	F6	System Clock	6-MHz from data slicer SDA 5231
10	VCS	Composite Sync	Sliced sync signal, part of the CVBS signal, coming from the data slicer SDA 5231.
11	SAND	SANDCASTLE	Three-level signal for SDA 5231 for synchronization of F6.
12	$\overline{TCS}/\overline{SCS}$	Sync Input/Output	Synchronization output during text reproduction.
13, 14, 15	RGB	Red, Green, Blue	Open drain video output signal for TV output stages.
16	$\overline{COR}$	Contrast Reduction	Open drain video output signal for contrast reduction.
17	BLAN	Blanking	Blanking signal open drain output
18	Y	Character Output	Open drain video output signal for black/white
19	SCL	Serial Clock	I^2C bus clock input
20	SDA	Serial Data	Bidirectional I^2C bus data port (open drain stage)
21	V_{SS}	Ground Digital	
22	V_{SSA}	Ground Analog	Analog ground for PLL
23	RC	RC	RC network for PLL loop to V_{SSA}

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function	Description
24	V_{DDA}	+ 5V	Analog voltage supply for PPL
25	N.C	N.C	Output always low
26-29	D0-D3	RAM Data	Tristate bidirectional data port
30	$\overline{WE}$	Write Enable	RAM control signal (active low)
31	$\overline{RAS}$	Row Address Strobe	Control signal (active low)
32	$\overline{CAS}$	Column Address Strobe	RAM control signal (active low)
33	$\overline{OE}$	Output Enable	RAM control signal (active low)
34-40	A0-A6	RAM Address	Operation with dynamic memories with 4-bit organization.

Circuit Description

Data Acquisition

The SDA 5248 meets all the requirements of the present teletext standard.

Data arriving at the TTD pin are accepted as teletext data as soon as the start code **(diagram 1)** appears within the data entry window. All bytes are checked for odd parity errors and 1-bit errors are corrected in the bytes with Hamming protection. The parity check for the data bytes can be deselected for reception of 8-bit data without parity. The following acquisition features are available:

- Automatic data font changeover to one of 6 language by transmitted control bits, independent of the selection over the I^2C bus **(diagram 8 and 10)**.
- Data reception during lines 2 through 22 in each half frame.
- Data reception in all lines of a full frame by switching over to full channel operation. In full channel operation one must note that the automatic erase function is only partially available, hence all lines of every page must be transmitted in sequence or the whole page erased by software.
- Memory control of storage of up to 128 teletext page, 4 teletext pages are sought simultaneously and when received are transferred into the memory bank selected by the page memory pointers **(diagram 7, register 13)**.
- In the "don't care" mode pages can be sought whose page numbers are not precisely know, by inserting a don't care bit in place of the unknown number. This causes a search for all numbers between 0HEX and FHEX at the indicated location **(diagram 5, register 3)**.

- Capability of receiving supplementary information (ghost rows) which can be processed in a microcomputer. This allows reception of 24 virtual lines per page in addition to the normal text lines, and 2 Kbytes of memory are needed to store one page **(diagram 2b)**.
- The transmitted clock time is directly written into page memory selected for display.
- Automatic erasing of stored pages 0-7 for standard teletext.
- Erasure of single pages by software command.
- Rolling page number during search.

Character Generation

The character generator provides 192 alphanumeric characters and 2x64 graphics symbols in a raster comprising 12 horizontal and 10 vertical points. The various display possibilities can be selected by means of 32 control characters contained in the text **(diagrams 8-11)**.

6 language are automatically selected by the transmitted page header control bits C12, C13 and C14 (**diagram 3**, line 25, byte 7) in standardized 7-bit operation **(diagram 10 and 11)**. In addition the capability exist in 8-bit operation, to select nearly all characters independently of the control bits using the I^2C bus **(diagram 8)**.

Teletext signals R, G, B, Y, BLAN and $\overline{COR}$ are available at the open-drain outputs. The $\overline{COR}$ signal makes it possible to reduce the contrast during the mixed mode as well as inside or outside of a teletext box area. The Y signal reproduces only the teletext character plane without color information and does not have a flash function. **Diagram 12** shows the active display area.

Additional features include:

- User-controllable character-height doubling with top/bottom selection.
- Status information above or below the main text.
- Insertion of all control, graphics or alphanumeric characters in the 24 standard rows and in one extra status row is possible via the I^2C bus. By doing so the selected position of the character can be made visible by means of a cursor.

Timing

The internal system clock is derived from the 6-MHz clock F6 provided by the data slicer SDA 5231-2. The input F6 is AC coupled internally.

Vertical synchronization with the video signal occurs via the VCS input. The noise content of the VCS signal is reduced by integration. If the signal is too noisy or no synchronization can be achieved for other reasons the data acquisition is disabled. The device is able to supervise the quality of the incoming video signal at the VCS input. This is done by means of counting the sync pulses received during 64 µs. A good line of a video signal consist of 1 or 2 pulses during 64 µs. By means of an integration over the lines of move fields a good and weak signal quality is defined. Under worse signal conditions the data acquisition is stopped. The quality status bit of the VCS signal (VCSOK) is stored in the I^2C bus register 11B **(see diagram 6)**. Therefore the microprocessor can be used to supervise the signal quality level.

During the normal operation of the SDA 5248 (reg. 0, bit d3 = 0) and weak signal quality is detected the IC will automatically switch to the unlocked operation mode. This means PLL and video signal are no longer synchronized.
Is the bit d3 set to "1" there is forced synchronization even if the signal quality is weak. The data acquisition will be stopped. But if the signal quality will get weaker it has to be considered that the PLL jitter can be increased. During this operation mode bit d0 in register 11B indicates the quality of the last line received before reading the register. In the normal mode this bit indicates the quality of the VCS signal integrated during some TV fields.

One evaluation in the SDA 5248 recognizes by good signal (VCSOK = 1) the field frequency of the received VCS signal (50 Hz or 60 Hz) and the result is stored in I^2C register 11B **(see diagram 6)**.

The $\overline{TCS}/\overline{SCS}$ pin can be defined as an input via the I^2C bus. 17 µsec after the start of a line an internal signal is used to sample the input sync signal. **(Refer to diagram 13 a and 13 b)**. Therefore the input signal shall have only low distortions and low noise. The first change from "high" level to "low" level detected by this sampling process initiates the external vertical synchronization of this device **(see application circuit 3c)**.

To reduce the hardware expense for the synchronization of the display part i.e. 60-Hz signals (NTSC) the vertical external synchronization of the integrated circuit can also be done via I^2C bus through the VCS input **(see application circuit 3b)**. In this case, the bit VCS_to_SCS in I^2C register 1, bit d7 **(see diagramm 5)** must be reset to 1.
There is no requirement for an external switch-over circuit including an inversion for the SCS input. At the same time the 6-MHz clock signal F6 and due to this the internal system clock are always synchronized to the input signal. This doesn't depend on the signal quality of the input signal. Furthermore, the noise components of the sync-signals are reduced by integration.

When the $\overline{TCS}/\overline{SCS}$ pin is switched as an output it deliners a sync signal (interlaced or non-interlaced) for the TV deflection circuit **(see application circuit 3a and diagram 13a)**.

The SAND output delivers a three-level signal which contains the phase-lock signal PL and the color burst blanking signal FBB. The PL signal synchronizes the 6-MHz clock in the SDA 5231-2. If for some reasons no synchronization is possible, the PL signal component of the sand signal **(refer to timing diagram 3)** is switched off and the oscillator is running unsynchronized.

The field recognition output EVEN changes its state once per field. Using this signal it is possible to realize non-interlaced displays. The synchronization of the display can be derived from the acquisition or the display related circuits in the device (e.g. in the after hour operation mode).

The display locked synchronization mode can be selected by means of the I^2C bus bit VCS_to_SCS set to 1 (register 1, d7 = 1) or the I^2C bits "external synchronization" (register 1, d0 = d1 = 1). Otherwise the display synchronization is locked to the acquisition circuit. The line or timing relation of the EVEN output signal can be seen from **timing diagram 4**. The detector for the first field can be switched off via I^2C bus bit register 0,bit d2. The EVEN output will remain in "low" status after the detector is switch off.

Memory Interface

The following memory types can be connected to the SDA 5248 without additional external components:

- Dynamic RAMS with 64 K x 4 organization
- Dynamic RAMS with 128 K x 4 organization

The refresh for the dynamic memory occurs automatically in the range SAND = 0. The circuit configuration for the different memory types are shown in the **application circuits 1-2**.

Organization of the Page Memory

The external page memory is subdivided into 128 pages of 1 Kbyte each, which are numbered 0 through 127. The different pages 0 - 127 can be selected using the active chapter bits A0 till A7 in the I^2C bus register 8 **(diagram 6)**.
Bytes within a chapter can be selected via the I^2C bus addressing rows (I^2C bus register 9) and columns (I^2C bus register 10). Please refer to the **diagram 6**. In the functional block "memory interface" the row and column addresses are automatically converted into the 10 bit wide RAM address.
For the display chapter (A2 till A0 in register 4, **diagram 6**) and acquisition chapter (A2 till A0 in register 2, **diagram 5**) the addressing is done indirectly via the 8 page memory pointers (I^2C bus register 13, **diagram 7**).

Each CHAPTER contains 23 lines with 40 columns each for storing the normal teletext data **(diagram 2a)**. In addition it contains lines 0, 24 and 25. Line 0 is the page header. Line 24 is used to display status information from the control computer (to the user). Line 25 contains information for the control computer and 14 bytes free for optional use.

In the ghost-row mode the visible lines are stored in CHAPTER 0-3 and corresponding virtual lines in CHAPTERS 4-7. 8 pages are assigned to the chapters 0-7 by means of the 8 page memory pointers (I^2C bus register 13, **diagram 7**). **Diagram 2b** shows in which CHAPTER line a virtual line is stored.

On switch-on reset, the memory areas 0 till 7 are erased excepted for CHAPTER 0, line 0, column 7, where "alpha-white" (0000 0111) is written. During operation, erasing is possible via I^2C bus, but the erasing cycle requires up to 22 ms per page memory. As soon as the control bit C4 for one of the four pages being looked for is transmitted, this page is automatically erased. The actual state of C4 is stored in line 25 **(diagram 3)**.

For each 8-bit data word two write or read cycle are necessary. Every cycle requires 250 ns. The timing for the memory interface is given in the characteristics and in the **timing diagram 5**.

I²C Bus

Organization of the I²C Bus Registers 0010 001 R/$\overline{W}$ Component address

When the supply voltage is connected, a switch-on-reset is performed. The bus lines SDA and SCL are released. Registers 0-4 and 7-12 are set to 0000 0000, register 5 and 6 to 0000 0011. The page memory pointers in register 13 are set with the values:

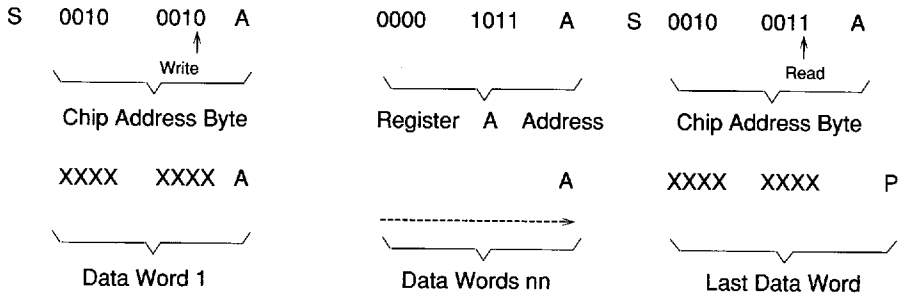
Page memory 0: 00000000
Page memory 1: 00000001
Page memory 2: 00000010
Page memory 3: 00000011
Page memory 4: 00000100
Page memory 5: 00000101
Page memory 6: 00000110
Page memory 7: 00000111

The circuit functions as slave-transmitter and slave-receiver. Registers R0 to R10, R12, R13 can be written only, register R11 can be written and read **(diagram 5 and 6)**.

Note: All reserved bits have to be written with "0".

Write

Read



In several registers, an auto-increment of the register or column address occurs after each byte is written. For example, when register 1 is addressed, the data in register 1, register 2 and the column selected by register 2 in register 3 are written, and an auto-increment of the column addresses 0-6 takes place in R3, i.e. 9 data bytes can follow directly after the register address 1.
The bits are numbered in reverse order of the I^2C bus data stream.

Register 0 Register Address 0000 0000 "Pin Function Switch"

Bit	Function	Comment
d7-d6		reserved
d5	0 = S0-pin = low 1 = S0-pin = high	
d6	0 = S0-pin = low 1 = S0-pin = high	
d3	0 = normal operation 1 = forced sync (free run mode blocked)	no automatic self sync by inferior VCS signal
d2	0 = EVEN-pin active 1 = EVEN-pin = 0V	
d1		not used
d0	0 = register 11 A is selected 1 = register 11 B is selected	

After a write to register 0 the register address is auto-incremented to 1

Register 1 Register Address 0000 0001 "Setting the Operational Mode"

Bit	Function	Comment
d7	0 = normal operation 1 = VCS T0 SCS	for 60-Hz display mode
d6	0 = acquisition of 7 bit and parity bit 1 = acquisition of 8 bit data words	parity check of TTX data no parity check
d5	0 = acquisition ON 1 = acquisition OFF	
d4	1 = enable GHOST ROWS	reception of lines 25 to 30
d3	0 = DEW 2-22, 1 = full channel operation	DEW = data entry window for line 2-22
d2	1 = TCS ON	$\overline{\text{TCS}}/\overline{\text{SCS}}$ pin is sync output
d1/d0	00 = 312/313 lines - MIX - mode	with interlace
d1/d0	01 = 312/313 lines - TEXT - mode	without interlace } is inhibit in flash
d1/d0	10 = 312/313 lines - TERMINAL - mode	without interlace } messages and subtitles
d1/d0	11 = external synchronization	$\overline{\text{TCS}}/\overline{\text{SCS}}$ pin is an input.

After a write to register 1 the register address is auto-incremented to 2

Register 2 Register Address 0000 0010 "Page Memory Selection"

Bit	Function	Comment
d7		Not used
d6	0 = page memory pointer 0-3 1 = page memory pointer 4-7	BANK selection
d5/d4	00 = page acquisition control ACQCCT0 page memory pointer 0 or 4	Register 3 selection, ACQCCT0, the acquired page is stored under the page memory address in register 13 page memory pointer 0 or 4.
d5/d4	01 = page acquisition control ACQCCT1 page memory pointer 1 or 5	Register 3 selection, ACQCCT1, the acquired page is stored under the page memory address in register 13 page memory pointer 1 or 5.
d5/d4	10 = page acquisition control ACQCCT2 page memory pointer 2 or 6	Register 3 selection, ACQCCT2, the acquired page is stored under the page memory address in register 13 page memory pointer 2 or 6.
d5/d4	11 = page acquisition control ACQCCT3 page memory pointer 3 or 7	Register 3 selection, ACQCCT3, the acquired page is stored under the page memory address in register 13 page memory pointer 3 or 7.
d3	1 = TB 0 = normal operation	Test bit.
d2-d0	addressing of column 0-6 in register 3	With address auto-increment

After a write in register 2 the register address is increased to 3

Register 3 Register Address 0000 0011 "Page Request Data"

This register contains 7 columns. The column address last written to register 2 is accessed. After every data word the column address in register 2 is auto-incremented.

Column Address 000 to 110

Bit d5-d7 are not evaluated

Column Address	Bit d4	Bit d3	Bit d2	Bit d1/d0
	1 = do care			
000	→ magazine number	$\overline{\text{HOLD}}$ (*)	← magazine number	→
001	→ tens position	←	page number tens position	→
010	→ units position	←	page number units	→
011	→ tens position	0	0	← hour tens →
100	→ units position	←	hour units	→
101	→ tens position	0	← minute tens	→
110	→ units position	←	minute tens	→

(*) $\overline{\text{HOLD}}$ = 0 Page contents are not updated
During an uninterrupted access to register 3 the HOLD function is automatically performed

Each page data acquisition controller ACQCCT0-3 contain one register 3 **(diagram 5)**. By searching the same page in several registers 3, the page data acquisition with the lowest number has the priority.

No auto-increment to register address 4.

Register 4 Register Address 0000 0100 "Display Chapter"

Register address must be transmitted (no auto-increment from register 3).

Bits 3-7 are not evaluated.

Bits 0-2 number of the page pointer 0 to 7 in register 13. The page memory pointer refer to the address of the page to be shown.

After a write to register 4 the register address is auto-incremented to 5.

Register 5 Register Address 0000 0101 "Display Control Normal Inside and Outside Box"

Bit	Function	Comment
d7	0 = only for foreground colors outside 1 = foreground and background colors outside	has priority over "picture outside"
d6	0 = only foreground colors inside 1 = foreground and background colors inside	has priority over "picture inside"
d5	0 = normal contrast 1 = contrast reduction outside	
d4	1 = contrast reduction inside	
d3	1 = text outside	
d2	1 = text inside	
d1	1 = picture outside	
d0	1 = picture inside	

Inside: inside a teletext box area
Outside: outside a teletext box

After a write to register 5 the register address is auto-increment to 6

Register 6 Register Address 0000 0110 "Display Control News Flash Subtitle"

Function analogous to register 5, valid only for flash messages and subtitles controlled by transmitted control bit C5 or C6.

Functions control as in register 5.

After a write to register 6 the register address is auto-incremented to 7.

Register 7 Register Address 0000 0111 "Display Mode"

Bit	Function	Comment
d7	1 = status information in row 0 0 = status information in row 24	
d6	1 = cursor "ON" for position addressed in reg. 9 and 10 0 = cursor "OFF"	cursor blinking is possible by repeated switching ON and OFF
d5	0 = reveal function activated	after conceal display controller character
d4/d3	01 = double character height, only lines 0-11 visible 11 = double character height only lines 12-23 visible X0 = normal image	
d2	1 = box on attribute enable in line 24	
d1	1 = box on attribute enable in line 1-23	a0 in d1 inhibits the display of flash messages and subtitle
d0	1 = box on attribute enable in line 0	

No auto-increment to register 8

Register 8 Register Address 0000 1000 "Active Chapter"

Register address must be sent (no auto-increment from register 7)
The bits 4-7 have no function.

Bit 3-1, erasing memory contents of the addressed page. The bit is not stored. Within one frame period, the blanking code 0010 0000 is written to all memory positions of line 0, column 0 to line 25, column 23.

Bit 0-2, Bit 4-7 the page memory addressed 0...127 for I^2C bus access. All pages can be addressed directly.

After a write to register 8 the register address is auto-incremented to 9.

Register 9 Register Address 0000 1001 "Active Row"

Bit 5-7 without function

Bit 0-4 selection of rows 0-25 in page memory.

Auto-increment of row address. Row 23 is followed by row 0.
Rows 24 a. 25 can only be selected directly.

After a write to register 9 the register address is auto-incremented to 10.

Register 10 Register Address 0000 1010 "Active Column"

Bit d6 and d7 without function

Bit d0-d5 selection of columns 0-39 in page memory

An auto-increment of the column address follows. Column 39 followed by column 0 and an auto-increment of the line address in register 9.

After a write to register 10 the register address is auto-incremented to 11.

Register 11A Register Address 0000 1011 and Register 0, d0 = 0
"Active Data"

Data Bit	**d7**	**d6**	**d5**	**d4**	**d3**	**d2**	**d1**	**d0**
Alphanumeric and control characters	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1

After writing a data byte, the column address is auto-incremented for the next data byte. After reading a data byte the position of the next byte to be read is automatically selected, if the last write command selected automatical the register 11 or if the last write command created an auto-increment from register 10 to register 11.

Register 11B Register Address 0000 1011 and Register 0, d0 = 1
"Status Register"

Bit	Function	Comment
d7	0 = 50-Hz VCS signal available 1 = 60-Hz VCS signal available	valid only for "VCS is OK." for d0 = 0 no used (d7 always 0)
d6-d1 d0	0 0 = VCS signal is interfered 1 = VCS is ok	register 0, d3=0
	0 = last VCS line was interfered 1 = last VCS line was interfered	register 0, d3 = 1

Write access to register 11B is impossible, if write access with the address 11B is attempted as a direct write access to the page memory by means of register 11A.
No auto-increment to register address 12.

Register 12 Register Address 0000 1100 "Address for Page Memory Pointers"

Bit d3 - d7 without function.

Bit d0 - d2 page address selection in register 13

After a write to register 12 the register address is auto-incremented to register address 13.

Register 13 Register address 0000 1101 "Page Memory Pointer"

This register contains 8 columns. The page address last written to register 12 is accessed. After writing of an address into register 13 the content of register 12 is automatically incremented. Therefore the next data byte received is automatically written into the next page memory pointer.

Bit d7 without function

Bit d0 - d6 address bit for page address

All 8 page memory pointers have to contain different addresses otherwise different acquired pages are written into the same area of the memory. After power-on reset the address pointers contain the page memory addresses 0-7.

Absolute Maximum Ratings
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	– 0.3		6	V
Voltages at: VCS, SAND, SDA, SCL, EVEN D0 to D3, A0 to A8 $\overline{OE}$, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$, S0, S1	V_{IN}	– 0.3		V_{DD}	V
TTC, F6	V_{IN}	– 0.3		11	V
$\overline{TSC/SCS}$, TTD	V_{IN}	– 0.3		8.5	V
R, G, B, BLAN, Y, $\overline{COR}$	V_A	– 0.3		6.5	V
Ambient temperature	T_A	– 20		70	°C
Storage temperature	T_{stg}	– 20		125	°C
Power dissipation	P_{tot}			1.1	W
Thermal resistance	R_{th}		39		K/W

Operating Range

Supply voltage	V_{DD}	4.5		5.5	V
Temperature	T_A	0		70	°C

Characteristics

T_A = 25°C (all voltages referenced to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.5	5	5.5	V	
	V_{DDA}	4.5	5	5.5	V	
Supply current	I_{DD}	80	130	200	mA	without load
	I_{DDA}	2	4	10	mA	F6 = 6 MHz
Inputs TTC and F6						
Input voltage*)	V_{IP}	– 0.3		10	V	min. and max. values
Input signal*)	V_{IPP}	1		7	Vpp	
Input leakage	I_I			20	µA	V_I = 0 – 10 V
Input capacitance	C_I			7	pF	
Input frequency	f_{TTC}	4	6.9375	8	MHz	
Input frequency	f_{F6}	4	6.0	8	MHz	
Rise and fall times	t_r, t_f	10		80	ns	
Input TTD						
Input signal**)	V_{IPP}	2		7	Vpp	
Input leakage	I_I			20	µA	V_I = 5.5 V
Input capacitance	C_I			7	pF	
Rise and fall times	t_r, t_f	10		80	ns	
Ext. coupling capacitor ***)	C_{ext}			50	nF	

*) timing diagram 1

**) test circuit 2, timing diagram 2

***) test circuit2

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input VCS						
L - input voltage	V_{IL}	0		0.8	V	
H - input voltage*)	V_{IH}			V_{DD}	V	
Input leakage current	I_I			10	µA	V_I = 5.5 V
Input capacitance	C_I			7	pF	
Rise and fall times	t_r, t_f			500	ns	
Input SCL, Input/Output SDA						
L - input voltage	V_{IL}	0		1.5	V	
H - input voltage	V_{IH}	3		V_{DD}	V	
Input leakage current	I_I			10	µA	V_I = 5.5 V
Input capacitance	C_I			7	pF	
Input frequency	f_{SCL}			100	kHz	
Rise and fall times	t_r, t_f			2	µs	
Max. capacity of bus	C_{max}			400	pF	
Fall time (acknowledge)	t_f			0.2	µs	from 3 to 1 V
SDA acknowledge	V_{AL}	0		0.5	V	I_{AL} = 3 mA

*) test circuit 2

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input/Output $\overline{TCS}/\overline{SCS}$						
Input signal $\overline{SCS}$ ($\overline{TSC}$ = high impedance)						
L - input voltage	V_{IL}	0		1.5	V	
H - input voltage	V_{IH}	3.5		8	V	
Input capacitance	C_I			7	pF	
Input leakage current	I_I			10	µA	V_I = 8 V
Rise and fall times	t_r, t_f			500	ns	
Output Signal $\overline{TSC}$						
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA
H - output voltage	V_{QH}	2.4		V_{DD} 5.5	V V	$-I_{QH}$ = 0.2 mA I_{QH} = 0.1 mA
Load capacitance	C_L			50	pF	
Rise and fall times	t_r, t_f			100	ns	between 0.6 and 2.2 V
RAM Data Interface D0 - D3 (Tristate input/output)						
L - input voltage	V_{IL}	0		0.8	V	
H - input voltage	V_{IH}	2		V_{DD}	V	
Input leakage current	I_I			10	µA	V_I = 5.5 V
Input capacitance	C_I			7	pF	
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA
H - output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA
Rise and fall times	t_r, t_f			20	ns	between 0.6 and 2.2 V, output active
Load capacitance	C_L			50	pF	

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output EVEN						
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA
H - output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA
Rise and fall times	t_r, t_f			100	ns	between 0.6 and 2.2 V
Load capacitance	C_L			50	pF	
Output SAND						
L - output voltage	V_{QL}	0		0.25	V	I_{QL} = 0.6 mA
Intermediate level*)	V_{QM}	1.1		2.9	V	$\pm I_{QM}$ = 30 µA
H - output voltage	V_{QH}	4.0		V_{DD}	V	$-I_{QH}$ = 30 µA
Rise time	t_{r1} t_{r2}			400 200	ns ns	between 0.4 and 1.1 V between 2.9 and 4 V
Fall time	t_f			50	ns	between 4 and 0.4 V
Load capacitance	C_L			30	pF	
RAM Address Outputs $\overline{OE}$, $\overline{WE}$, **A0 - A8,** $\overline{RAS}$, $\overline{CAS}$						
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA
H - output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA
Rise and fall times	t_r, t_f			20	ns	between 0.6 and 2.2 V
Load capacitance	C_L			50	pF	
Switch Outputs S0, S1						
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA
H - output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA
Rise and fall times	t_r, t_f			50	ns	between 0.6 and 2.2 V
Load capacitance	C_L			120	pF	

*) timing diagram 3

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs R, G, B, BLAN, Y, $\overline{COR}$ (open drain output)						
L - output voltage	V_{QL}	0 0		0.4 1	V V	I_{QL} = 2 mA I_{QL} = 5 mA
H - output voltage	V_{QH}	4.9		5	V	R_L = 1 kW an 5 V
Fall time (Test circuit 1)	t_f			20	ns	R_L = 1 kΩ by 5 V V_{PIN} = 4.5 → 1.5 V
Fall delay (Test circuit 1)	t_d			20	ns	with R_L =1 kΩ by 5 V
Output leakage	I_Q			20	µA	V_Q = 5 V
Load capacitance	C_L			25	pF	
Timing for Memory Interface						
Cycle time (page mode)**)	t_{RC}, t_{WC}	450	500	500	ns	
Delay address to $\overline{OE}$ *)	t_{OE}			10	ns	
Pulse duration $\overline{OE}$ *)	t_{OEL}	400			ns	
Row address hold hold time**)	t_{RAH}	25			ns	
Column address hold time**)	t_{CAH}	60			ns	
Row address set-up time**)	t_{ASR}	5			ns	
Column address set-up time**)	t_{ASC}	5			ns	
Data set-up time*)	t_{CAC}			60	ns	
Data hold time*)	t_{OFF}	0			ns	
Pulse duration $\overline{RAS}$ (page mode)**)	t_{RASP}	280			ns	
Pulse duration $\overline{CAS}$ **)	t_{CASL}	80			ns	
Set-up time $\overline{RAS}$ **)	t_{RP}	100			ns	

*) timing diagram 5b

**) timing diagram 5a, timing diagram 5b

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Timing for Memory Interface (cont'd) (test circuit 5a, timing diagram 5b)						
Set-up time $\overline{RAS}$ **)	t_{RP}	100			ns	
Set-up time $\overline{CAS}$ **)	t_{CP}	55			ns	
Delay $\overline{WE}$ *)	t_{WE}			10	ns	
Pulse duration $\overline{WE}$ *)	t_{WEL}	300			ns	
Data set-up time*)	t_{DS}	10			ns	
Data hold time*)	t_{DH}	60			ns	
$\overline{WE}$ to tristate*)	t_{OHZ}			40	ns	
PLL Filter Currents						
Load current	I_{CH}	20	80	200	µA	V_{OL} = 1.9 V
Load current	I_{CH}	20	80	200	µA	V_{OH} = 2.5 V
Load current	I_{DCH}	– 20	– 80	– 200	µA	V_{OL} = 1.9 V
Load current	I_{DCH}	– 20	– 80	– 200	µA	V_{OL} = 2.5 V

*) timing diagram 5a

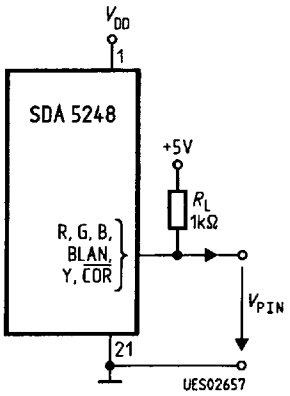
**) timing diagram 5a, timing diagram 5b

Components Used for the PLL Loop Filter (see test circuit 3)

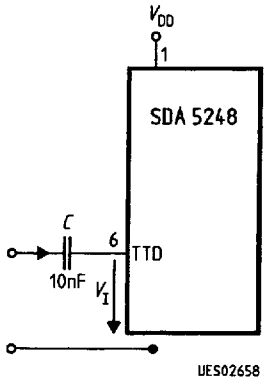
$C_{F1} \approx 1.6$ nF, $R_F \approx 1.8$ kΩ

$C_{F2} \approx 100$ pF

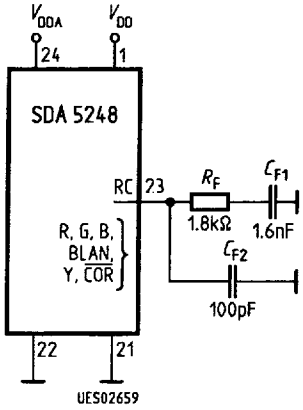
Test Circuit 1



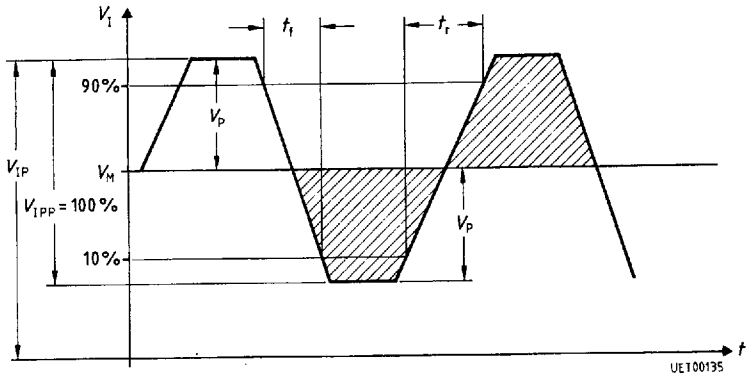
Test Circuit 2



Test Circuit 3

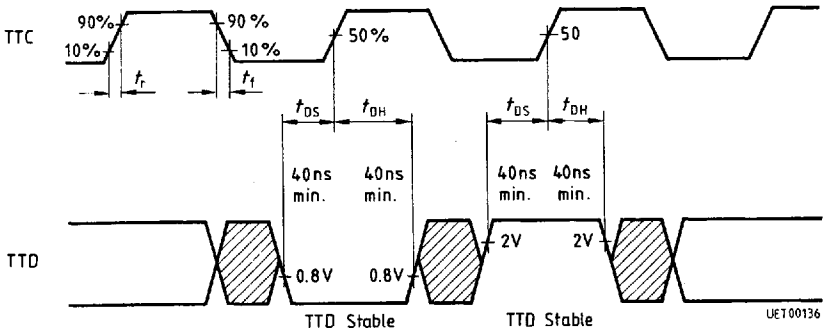


Timing Diagram 1
Input Signals TTC and F6

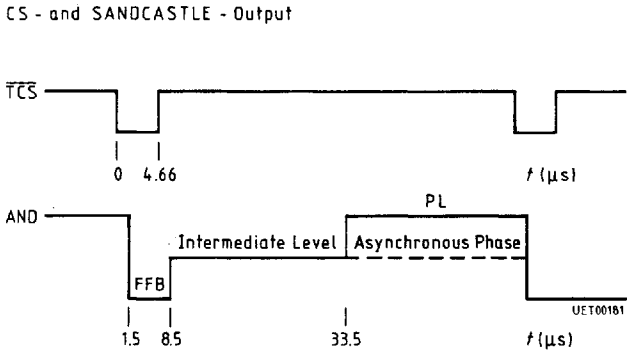


V_M = 50 % Line Giving Equal Areas

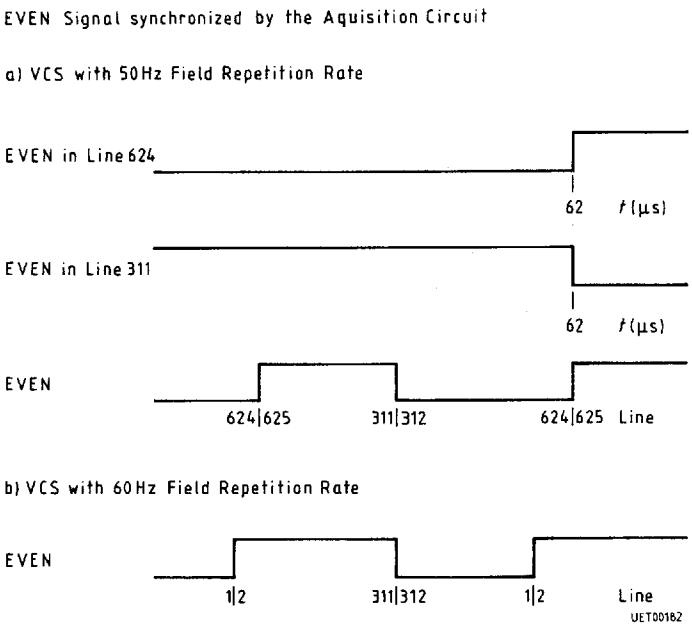
Timing Diagram 2
Input Signals TTC and TTD



Timing Diagram 3



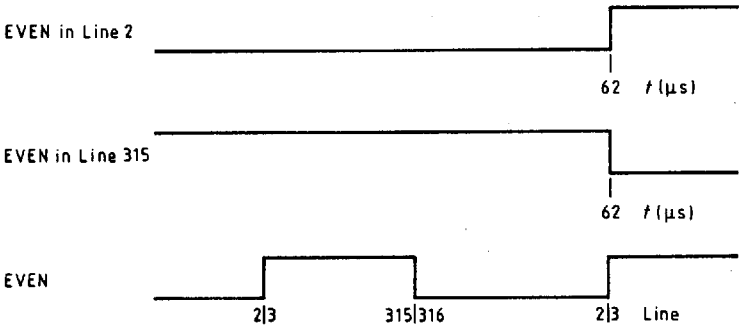
Timing Diagram 4a



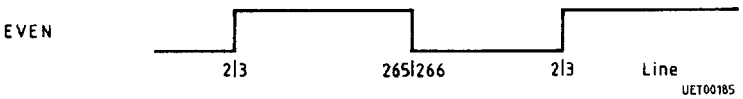
Timing Diagram 4b

EVEN Signal, synchronized by the Display Circuit:

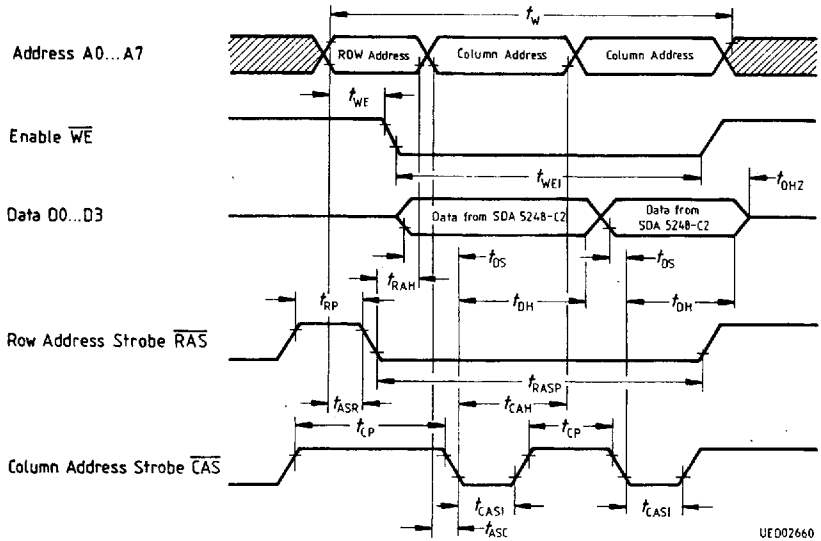
a) VCS with 50 Hz Field Repetition Rate



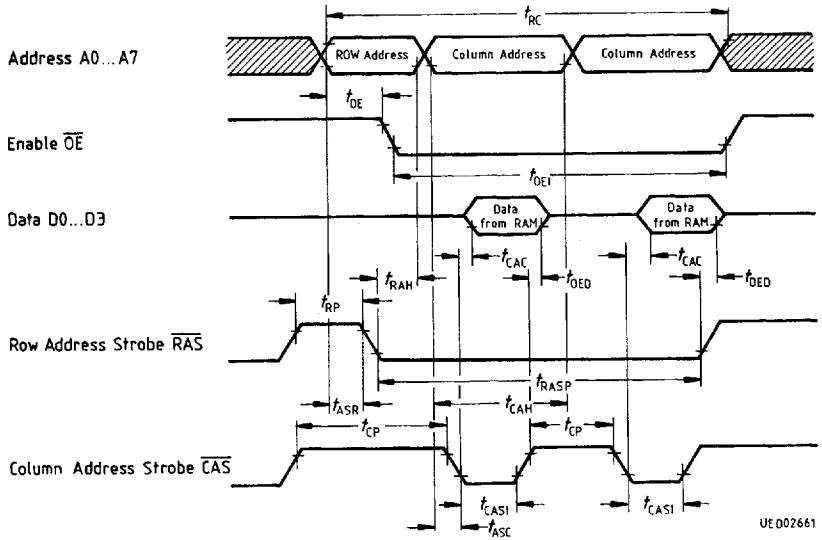
b) VCS with 60 Hz Field Repetition Rate



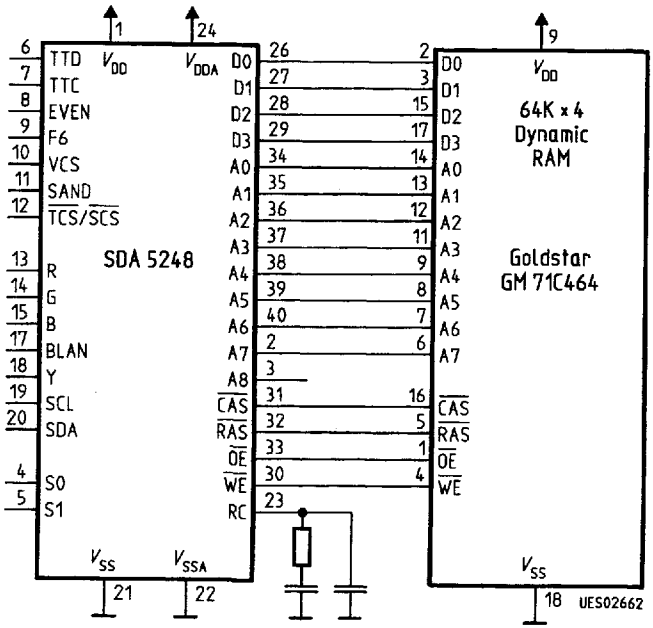
Timing Diagram 5a
Data Transfer with External Memory



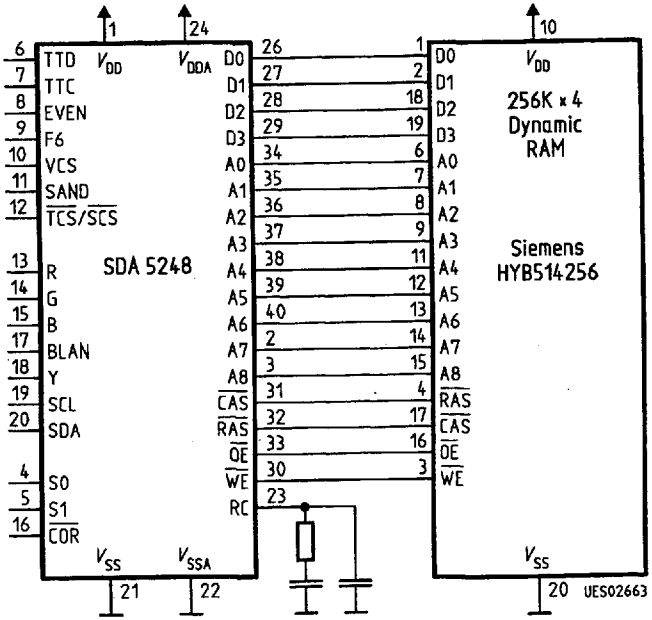
Timing Diagram 5b
Data Transfer with External Page Memory



Application Circuit 1
SDA 5248 Interfacing to 64 K x 4 Dynamic RAM for 32 Pages



Application Circuit 2
SDA 5248 Interfacing to 256 K x 4 RAM for 128 Pages



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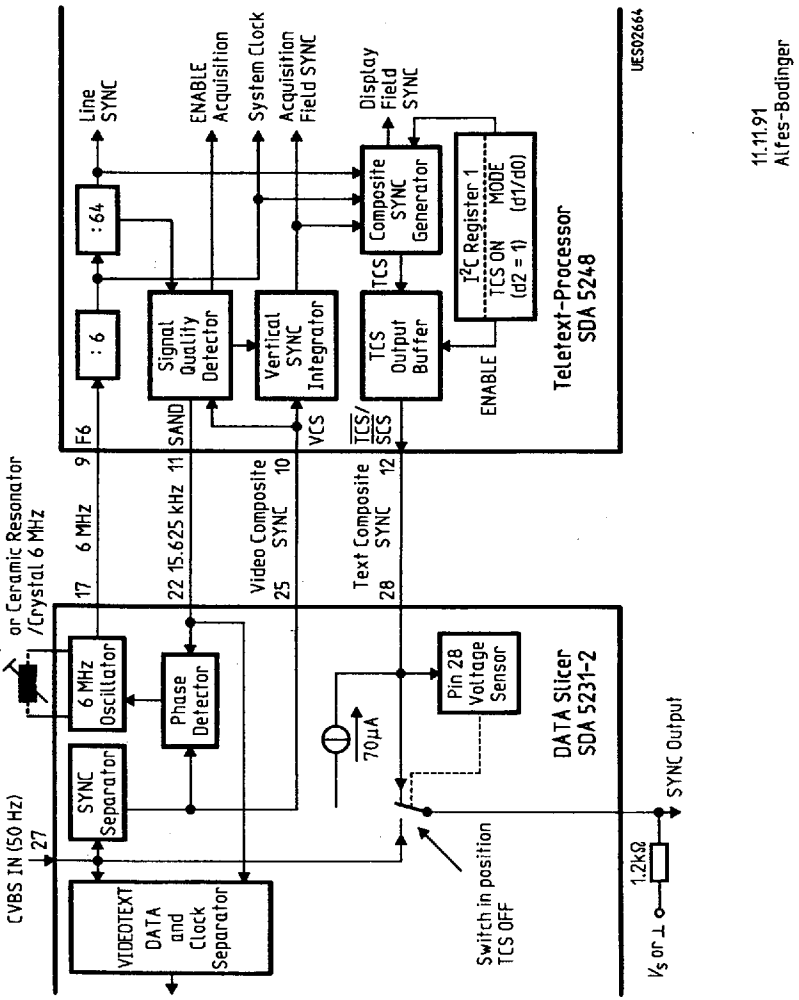
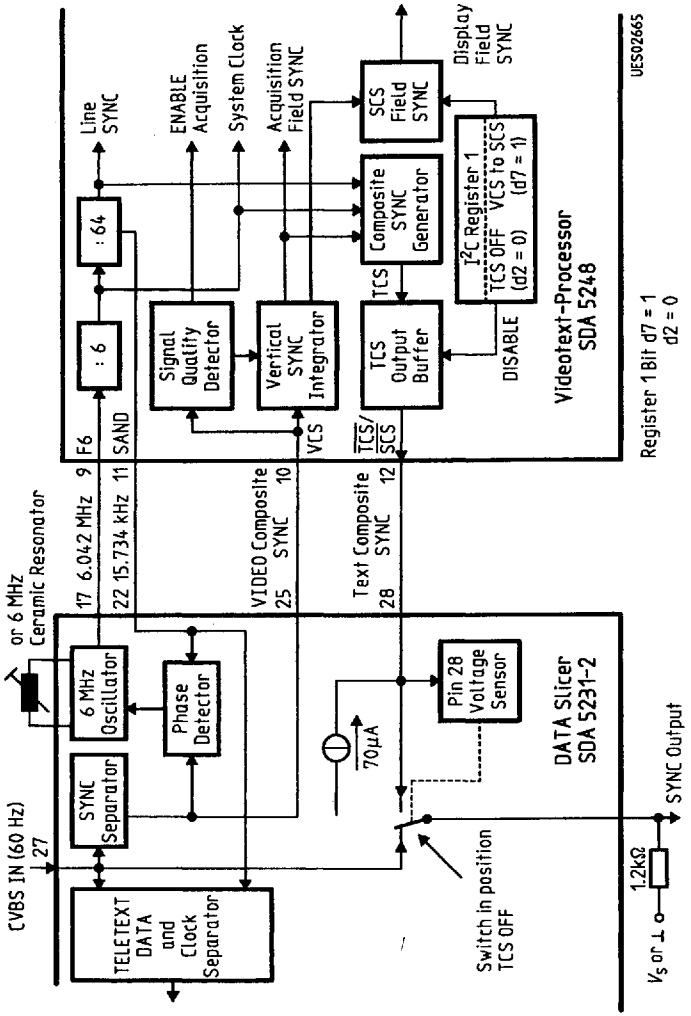
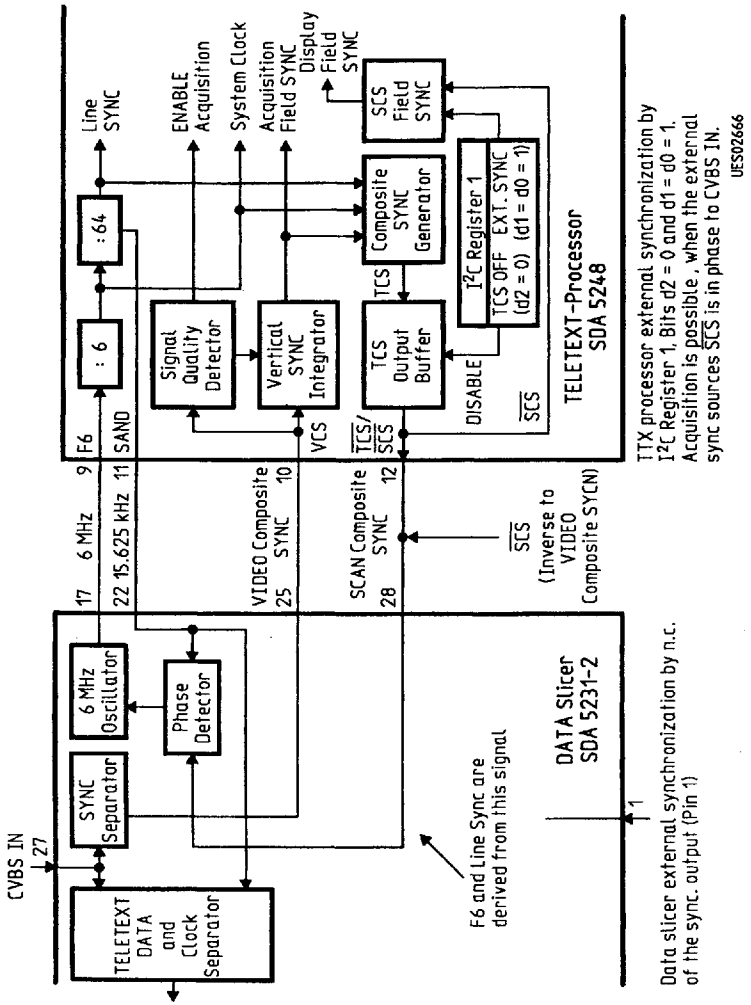
Application Circuit 3a
Teletext System Timing with CVBS Synchronization



Application Circuit 3b
Teletext Clock Control in 60-Hz Display Mode



Application Circuit 3c
Teletext Clock Control wit External Synchronization



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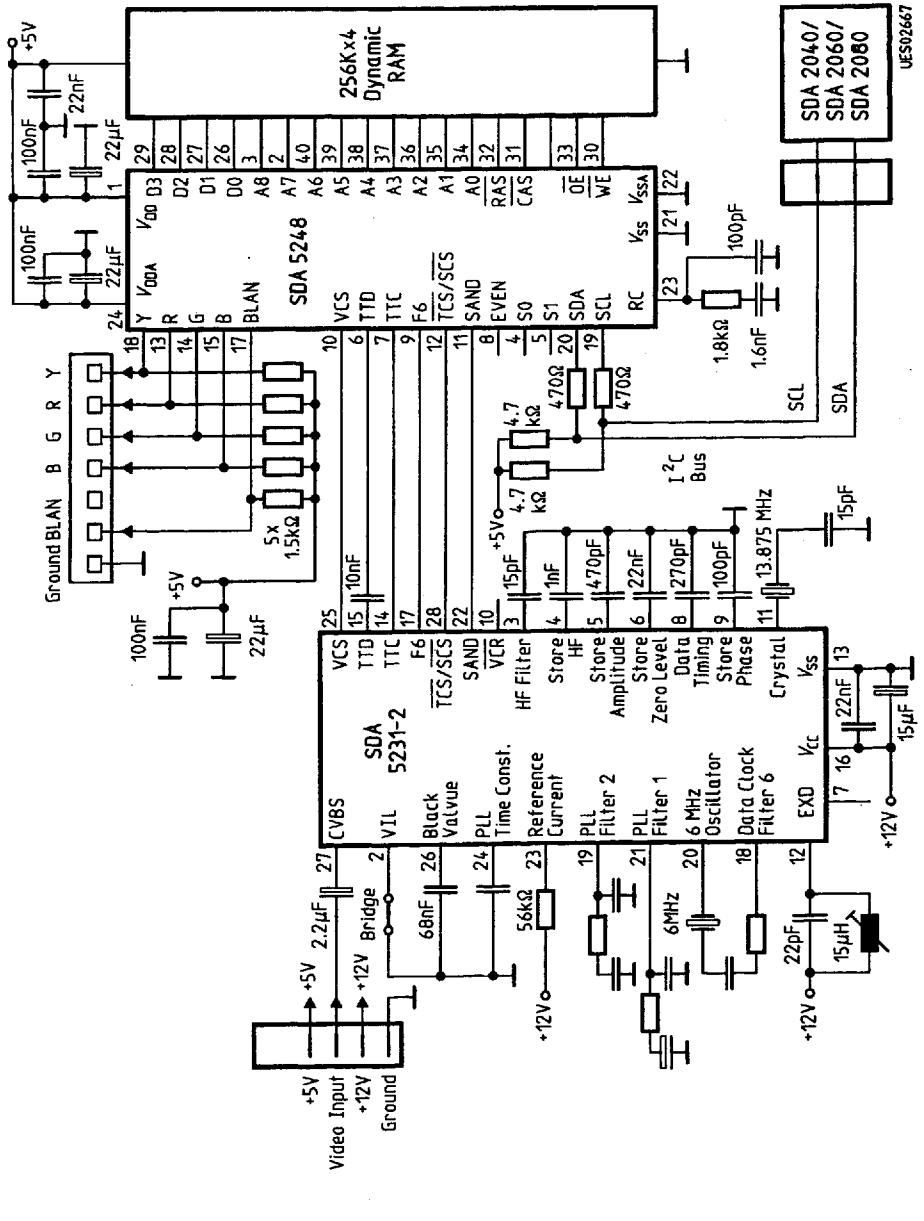
Application Circuit 4



Application Circuit 5

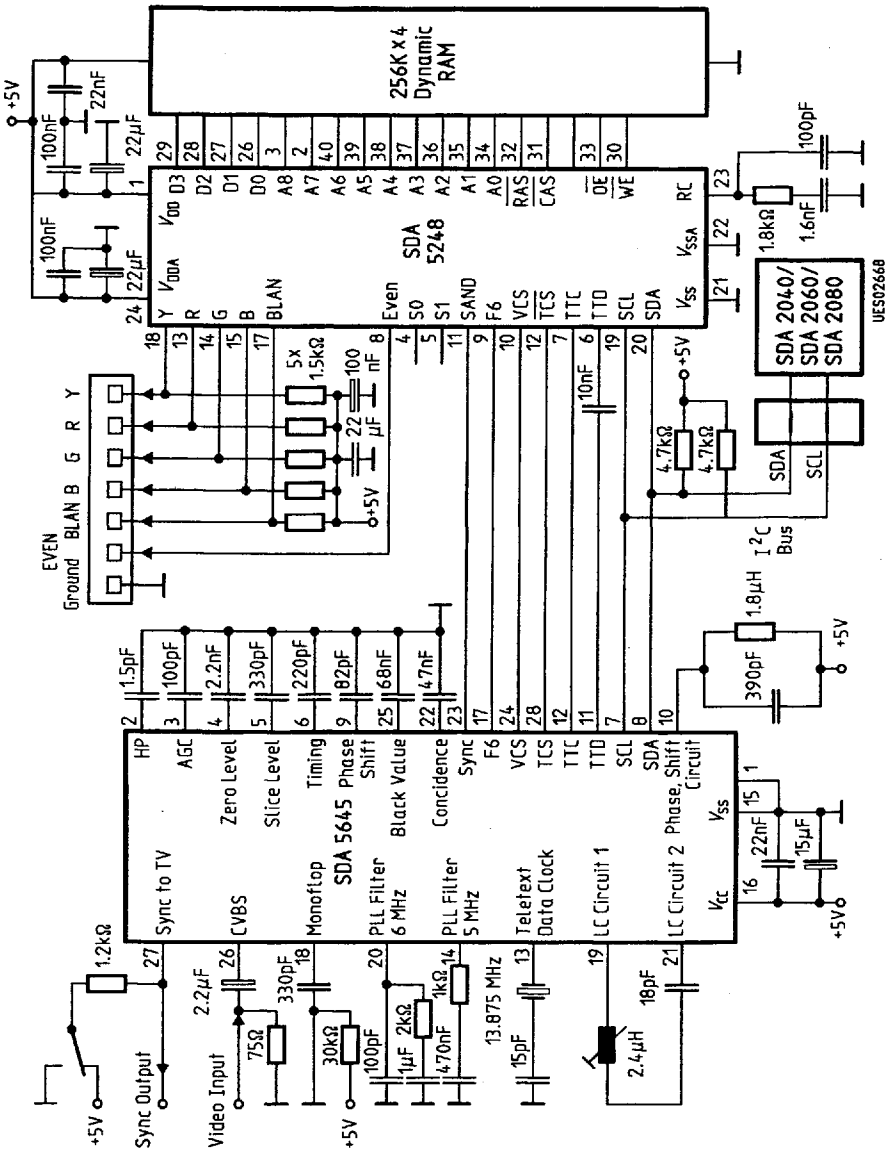


Diagram 1
Teletext Input Signal (Line 2 to 22 and 315 to 335)

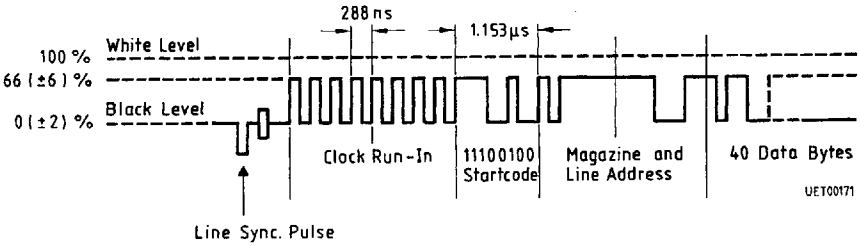


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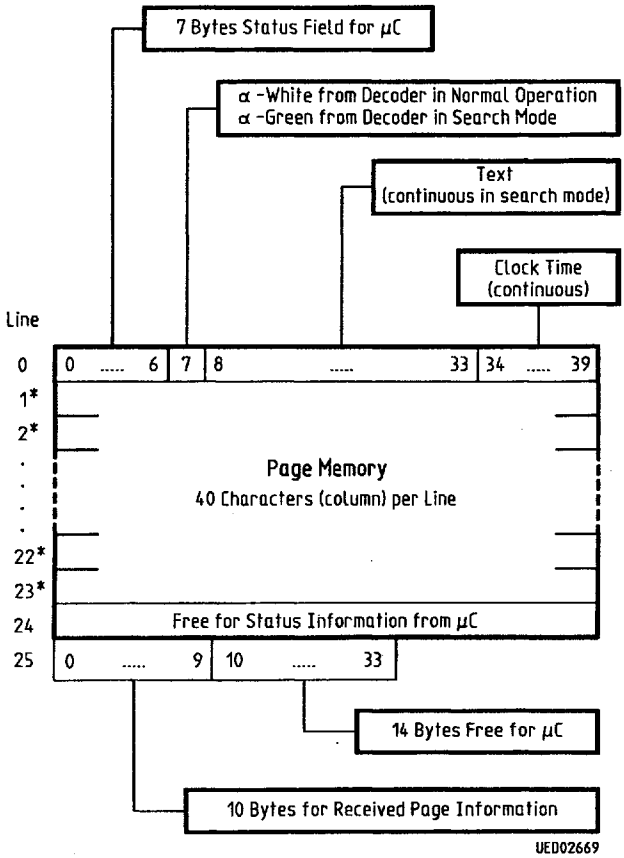
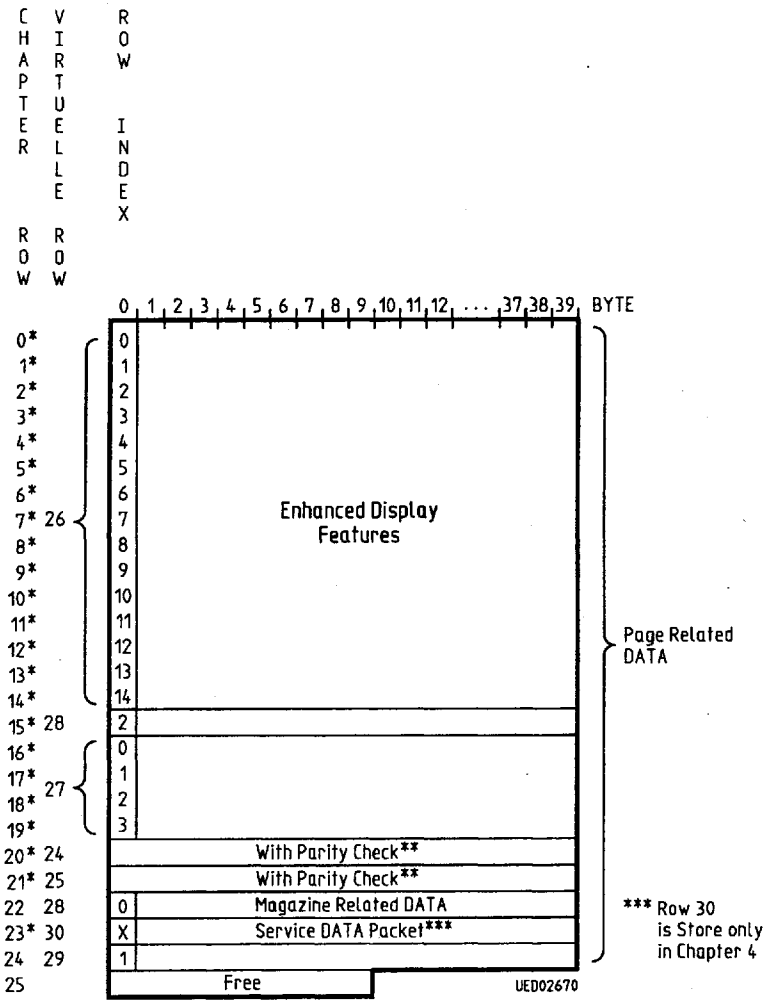
Diagram 2a
Page Memory Organization



* Automatic erasable lines with RESET, CLEAR MEMORY or control bit C4

Diagram 2b
Virtual Page (Ghost Rows)



* Automatic erasable lines with RESET, CLEAR MEMORY or control bit C4

** In 7-bit mode (register 1) the marking bytes are checked ODD parity and MSB is set to 0. Defective bytes are not tacked over in the page memory.

Diagram 3
Page Memory Organization

Line 25, Byte 0....9

Byte	Data Bits D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	HA	PU3	PU2	PU1	PU0
1	0	0	0	HA	PT3	PT2	PT1	PT0
2	0	0	0	HA	MU3	MU2	MU1	MU0
3	0	0	0	HA	C4	MT2	MT1	MT0
4	0	0	0	HA	HU3	HU2	HU1	HU0
5	0	0	0	HA	C6	C5	HT1	HT0
6	0	0	0	HA	C10	C9	C8	C7
7	0	0	0	HA	C14	C13	C12	C11
8	0	0	0	$\overline{\text{FOUND}}$	0	MAG2	MAG1	MAG0
9	0	0	PBLF	0	0	0	0	0

Information Bits

HA = High, Hamming error found in corresponding column
$\overline{\text{FOUND}}$ = Low, when a header has been found
PBLF = High, page search in progress

Page Number

MAG = Magazine number 0 to 7 (000....111)
PU = Page number units (0...9)
PT = Page number tens (0...9)
MU = Minutes units
MT = Minutes ten
HU = Hour units
HT = Hour ten

} usable as additional page sub code

Control Bits

C4 = erase page
C5 = news flash
C6 = subtitle
C7 = suppress header
C8 = update indicator
C9 = interrupted sequence
C10 = inhibit display
C11 = serial magazine sequence
C12, C13, C14 character set selection

Diagram 5
Register Configuration

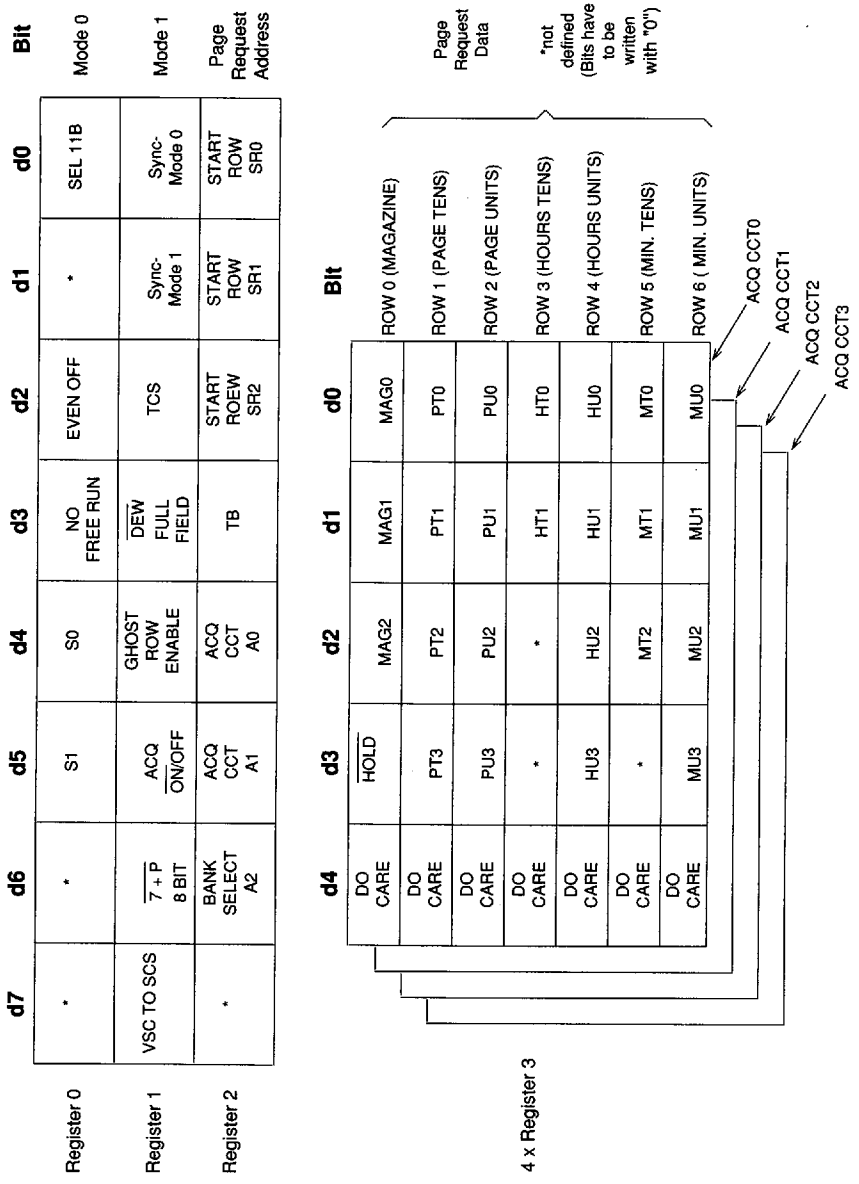


Diagram 6
Register Configuration

	d7	d6	d5	d4	d3	d2	d1	d0	Bit
Register 4	*	*	*	*	*	A2	A1	A0	DISPLAY CHAPTER
Register 5	BACK-GROUND OUT	BACK-GROUND IN	CONTRAST REDUCTION OUT	CONTRAST REDUCTION IN	TEXT OUT	TEXT IN	PICTURE OUT	PICTURE IN	DISPLAY CONTROL NORMAL INSIDE AND OUTSIDE BOX
Register 6	BACK-GROUND OUT	BACK-GROUND IN	CONTRAST REDUCTION OUT	CONTRAST REDUCTION IN	TEXT OUT	TEXT IN	PICTURE OUT	PICTURE IN	DISPLAY CONTROL NEWS FLASH OR SUBTITLE
Register 7	STATUS ROW $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL	$\overline{\text{TOP}}$ BOTTOM	$\overline{\text{SINGLE}}$ DOUBLE HEIGTH	BOX ON 24	BOX ON 1 - 23	BOX ON 0	DISPLAY MODE

RAM ACCESS REGISTER

	d7	d6	d5	d4	d3	d2	d1	d0	Bit
Register 8	A6	A5	A4	A3	CLEAR MODE	A2	A1	A0	ACTIVE CHAPTER
Register 9	*	*	*	R4	R3	R2	R1	R0	ACTIVE ROW
Register10	*	*	C5	C4	C3	C2	C1	C0	ACTIVE COLUMN
Register11A	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	ACTIVE DATA
Register11B	60 Hz	0	0	0	0	0	0	VCSOK/ LLNOR	STATUS

* not defined
(Register have to be written with "0")

Diagram 7
Register Configuration

Register 12

*	*	*	*	*	PA2	PA1	PA0

Address for Page Memory Pointers

8 x Register 13

*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 0
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 1
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 2
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 3
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 4
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 5
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 6
*	A6	A5	A4	A3	A2	A1	A0	Page Memory Pointer 7

* not defined
(Bits have to be written with "0")

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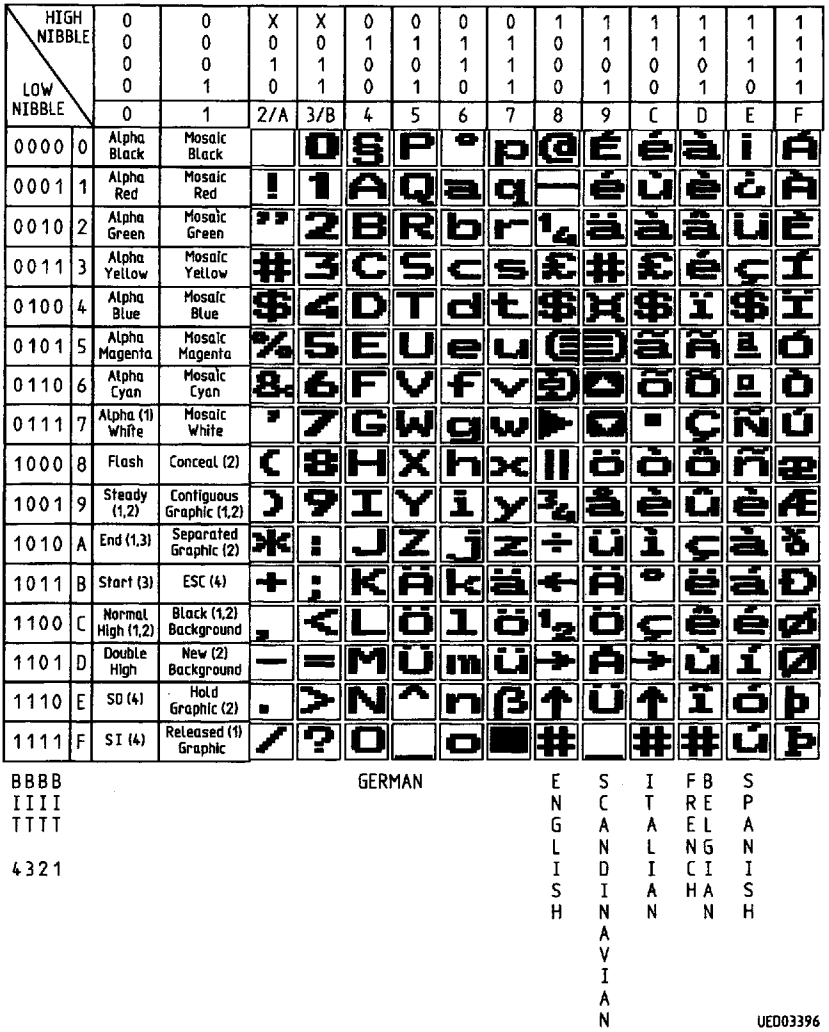
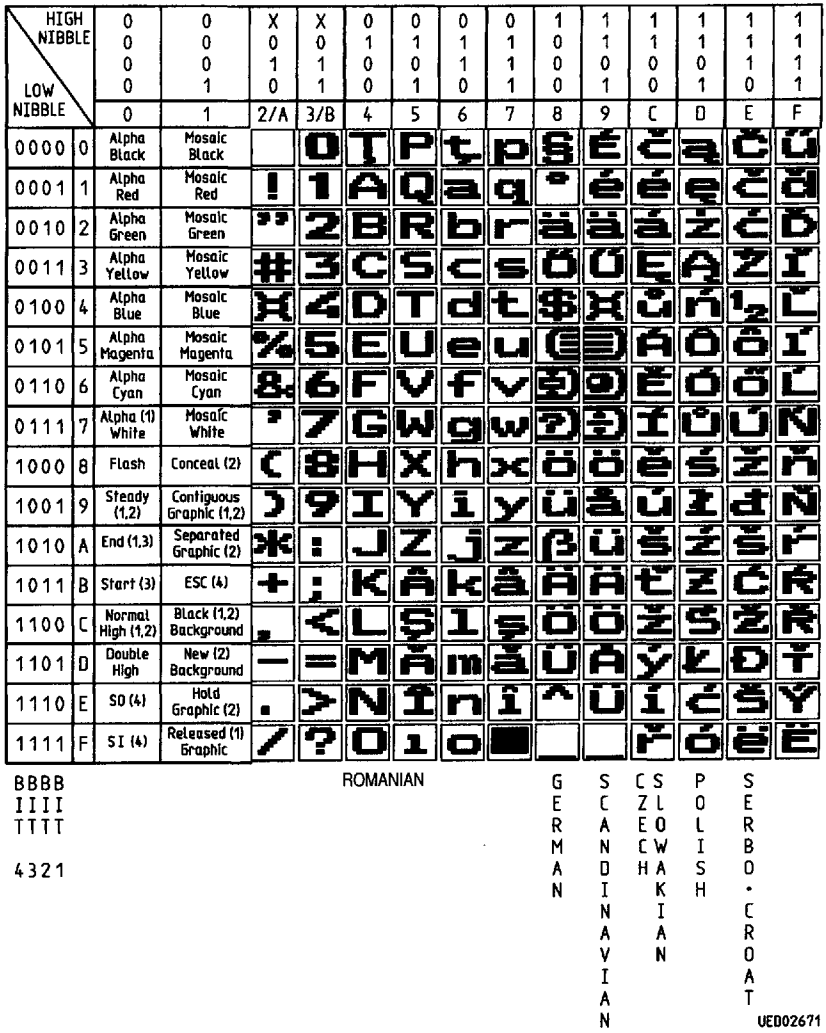
Diagram 8.1
Character Set Selection
Display of the Complete Character Set SDA 5248C1



(1) Reset before the start of each row
(2) Is implemented for the control character and not just the following characters
(3) These control characters have to be transmitted twice in succession implementation begins between control characters
(4) Not implemented

Comment: The random access to ^, β and § can be done only when the language selection bits C12, C13, C14 are adjusted to the German language.

Diagram 8.2
Character Set Selection
Display of the Complete Character Set SDA5248C2

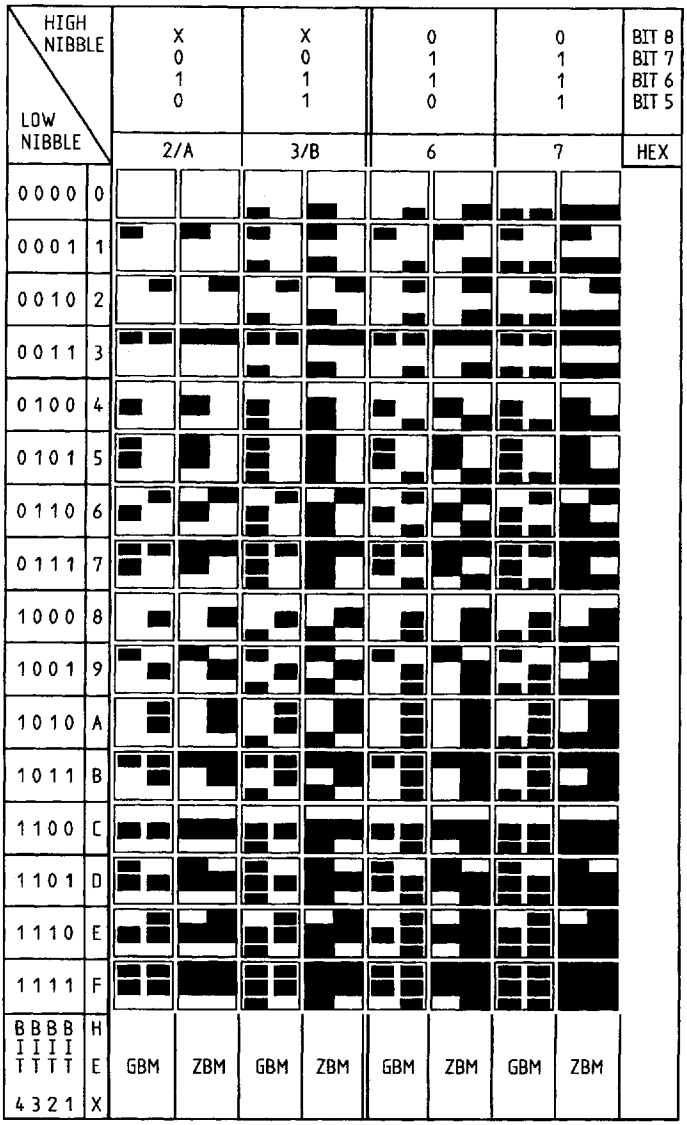


(1) Reset before the start of each row
(2) Is implemented for the control character and not just the following characters
(3) These control characters have to be transmitted twice in succession implementation begins between control characters
(4) Not implemented

Comment: The random access to ^, β and § can be done only when the language selection bits C12, C13, C14 are adjusted to the German language.

Diagram 9
Graphic Characters

Graphics mode is activated by control character (0001 0XXX).



UED02672

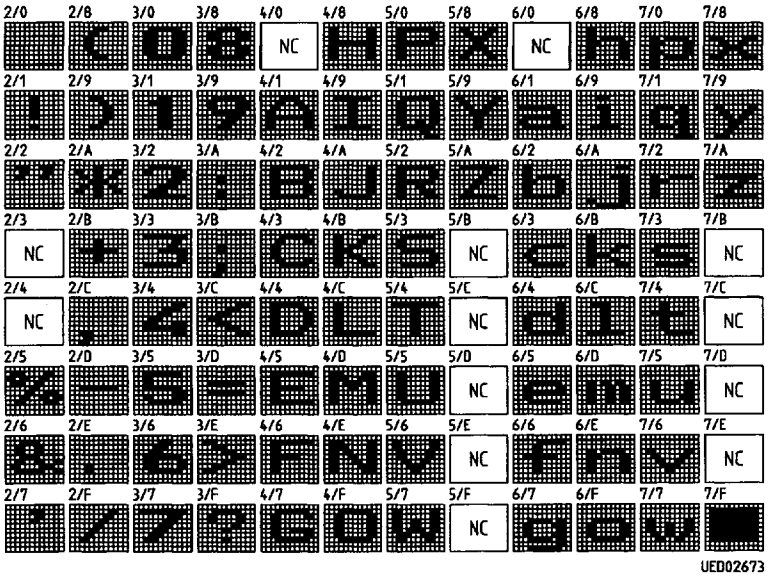
SG: Separated Graphics
CG: Contiguous Graphics

Diagram 10.1a
National Character Set Selection Using the Transmitted Control Bits

Bit 8 transmitted parity bit is reset to 0.
The national characters in **diagram 11** are implemented in the corresponding positions in **diagram 10b**.

Trans-mitter	English	German	Swedish	Italian	French	Spanish	Dynamic Character Redefinition	Reserve
Control bits								
C12	0	0	0	0	1	1	1	1
C13	0	0	1	1	0	0	1	1
C14	0	1	0	1	0	1	0	1
Siemens SDA 5248C1	English	German	Swedish	Italian	French	Spanish	English	English

Diagram 10.1b
Basic Character Set SDA 5248C1



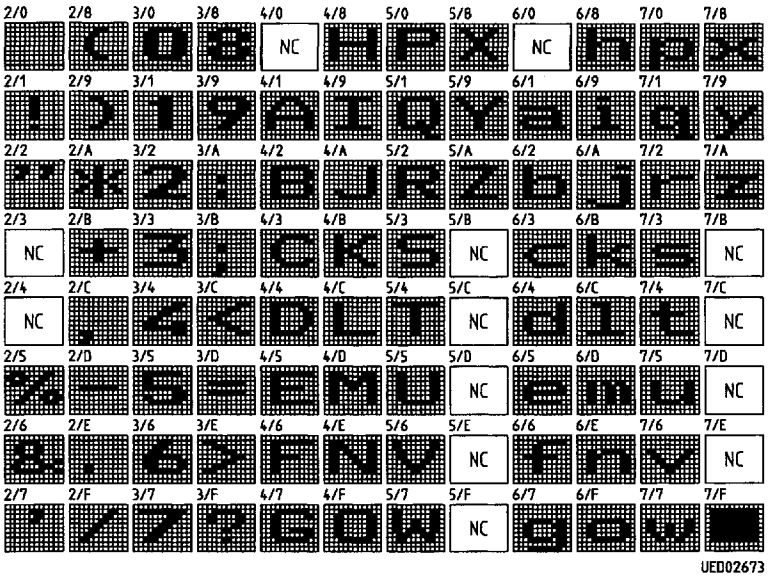
Basic character set (code: high nibble/low nibble for bit 8 = 0)
NC = National Character (**diagram 11**)

Diagram 10.2a
National Character Set Selection Using the Transmitted Control Bits

Bit 8 transmitted parity bit is reset to 0.
The national characters in **diagram 11** are implemented in the corresponding positions in **diagram 10b**.

Trans-mitter	English	German	Swedish	Italian	French	Spanish	Dynamic Character Redefinition	Reserve
Control bits								
C12	0	0	0	0	1	1	1	1
C13	0	0	1	1	0	0	1	1
C14	0	1	0	1	0	1	0	1
Siemens SDA 5248C2	Polish	German	Scandi-navian	German	German	Serbo-croat	Czech-Slovak	Romania

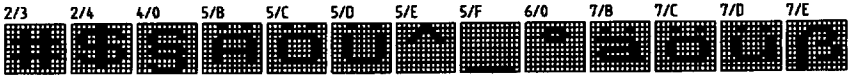
Diagram 10.2b
Basic Character Set SDA 5248C2



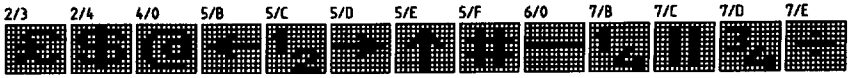
Basic character set (code: high nibble/low nibble for bit 8 = 0)
NC = National Character (**diagram 11**)

Diagram 11.1a
National Characters SDA 5248C1 (NC)

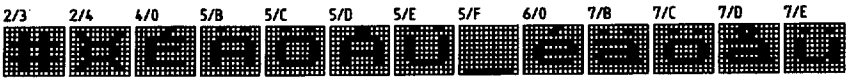
German



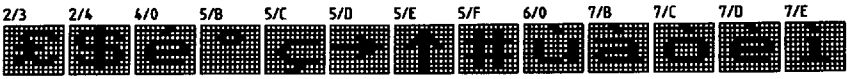
English



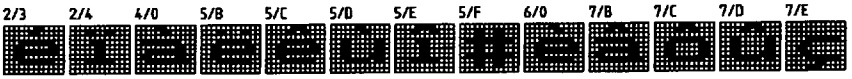
Scandinavian



Italian



French, Belgian



Spanish

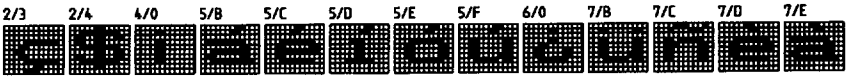


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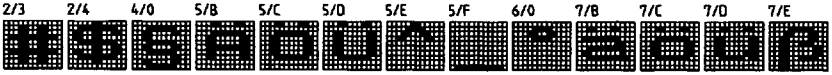
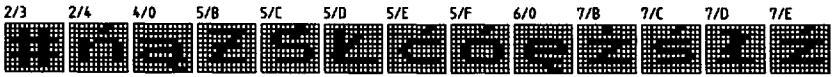
Diagram 11.2a
National Characters SDA 5248C2 (NC)

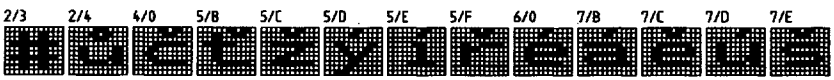
German



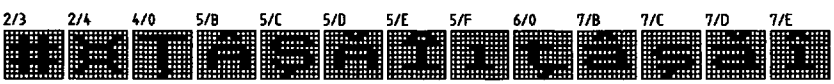
Polish



Czek-Slovak



Romanian



Scandinavian

Serbo-Croat

UED02674

Diagram 11.1b
National Characters SDA 5248C1 (NC)

Fixed special characters

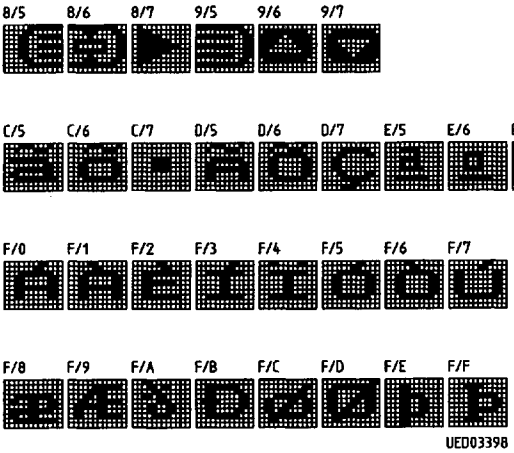


Diagram 11.2b
National Characters SDA 5248C2 (NC)

Fixed special characters

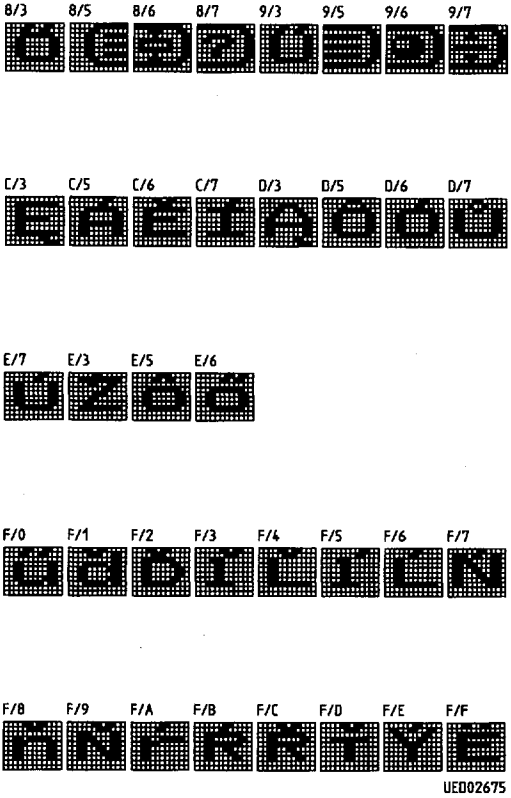
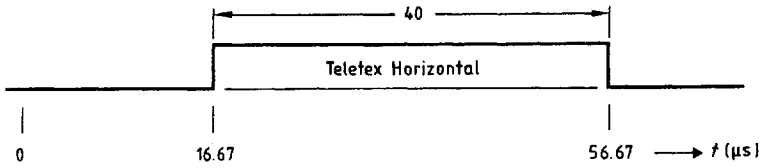


Diagram 12

Display Timing



0 is the reference in test circuit 3

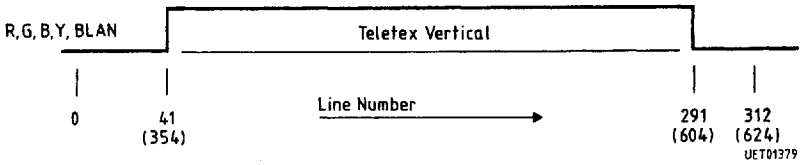


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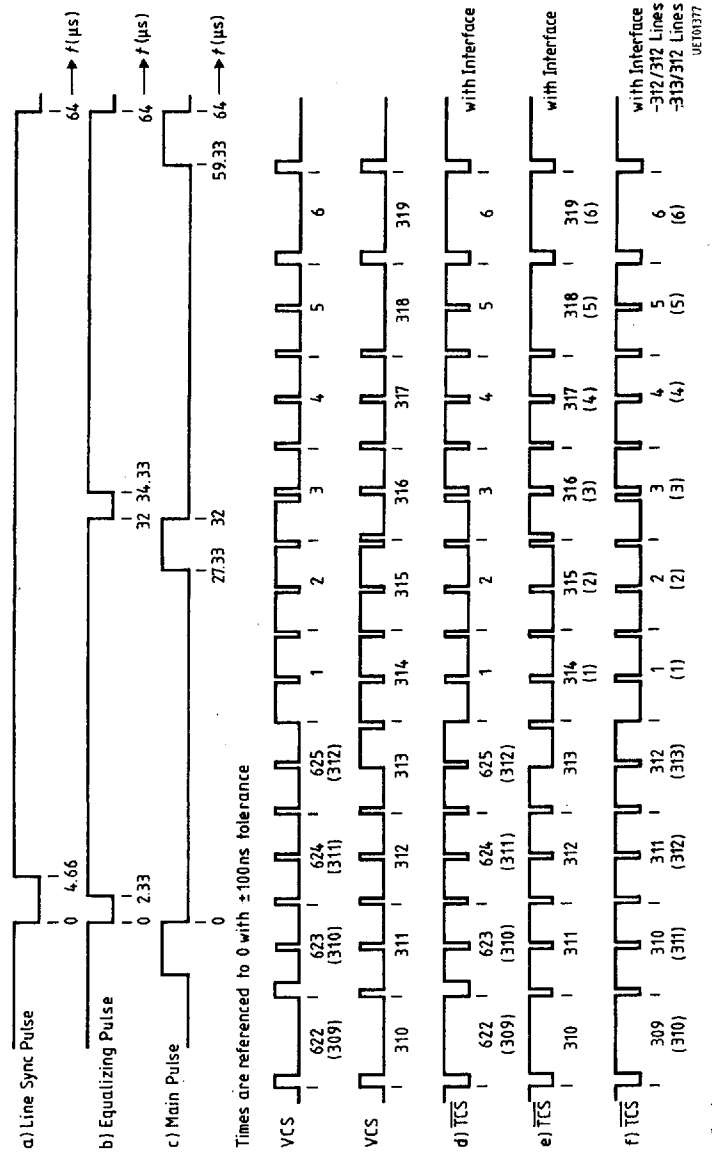
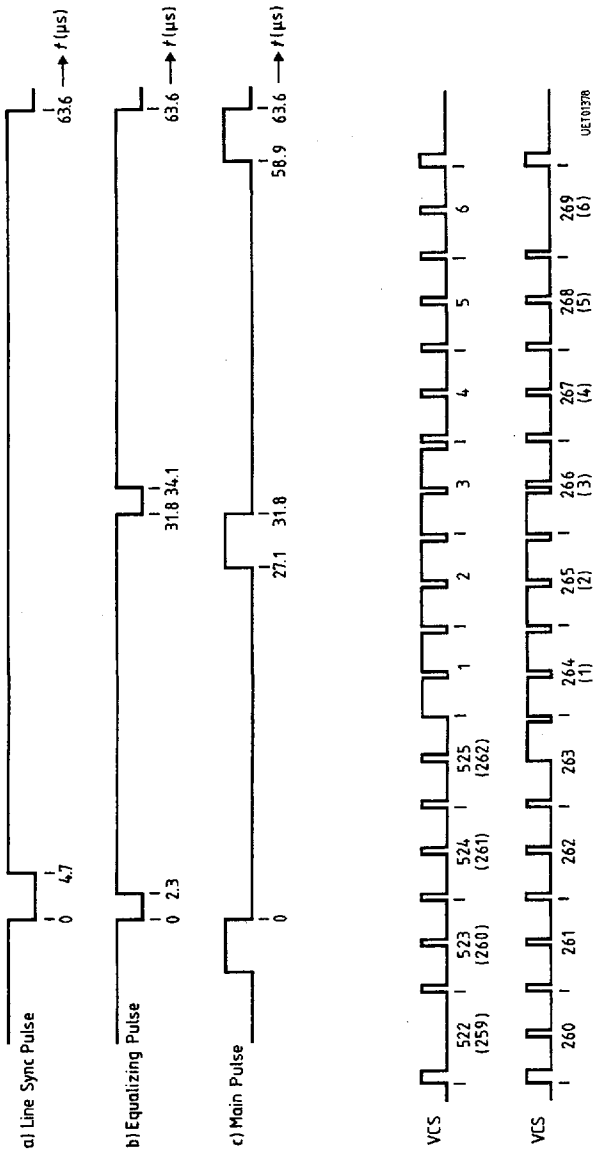
Diagram 13a
Raster Change Frequency 50 Hz



Composite sync $\overline{TCS}$ contains line sync pulse equalizing pulses and main pulses.
D, e, f are the vertical sync signals with line numbers.

Diagram 13b
Raster Change Frequency 60 Hz



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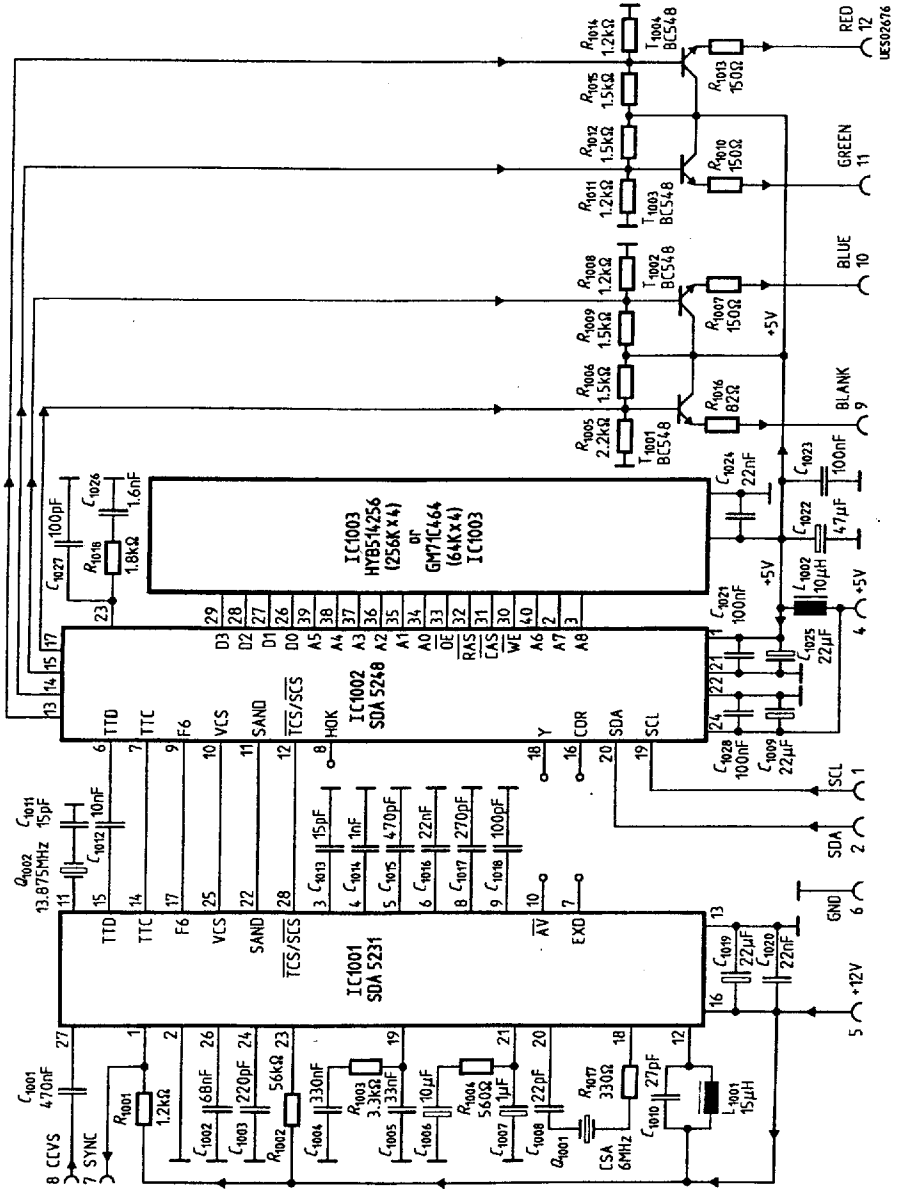
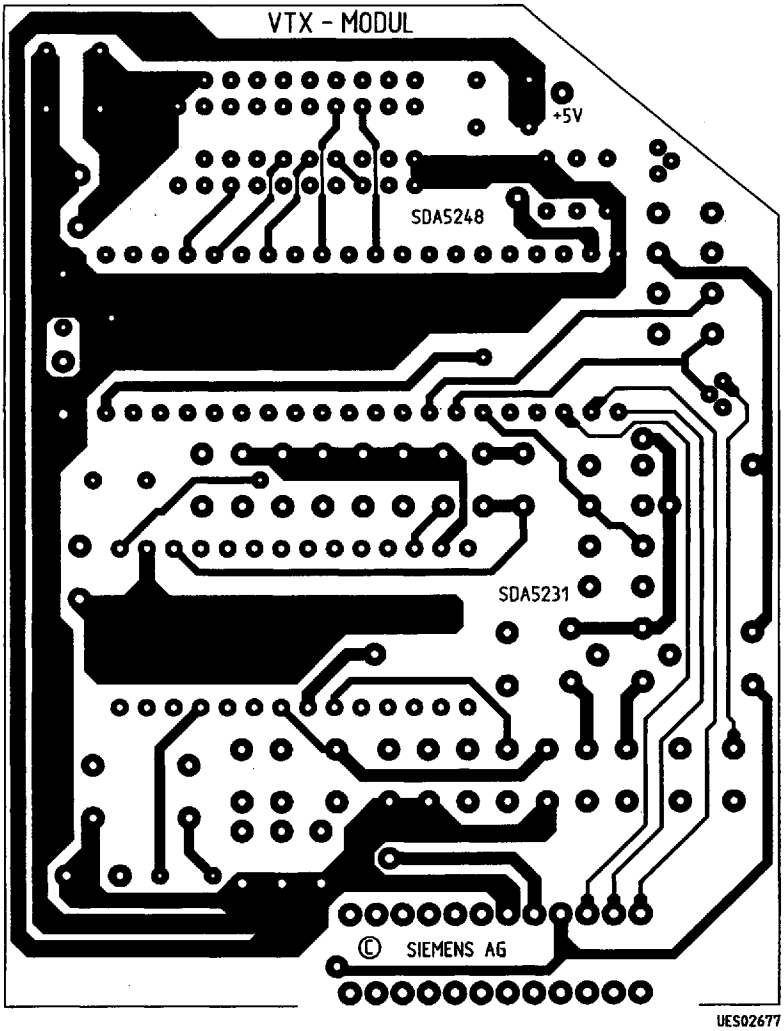
Application Circuit
VTX Modul (D-RAM Version)



Layout / Plug-In Location Plan



Plug-In Location Plan