QL3012
12,000 Usable PLD Gate pASIC®3 FPGA
Combining High Performance *and* High Density

April, 1999

pASIC 3 HIGHLIGHTS

... 12,000 usable PLD gates, 118 I/O pins

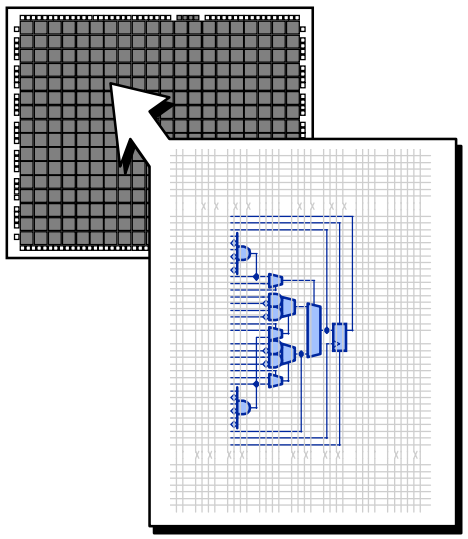
320 Logic Cells

High Performance and High Density
-12,000 Usable PLD Gates with 118 I/Os
-16-bit counter speeds over 300 MHz, data path speeds over 400 MHz
-0.35µm four-layer metal non-volatile CMOS process for smallest die sizes

Easy to Use / Fast Development Cycles
-100% routable with 100% utilization and complete pin-out stability
-Variable-grain logic cells provide high performance and 100% utilization
-Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities
-Interfaces with both 3.3 volt and 5.0 volt devices
-PCI compliant with 3.3V and 5.0V buses for -1/-2/-3/-4 speed grades
-Full JTAG boundary scan
-Registered I/O cells with individually controlled clocks and output enables

QL3012 Block Diagram



QUICKLOGIC

PRODUCT SUMMARY

The QL3012 is a 12,000 usable PLD gate member of the pASIC 3 family of FPGAs. pASIC 3 FPGAs are fabricated on a 0.35µm four-layer metal process using QuickLogic's patented ViaLink technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL3012 contains 320 logic cells. With a maximum of 118 I/Os, the QL3012 is available in 84-pin PLCC, 100-pin TQFP, and 144-pin TQFP packages.

Software support for the complete pASIC 3 family, including the QL3012, is available through three basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The QuickWorks-Lite™ and Quick*Tools*™ packages provide a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Veribest, or other third-party tools for design entry, synthesis, or simulation.

Total of 118 I/O Pins

- 110 bidirectional input/output pins, PCI-compliant for 5.0 volt and 3.3 volt buses for -1/-2/-3/-4 speed grades
- 4 high-drive input-only pins
- 4 high-drive input/distributed network pins

Four Low-Skew Distributed Networks

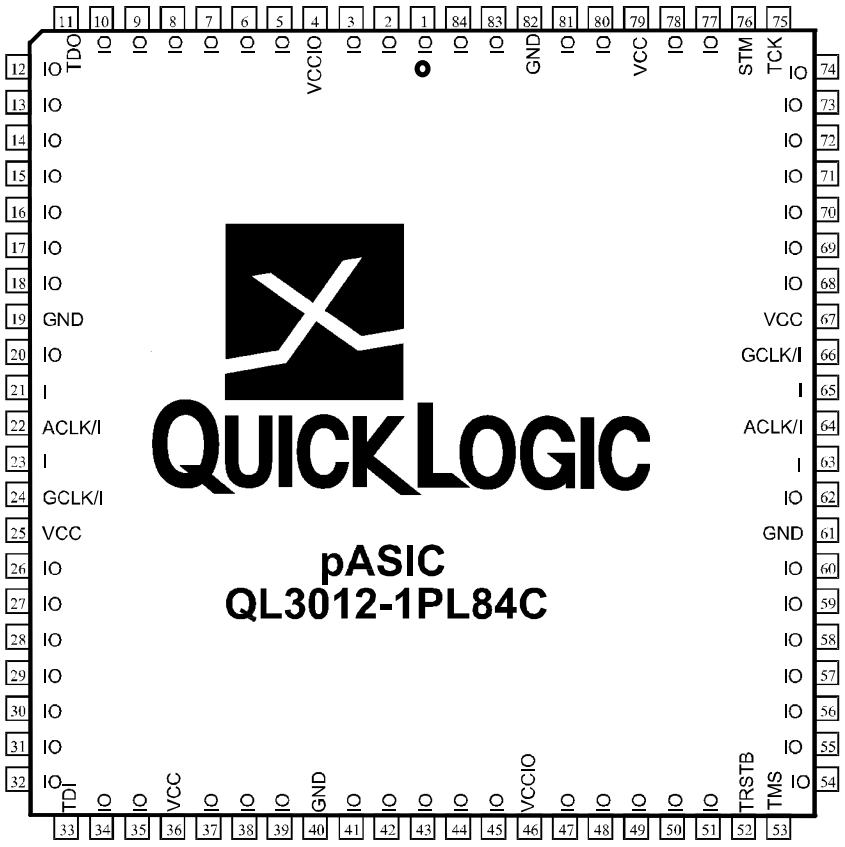
- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs - each driven by an input-only pin
- Two global clock/control networks available to the logic cell F1, clock, set and reset inputs and the input and I/O register clock, reset and enable inputs as well as the output enable control - each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance

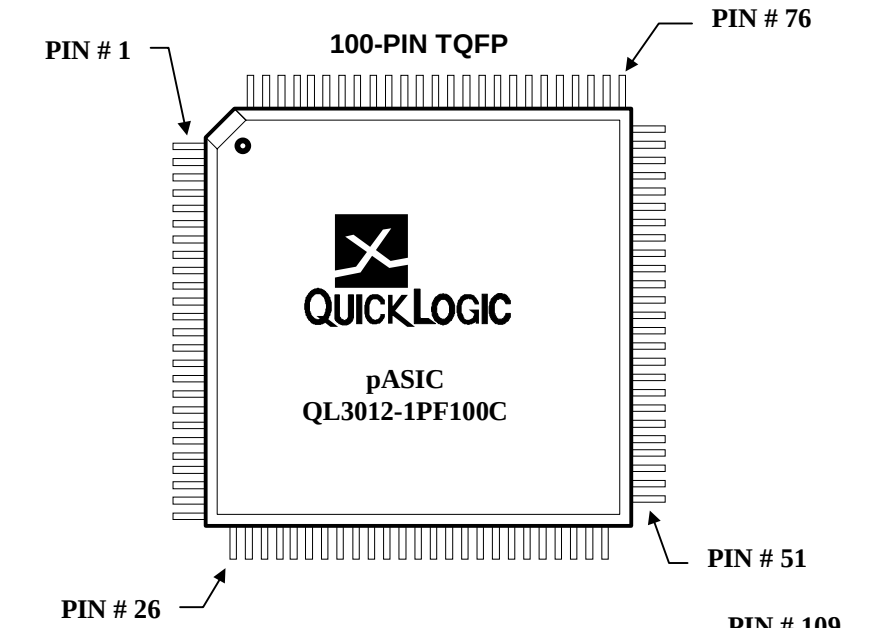
- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz

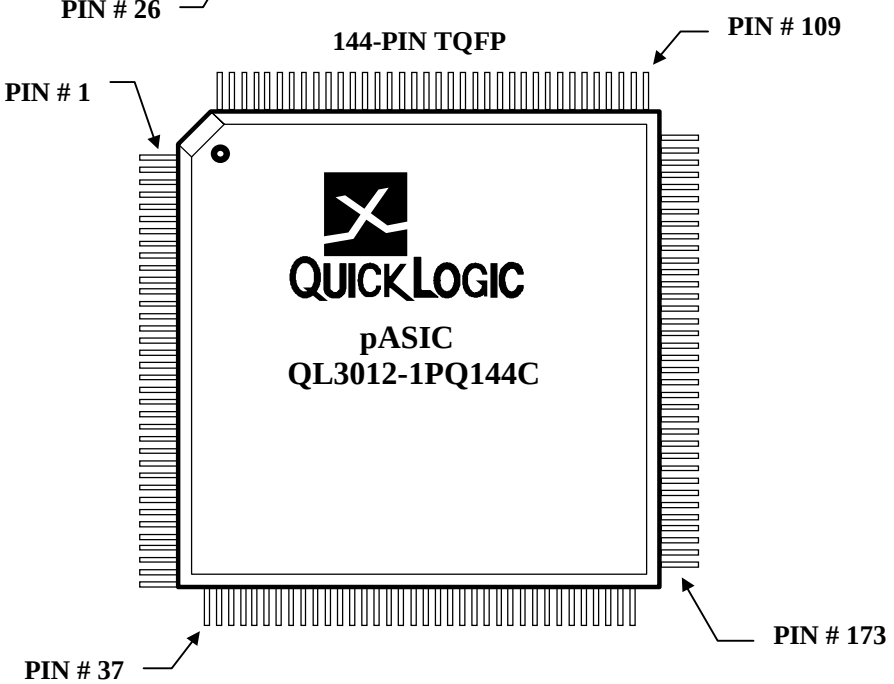
PINOUT DIAGRAM

84-PIN PLCC



PINOUT DIAGRAMS





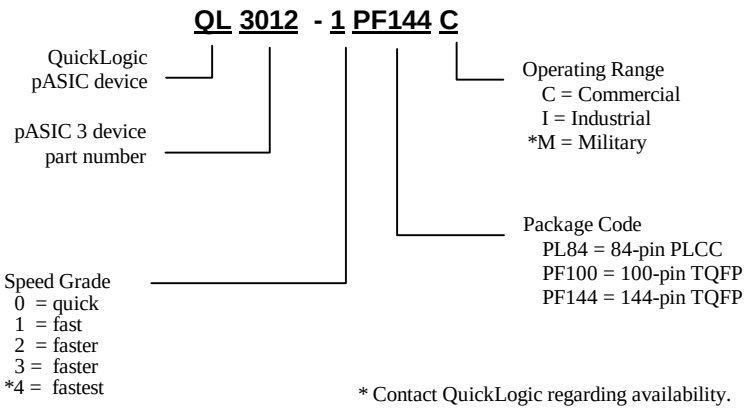
100 TQFP and 144 TQFP Pinout Table

144 TQFP	100 TQFP	Function	144 TQFP	100 TQFP	Function	144 TQFP	100 TQFP	Function	144 TQFP	100 TQFP	Function
1	2	I/O	38	26	TDI	75	53	I/O	111	78	I/O
2	3	I/O	39	27	I/O	76	54	I/O	112	79	I/O
3	NC	I/O	40	28	I/O	77	55	I/O	113	80	I/O
4	4	I/O	41	29	I/O	78	NC	I/O	114	NC	VCC
5	NC	I/O	42	NC	VCC	79	NC	VCC	115	81	I/O
6	5	I/O	43	30	I/O	80	NC	I/O	116	82	I/O
7	NC	VCC	44	31	I/O	81	56	I/O	117	83	I/O
8	6	I/O	45	NC	I/O	82	NC	I/O	118	NC	I/O
9	NC	I/O	46	32	I/O	83	57	I/O	119	84	I/O
10	7	I/O	47	33	I/O	84	NC	I/O	120	NC	I/O
11	NC	I/O	48	NC	I/O	85	58	I/O	121	NC	I/O
12	NC	I/O	49	34	I/O	86	NC	I/O	122	85	GND
13	8	I/O	50	35	GND	87	59	GND	123	NC	I/O
14	NC	I/O	51	36	I/O	88	60	I/O	124	86	I/O
15	9	GND	52	NC	I/O	89	61	I	125	87	I/O
16	10	I/O	53	37	I/O	90	62	ACLK / I	126	88	GND
17	11	I	54	38	GND	91	63	VCC	127	89	I/O
18	12	ACLK / I	55	39	I/O	92	64	I	128	90	I/O
19	13	VCC	56	40	I/O	93	65	GCLK / I	129	91	I/O
20	14	I	57	41	I/O	94	66	VCC	130	92	VCCIO
21	15	GCLK / I	58	42	VCCIO	95	67	I/O	131	NC	I/O
22	16	VCC	59	NC	I/O	96	NC	I/O	132	93	I/O
23	17	I/O	60	43	I/O	NC	68	I/O	133	NC	I/O
24	18	I/O	61	44	I/O	97	NC	I/O	134	94	I/O
25	NC	I/O	62	45	I/O	98	69	I/O	135	NC	I/O
26	19	I/O	63	NC	I/O	99	NC	I/O	136	NC	I/O
27	NC	I/O	64	NC	I/O	100	70	I/O	NC	95	I/O
28	20	I/O	65	46	I/O	101	71	I/O	137	NC	I/O
29	21	I/O	66	NC	GND	102	NC	GND	138	NC	GND
30	NC	GND	67	NC	I/O	103	NC	I/O	139	96	I/O
31	NC	I/O	68	NC	I/O	104	72	I/O	140	97	I/O
32	22	I/O	69	47	I/O	105	NC	I/O	141	98	I/O
33	23	I/O	70	48	I/O	106	73	I/O	142	99	I/O
34	NC	I/O	71	49	TRSTB	107	74	I/O	143	100	TDO
35	NC	I/O	72	50	TMS	108	75	I/O	144	1	I/O
36	24	I/O	73	51	I/O	109	76	TCK			
37	25	I/O	74	52	I/O	110	77	STM			

PIN DESCRIPTIONS

Pin	Function	Description
TDI	Test Data In for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TRSTB	Active low Reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
VCC	Power supply pin	Connect to 3.3V supply.
VCCIO	Input voltage tolerance pin	Connect to 5.0 volt supply if 5 volt input tolerance is required, otherwise connect to 3.3V supply.
GND	Ground pin	Connect to ground.

ORDERING INFORMATION



* Contact QuickLogic regarding availability.

ABSOLUTE MAXIMUM RATINGS

VCC Voltage …….. -0.5 to 4.6V
VCCIO Voltage……-0.5 to 7.0V
Input Voltage ……..… -0.5 to VCCIO +0.5V
Latch-up Immunity ……. ±200 mA

DC Input Current ….……..±20 mA
ESD Pad Protection ….……..……..±2000V
Storage Temperature……..…….-65°C to + 150°C
Lead Temperature ……..……300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
VCCIO	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-0 Speed Grade			0.43	1.90	0.46	1.85	
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	
		-3 Speed Grade			0.43	0.95	0.46	0.93	
		-4 Speed Grade			0.43	0.86	0.46	0.84	

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		0.5VCC	VCCIO+0.5	V
VIL	Input LOW Voltage		-0.5	0.3VCC	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 µA	0.9VCC		V
VOL	Output LOW Voltage	IOL = 16 mA [1]		0.45	V
		IOL = 1.5 mA		0.1VCC	V
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-10	10	µA
CI	Input Capacitance [2]			10	pF
IOS	Output Short Circuit Current [3]	VO = GND	-15	-180	mA
		VO = VCC	40	210	mA
ICC	D.C. Supply Current [4]	VI, VIO = VCCIO or GND	0.50 (typ)	2	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	µA

Notes:

[1] Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
[2] Capacitance is sample tested only. Clock pins are 12 pF maximum.
[3] Only one output at a time. Duration should not exceed 30 seconds.
[4] For -1/-2/-3/-4 commercial grade devices only. Maximum ICC is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer engineering.

AC CHARACTERISTICS at VCC = 3.3V, TA = 25°C (K = 1.00)

(To calculate delays, multiply the appropriate K factor in the "Operating Range" section by the following numbers.)

Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [5]				
		1	2	3	4	8
tPD	Combinatorial Delay [6]	1.4	1.7	1.9	2.2	3.2
tSU	Setup Time [6]	1.7	1.7	1.7	1.7	1.7
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
tCWHI	Clock High Time	1.2	1.2	1.2	1.2	1.2
tCWLO	Clock Low Time	1.2	1.2	1.2	1.2	1.2
tSET	Set Delay	1.0	1.3	1.5	1.8	2.8
tRESET	Reset Delay	0.8	1.1	1.3	1.6	2.6
tSW	Set Width	1.9	1.9	1.9	1.9	1.9
tRW	Reset Width	1.8	1.8	1.8	1.8	1.8

Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [5]						
		1	2	3	4	8	12	24
tIN	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
tINI	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
tISU	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
tIH	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
tICLK	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
tIRST	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
tIESU	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
tIEH	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Notes:

[5] Stated timing for worst case Propagation Delay over process variation at VCC=3.3V and TA=25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

[6] These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell *including typical net delays*. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [7]						
		1	2	3	4	8	10	11
tACK	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
tGCKP	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
tGCKB	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

I/O Cells

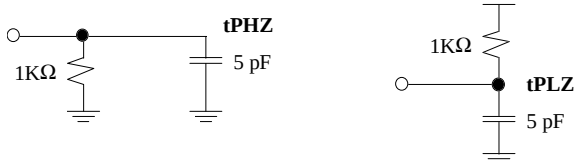
Symbol	Parameter	Propagation Delays (ns) Fanout [5]					
		1	2	3	4	8	10
tI/O	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
tISU	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
tIH	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
tIOCLK	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
tIORST	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
tIESU	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
tIEH	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
tOUTHL	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
tPZH	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
tPZL	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
tPHZ	Output Delay High to Tri-State [8]	2.0				
tPLZ	Output Delay Low to Tri-State [8]	1.2				

Notes:

[7] The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.

[8] The following loads are used for tPXZ:



QL3012-rev. B