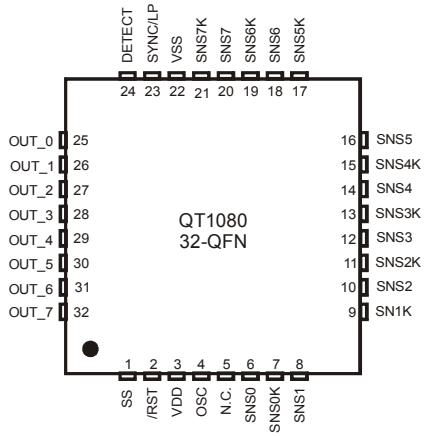
QT1080

8 KEY QTOUCH™ SENSOR IC

- **8 completely independent QT touch sensing fields**
- **Designed for low-power portable applications**
- **100% autocal for life - no adjustments required**
- **Direct outputs - either encoded or 'per key'**
- **Fully debounced results**
- **2.8V ~ 5.0V single supply operation**
- **45µA current typ @ 3V in 360ms LP mode**
- **AKS™ Adjacent Key Suppression**
- **Spread spectrum bursts for superior noise rejection**
- **Sync pin for excellent LF noise rejection**
- **10ms 'fast mode' for use in slider applications**
- **Pb-free packages: 32-QFN and 48-SSOP**



APPLICATIONS

- **MP3 players**
- **Mobile phones**
- **PC peripherals**
- **Television controls**
- **Pointing devices**
- **Remote controls**

QT1080 charge-transfer ("QT'") QTouch IC is a self-contained digital controller capable of detecting near-proximity or touch on up to 8 electrodes. It allows electrodes to project independent sense fields through any dielectric such as glass or plastic. This capability coupled with its continuous self-calibration feature can lead to entirely new product concepts, adding high value to product designs. The devices are designed specifically for human interfaces, like control panels, appliances, gaming devices, lighting controls, or anywhere a mechanical switch or button may be found; they may also be used for some material sensing and control applications.

Each of the channels operates independently of the others, and each can be tuned for a unique sensitivity level by simply changing a corresponding external Cs capacitor.

AKS™ Adjacent Key Suppression (patent pending) suppresses touch from weaker responding keys and allows only a dominant key to detect, for example to solve the problem of large fingers on tightly spaced keys.

Spread spectrum burst technology provides superior noise rejection. These devices also have a SYNC/LP pin which allows for synchronization with additional similar parts and/or to an external source to suppress interference, or, an LP (low power) mode which conserves power.

By using the charge transfer principle, this device delivers a level of performance clearly superior to older technologies yet is highly cost-effective.

This part is available in both 32-QFN and 48-SSOP lead-free packages.

AVAILABLE OPTIONS

T_A	32-QFN	48-SSOP
-40ºC to +85ºC	QT1080-ISG	QT1080-IS48G

1 - OVERVIEW

The QT1080 is an easy to use, 8 touch-key sensor IC based on Quantum's patented charge-transfer principles for robust operation and ease of design. This device has many advanced features which provide for reliable, trouble-free operation over the life of the product.

Burst operation: The device operates in 'burst mode'. Each key is acquired using a burst of charge-transfer sensing pulses whose count varies depending on the value of the reference capacitor Cs and the load capacitance Cx. In LP mode, the device sleeps in an ultra-low current state between bursts to conserve power. The keys signals are acquired using two successive bursts of pulses:

Burst A: Keys 0, 1, 4, 5
Burst B: Keys 2, 3, 6, 7

Bursts always operate in A-B sequence.

Self-calibration: On power-up, all 8 keys are self-calibrated within 350 milliseconds (typical) to provide reliable operation under almost any conditions.

Auto-recalibration: The device can time out and recalibrate each key independently after a fixed interval of continuous touch detection, so that the keys can never become 'stuck on' due to foreign objects or other sudden influences. After recalibration the key will continue to function normally. The delay is selectable to be either 10s, 60s, or infinite (disabled).

The device also auto-recalibrates a key when its signal reflects a sufficient decrease in capacit ance. In this case the device recalibrates after ~2 seconds so as to recover normal operation quickly.

Drift compensation operates to correct the reference level of each key slowly but automatically over time, to suppress false detections caused by changes in temperature, humidity, dirt and other environmental effects.

The drift compensation is asymmetric: in the increasing capacitive load direction the device drifts more slowly than in the decreasing direction. In the increasing direction, the rate of compensation is 1 count of signal per 2 seconds; in the opposing direction, it is 1 count every 500ms.

Detection Integrator ('DI') confirmation reduces the effects of noise on the QT1080 outputs. The 'detect integrator' mechanism requires consecutive detections over a number of measurement bursts for a touch to be confirmed and indicated on the outputs. In a like manner, the end of a touch (loss of signal) has to be confirmed over a number of measurement bursts. This process acts as a type of 'debounce' against noise.

In normal operation, both the start and end of a touch must be confirmed for 6 measurement bursts. In a special 'Fast Detect' mode (available via jumper resistors), confirmation of the start of a touch requires only 2 sequential detections, but confirmation of the end of a touch is still 6 bursts.

Fast detect is only available when AKS is disabled.

Spread Spectrum operation: The bursts operate over a spread of frequencies, so that external fields will have minimal effect on key operation and emissions are very weak. Spread spectrum operation works with the 'detect integrator' (DI) mechanism to dramatically reduce the probability of false detection due to noise.

Sync Mode: The QT1080 features a Sync mode to allow the device to slave to an external signal source, such as a mains signal (50/60Hz), to limit interference effects. This is performed using the SYNC/LP pin. Sync mode operates by triggering two sequential acquire bursts, in sequence A-B from the Sync signal (see above); thus, each Sync pulse causes all 8 keys to be acquired.

Low Power (LP) Mode: The device features an LP mode for microamp levels of current drain with a slower response time, to allow use in battery operated devices. On detection of touch, the device automatically reverts to its normal mode and asserts the DETECT pin active to wake up a host controller. The device remains in normal, full acquire speed mode until another pulse is seen on its SYNC/LP pin, upon which it goes back to LP mode.

AKS™ Adjacent Key Suppression is a patent-pending feature that can be enabled via jumper resistors. AKS works to prevent multiple keys from responding to a single touch, a common complaint about capacitive touch panels. This can happen with closely spaced keys, or with control surfaces that have water films on them.

AKS operates by comparing signal strengths from keys within a group of keys to suppress touch detections from those that have a weaker signal change than the dominant one.

The QT1080 has two different AKS groupings of keys, selectable via option resistors. These groupings are:

- AKS operates in two groups of 4 keys.
- AKS operates over all 8 keys.

These two modes allow the designer to provide AKS while also providing for shift or function operations.

If AKS is disabled, all keys can operate simultaneously.

Outputs: There are two output modes: one per key, and binary coded.

One per key outputs: In this mode there is one output pin per key. This mode has two output drive options, push-pull and open-drain. The outputs can also be made either active-high or active-low. These options are set via external configuration resistors.

Binary coded outputs: In this mode, 3 output lines encode for one possible key in detect. If more than one key is detecting, only the first one touched will be indicated.

Simplified Mode: To reduce the need for option resistors, the simplified operating mode places the part into fixed settings with only the AKS feature being selectable. LP mode is also possible in this configuration. Simplified mode is suitable for most applications.

1.1 - Wiring

Table 1.1 Pinlist

32-QFN Pin	48-SSOP Pin	Name	Type	Function	Notes	If Unused
1	33	SS	OD	Spread spectrum	Spread spectrum drive	100K resistor to Vss
-	34	n/c	-	-	Leave open	-
2	35	/RST	I	Reset input	Active low reset	Vdd
3	36	Vdd	Pwr	Power	+2.8 ~ +5.0V	-
4	37	OSC	I	Oscillator	Resistor to Vdd and optional spread spectrum RC network	-
5	38, 39, 40, 41, 42	n/c	-	-	Leave open	-
6	43	SNS0	I/O	Sense pin and option select	To Cs0 and/or option resistor	Option resistor
7	44	SNS0K	I/O	Sense pin	To Cs0 + Key	Open
8	45	SNS1	I/O	Sense pin and option select	To Cs1 and/or option resistor*	Open or option resistor*
9	46	SNS1K	I/O	Sense pin	To Cs1 + Key	Open
10	47	SNS2	I/O	Sense pin and option select	To Cs2 and/or option resistor*	Open or option resistor*
11	48	SNS2K	I/O	Sense pin	To Cs2 + Key	Open
12	1	SNS3	I/O	Sense pin and option select	To Cs3 and/or option resistor*	Open or option resistor*
13	2	SNS3K	I/O	Sense pin	To Cs3 + Key	Open
14	3	SNS4	I/O	Sense pin and option select	To Cs4 and/or option resistor*	Open or option resistor*
15	4	SNS4K	I/O	Sense pin	To Cs4 + Key	Open
16	5	SNS5	I/O	Sense pin and option select	To Cs5 and/or option resistor*	Open or option resistor*
17	6	SNS5K	I/O	Sense pin	To Cs5 + Key	Open
18	7	SNS6	I/O	Sense pin and option select	To Cs6 and/or option resistor*	Open or option resistor*
19	8	SNS6K	I/O	Sense pin and mode select	To Cs6 + Key and/or mode resistor†	Open or mode resistor†
20	9	SNS7	I/O	Sense pin and mode or option select	To Cs7 and/or mode resistor† or option resistor*	Open or mode resistor† or option resistor*
21	10	SN7K	I/O	Sense pin	To Cs7 + Key	Open
-	11, 12, 13, 14, 15, 16	n/c	-	-	Leave open	-
22	17	Vss	Pwr	Ground	0V	-
-	18, 19, 20	n/c	-	-	Leave open	-
23	21	SYNC/LP‡	I	Sync In or LP In	Rising edge sync or LP pulse	Vdd or Vss
24	22	DETECT	O/OD	Detect Status	Active = any key in detect	Open
-	23, 24	n/c	-	-	Leave open	-
25	25	OUT_0	O/OD	Out 0	Also, binary coded output 0	Open
26	26	OUT_1	O/OD	Out 1	Also, binary coded output 1	Open
27	27	OUT_2	O/OD	Out 2	Also, binary coded output 2	Open
28	28	OUT_3	O/OD	Out 3	In binary coded mode, these pins are clamped internally to Vss	Open
29	29	OUT_4	O/OD	Out 4		Open
30	30	OUT_5	O/OD	Out 5		Open
31	31	OUT_6	O/OD	Out 6		Open
32	32	OUT_7	O/OD	Out 7		Open

Pin Type

I	CMOS input only
I/O	CMOS I/O
O	CMOS push-pull output
OD	CMOS open drain output
O/OD	CMOS push pull or open-drain output (option selected)
Pwr	Power / ground

Notes

† Mode resistor is required only in Simplified mode (see Figure 1.2)
* Option resistor is required only in Full Options mode (see Figure 1.1)
‡ Pin is either Sync or LP depending on options selected (functions SL_0, SL_1, see Figure 1.1)

Figure 1.1 Connection Diagram - Full Options; Shown for 32-QFN Package

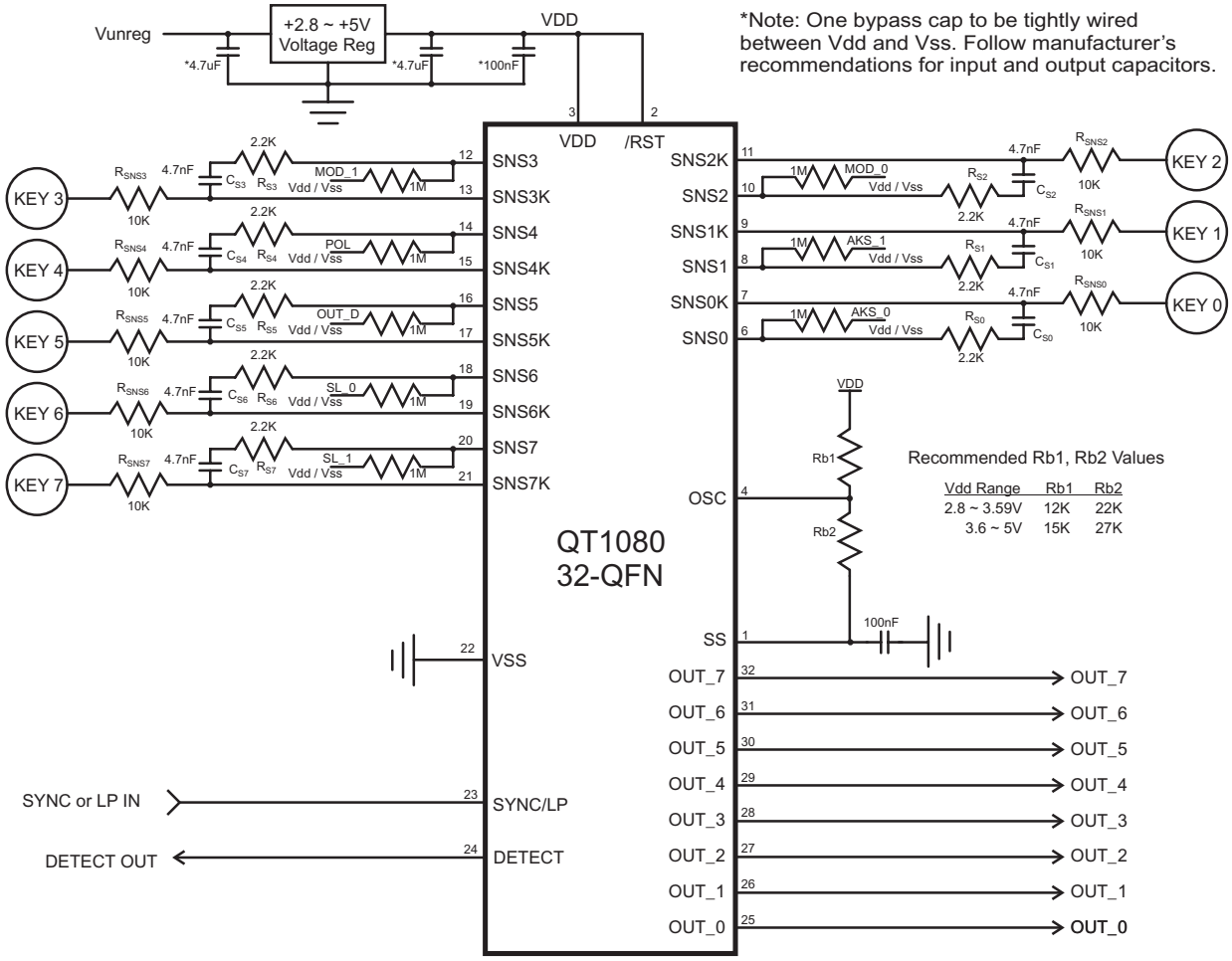


Table 1.2
AKS / Fast-Detect Options

AKS_1	AKS_0	AKS MODE	FAST-DETECT
Vss	Vss	Off	Off
Vss	Vdd	Off	Enabled
Vdd	Vss	On, in 2 groups	Off
Vdd	Vdd	On, global	Off

Table 1.3
Max On-Duration

MOD_1	MOD_0	MAX ON-DURATION MODE
Vss	Vss	10 seconds (nom) to recalibrate
Vss	Vdd	60 seconds (nom) to recalibrate
Vdd	Vss	Infinite (disabled)
Vdd	Vdd	(reserved)

Table 1.4
Polarity & Output

OUT_D	POL	OUT_n, DETECT PIN MODE
Vss	Vss	Binary coded, active high, push-pull
Vss	Vdd	Direct, active low, open-drain
Vdd	Vss	Direct, active high, push-pull
Vdd	Vdd	Direct, active low, push-pull

Table 1.5
SYNC/LP Function

SL_1	SL_0	SYNC/LP PIN MODE
Vss	Vss	Sync
Vss	Vdd	LP mode: 110ms nom response time
Vdd	Vss	LP mode: 200ms nom response time
Vdd	Vdd	LP mode: 360ms nom response time

Figure 1.2 Connection Diagram - Simplified Mode; Shown for 32-QFN
SMR resistor installed between SNS6K and SNS7.

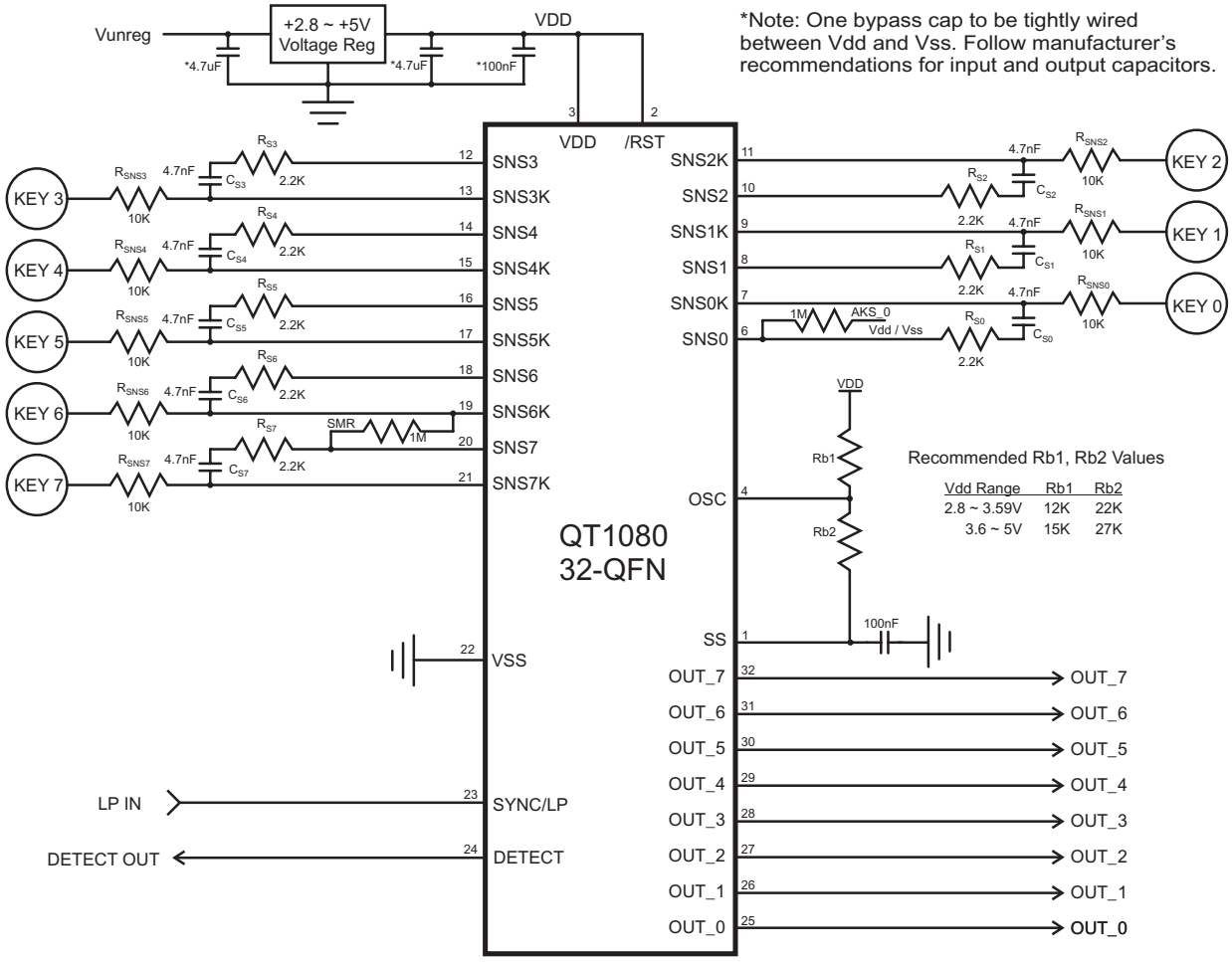


Table 1.6
AKS Resistor Options

AKS_0	AKS MODE	FAST-DETECT
Vss	Off	Enabled
Vdd	On, global	Off

Table 1.7
Functions in Simplified Mode

Output Drive, Polarity	Direct outputs, push-pull, active high
SYNC/LP pin	200ms nom LP function; sync not available
Max on-duration delay	60 seconds (nom)
Detect Pin	Active high on any detect

2 DEVICE OPERATION

2.1 Startup Time

After a reset or power-up event, the device requires 350ms to initialize, calibrate, and start operating normally. Keys will work properly once all keys have been calibrated after reset.

2.2 Option Resistors

The option resistors are read on power-up only. There are two primary option mode configurations: full, and simplified.

In full options mode, eight 1MΩ option resistors are required as shown in Figure 1.1. All eight resistors are mandatory.

To obtain simplified mode, a 1MΩ resistor should be connected from SNS6K to SNS7. In simplified mode, only one additional 1MΩ option resistor is required for the AKS feature (Figure 1.2).

Note that the presence and connection of option resistors will affect the required values of Cs; this effect will be especially noticeable if the Cs values are under 22nF. Cs values should be adjusted for optimal sensitivity after the option resistors are connected.

2.3 OUT Pins - Direct Mode

Direct output mode is selected via option resistors, as shown in Table 1.4.

In this mode, there is one output for each key; each is active when there is a touch confirmed on the corresponding electrode. Unused OUT pins should simply be left open.

If AKS is off, it is possible for all OUT pins to be active at the same time.

Circuit of Figure 1.1: OUT polarity and drive are governed by the resistor connections to Vdd or Vss according to Table 1.4. The drive can be either push-pull or open-drain, active low or high.

Circuit of Figure 1.2: In this simplified circuit, the OUT pins are active high, push-pull only.

2.4 OUT Pins - Binary Coded Mode

Binary code mode is selected via option resistors, as shown in Table 1.4.

In this mode, a key detection is registered as a binary code on pins OUT_2, OUT_1 and OUT_0, with possible values from 000 to 111. In practice, 4 lines are required to read the code, unless key 0 is not implemented: the output code 000 can mean either 'nothing detecting' or 'key 0 is detecting'. The 4th required line (if all 8 keys are implemented) is the DETECT signal, which is active-high when any key is active.

The first key touched always wins and shows its output. Keys that come afterwards are hidden until the currently reported key has stopped detecting, in which case the code will change to the latent key.

This mode is useful to reduce the number of connections to a host controller, at the expense of being able to only report one active key at a time. Note that in global AKS mode (Section 2.7), only one key can report active at a time anyway.

Circuit of Figure 1.1: OUT polarity and drive can only be push-pull and active high.

Circuit of Figure 1.2: Binary coded not available.

2.5 DETECT Pin

DETECT represents the functional logical-OR of all eight keys. DETECT can be used to wake up a battery-operated product upon human touch.

DETECT is also required to indicate to a host when the binary coded output pins (in that mode) are showing an active key. While DETECT is active, the binary coded outputs should be read at least twice along with DETECT to make sure that the code was not transitioning between states, to prevent a false reading.

The output polarity and drive of DETECT are governed according to Table 1.4.

2.6 SYNC/LP Pin

The SYNC / LP pin function is configured according to the SL_0 and SL_1 resistor connections to either Vdd or Vss, according to the Table 1.5.

Sync mode: Sync allows the designer to synchronize acquire bursts to an external signal source, such as mains frequency (50/60 Hz) to suppress interference. It can also be used to synchronize two QT parts which operate near each other, so that they will not cross-interfere if two or more of the keys (or associated wiring) of the two parts are near each other.

The SYNC input of the QT1080 is positive pulse triggered. If the SYNC input does not change, the device will free-run at its own rate after ~150ms.

A trigger pulse on SYNC will cause the device to fire two acquire bursts in A-B sequence:

Burst A: Keys 0, 1, 4, 5
Burst B: Keys 2, 3, 6, 7

Low Power LP Mode: This allows the device to enter a slow mode with very low power consumption, in one of three response time settings - 110ms, 200ms, and 360ms nominal.

LP mode is entered by a positive, >150µs trigger pulse on the SYNC/LP pin. Once the LP pulse is detected, the device will enter and remain in this microamp mode until it senses and confirms a touch, upon which it will switch back to normal (full speed) mode on its own, with a response time of 30ms typical (burst length dependent). The device will go back to LP mode again if SYNC/LP is held high, or after another LP pulse is received.

The response time setting is determined by option resistors SL_1 and SL_0; see Table 1.5. Slower response times result in lower power drain.

The SYNC/LP pulse should be >150µs in duration.

If the SYNC/LP pin is held high permanently, the device will go into normal mode during a key touch, and return to low-current mode when the detection ceases.

If the SYNC/LP pin is held low constantly, the device will simply remain in normal mode (25ms typical response time) continuously.

2.7 AKS™ Function Pins

The QT1080 features an adjacent key suppression (AKS™) function with 2 modes. Option resistors act to set this feature according to Tables 1.2 and 1.6. AKS can also be disabled, allowing any combination of keys to become active at the same time. When operating, the modes are:

Global: AKS functions operates across all 8 keys. This means that only one key can be active at any one time.

Groups: AKS functions among two groups of four keys: 0-1-4-5 and 2-3-6-7. This means that up to 2 keys can be active at any one time.

In Group mode, keys in one group have no AKS interaction with keys in the other group.

Note that in Fast Detect mode, AKS can only be off.

2.8 MOD_0, MOD_1 Inputs

In full option mode, MOD_0 and MOD_1 resistors are used to set the 'Max On-Duration' recalibration timeouts. If a key becomes stuck on for a lengthy duration of time, this feature will cause an automatic recalibration event of that specific key only once the specified on-time has been exceeded. Settings of 10s, 60s, and infinite are available.

The Max On-Duration feature operates on a key-by-key basis; when one key is stuck on, its recalibration has no effect on other keys.

The logic combination on the MOD option pins sets the timeout delay; see Table 1.3.

Simplified mode MOD timing: In simplified mode, the max on-duration is fixed at 60 seconds.

2.9 Fast Detect Mode

In many applications, it is desirable to sense touch at high speed. Examples include scrolling 'slider' strips or 'Off' buttons. It is possible to place the device into a 'Fast Detect' mode that usually requires under 10ms to respond. This is accomplished internally by setting the Detect Integrator to only 2 counts, i.e. only two successive detections are required to detect touch.

In LP mode, 'Fast' detection will not speed up the initial delay (which could be up to 360ms nominal depending on the option setting), however once a key is detected the device is forced back into normal speed mode; it will remain in this faster mode until another LP pulse is received.

When used in a 'slider' application, it is normally desirable to run the keys without AKS.

In both normal and 'Fast' modes, the time required to process a key release is the same: it takes 6 sequential confirmations of non-detection to turn a key off.

Fast Detect mode can be enabled as shown in Tables 1.2 and 1.6.

2.10 Simplified Mode

A simplified operating mode which does not require the majority of option resistors is available. This mode is set by connecting a resistor labelled SMR between pins SNS6K and SNS7; see Figure 1.2.

In this mode there is only one option possible - AKS enable or disable. When AKS is disabled, Fast Detect mode is enabled; when AKS is enabled, Fast Detect mode is off.

AKS in this mode is Global only (i.e. operates across all functioning keys).

The other option features are fixed as follows:

OUT_n, DETECT Pins: Push-pull, active high, direct outputs

SYNC/LP Function: LP mode, ~200ms response time

Max On-Duration: 60 seconds

See also Tables 1.6 and 1.7.

2.11 Unused Keys

Unused keys should be disabled by removing the corresponding Cs, Rs, and Rsns components and connecting SNS pins as shown in the 'Unused' column of Table 1.1. Unused keys are ignored and do not factor into the AKS function (Section 2.7).

3 - DESIGN NOTES

3.1 Oscillator Frequency

The QT1080's internal oscillator runs from an external resistor network connected to the OSC and SS pins as shown in Figures 1.1 and 1.2 to achieve spread spectrum operation. If spread spectrum mode is not required, the OSC pin should simply be connected to Vdd with an 18K ohm 1% resistor.

Under different Vdd voltage conditions the resistor network (or the solitary 18K ohm resistor) might require minor adjustment to obtain the specified burst center frequency. The network should be adjusted slightly so that the positive pulses on any key are approximately 2µs wide in the 'solitary 18K resistor' mode, or 2.15µs wide at the beginning of a burst with the recommended spread spectrum circuit (see next section).

In practice, the pulse width has little effect on circuit performance if it varies in the range from 1.5µs to 2.5µs. The only effects will be seen in non-LP mode, as proportional variations in Max On-Duration times and response times.

3.2 Spread Spectrum Circuit

The QT1080 offers the ability to spectrally spread its frequency of operation to heavily reduce susceptibility to external noise sources and to limit RF emissions. The SS pin is used to modulate an external passive RC network that modulates the OSC pin. OSC is the main oscillator current input. The circuit is shown in both Figures 1.1 and 1.2.

The resistors Rb1 and Rb2 should be changed depending on Vdd. As shown in Figures 1.1 and 1.2, two sets of values are recommended for these resistors depending on Vdd. The power curves in Section 4.6 also show the effect of these resistors.

The circuit can be eliminated if it is not desired by simply using an 18K ohm resistor from OSC to Vdd to drive the oscillator, and connecting SS to Vss with a 100K ohm resistor. This mode consumes significantly less current than spread spectrum mode.

The spread-spectrum RC network might need to be modified slightly if the burst lengths are particularly long. Vdd variations can shift the center frequency and spread slightly. The sawtooth waveform observed on SS should reach a crest height as follows:

Vdd >= 3.6V: 17% of Vdd
Vdd < 3.6V: 20% of Vdd

The 100nF capacitor connected to SS (Figures 1.1 and 1.2) should be adjusted so that the waveform approximates the above amplitude, +/-10%, during normal operation in the target circuit. If this is done, the circuit will give a spectral modulation of 12-15%.

3.3 Cs Sample Capacitors; Sensitivity

The Cs sample capacitors accumulate the charge from the key electrodes and determine sensitivity. Higher values of Cs make the corresponding sensing channel more sensitive. The values of Cs can differ for each channel, permitting differences in sensitivity from key to key or to balance unequal sensitivities. Unequal sensitivities can occur due to key size and placement differences and stray wiring capacitances. More stray capacitance on a sense trace will desensitize the corresponding key; increasing the Cs for that key will compensate for the loss of sensitivity.

The Cs capacitors can be virtually any plastic film or low to medium-K ceramic capacitor. The 'normal' Cs range is 2.2nF to 50nF depending on the sensitivity required; larger values of Cs require better quality to ensure reliable sensing. Acceptable capacitor types for most uses include PPS film, polypropylene film, and NP0 and X7R ceramics. Lower grades than X7R are not advised.

The required values of Cs can be noticeably affected by the presence and connection of the option resistors (see Section 2.2).

3.4 Power Supply

The power supply can range from 2.8 to 5.0 volts. If this fluctuates slowly with temperature, the device will track and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism will not be able to keep up, causing sensitivity anomalies or false detections.

The power supply should be locally regulated using a 3-terminal device, to between 2.8V and 5.0V. If the supply is shared with another electronic system, care should be taken to ensure that the supply is free of digital spikes, sags, and surges which can cause adverse effects.

For proper operation a 0.1µF or greater bypass capacitor must be used between Vdd and Vss; the bypass capacitor should be routed with very short tracks to the device's Vss and Vdd pins.

3.5 PCB Layout and Construction

Please refer to Quantum application note AN-KD02 for information related to layout and construction matters.

4 - SPECIFICATIONS

4.1 Absolute Maximum Specifications

Operating temperature, Ta. . . . . -40 ~ +85ºC
Storage temp, Ts. . . . . -50ºC ~ +125ºC
Vdd. . . . . -0.3 ~ +6.0V
Max continuous pin current, any control or drive pin. . . . . ±20mA
Short circuit duration to ground or Vdd, any pin. . . . . infinite
Voltage forced onto any pin. . . . . -0.3V ~ (Vdd + 0.3) Volts

4.2 Recommended Operating Conditions

Operating temperature, Ta. . . . . -40 ~ +85ºC
VDD. . . . . +2.8 ~ +5.0V
Short-term supply ripple+noise. . . . . ±5mV/s
Long-term supply stability. . . . . ±100mV
Cs range. . . . . 2.2nF ~ 100nF
Cx range. . . . . 0 ~ 50pF

4.3 AC Specifications

Vdd = 5.0, Ta = recommended, Cx = 5pF, Cs = 4.7nF; circuit of Figure 1.1

Parameter	Description	Min	Typ	Max	Units	Notes
Trc	Recalibration time		150		ms	
Fc	Burst center frequency		132		kHz	
Fm	Burst modulation, percent		15		%	Total deviation
Tpc	Sample pulse duration		2		µs	
Tsu	Startup time from cold start		350		ms	
Tbd	Burst duration		3.4		ms	Both bursts together
Tdf	Response time - Fast mode		10		ms	
Tdn	Response time - Normal mode		25		ms	
Tdl	Response time - LP mode		200		ms	200ms LP setting
Tdr	Release time - all modes		25		ms	End of touch

4.4 DC Specifications

Vdd = 5.0, Ta = recommended, Cx = 5pF, Cs = 4.7nF; circuit of Figure 1.1 unless noted

Parameter	Description	Min	Typ	Max	Units	Notes
IDDN	Supply current, normal mode*		4.5 2.7 2.2 1.8 1.5 1.3	8	mA	@ Vdd = 5.0 @ Vdd = 4.0 @ Vdd = 3.6 @ Vdd = 3.3 @ Vdd = 3.0 @ Vdd = 2.8
IDDL	Supply current, LP mode*		45		µA	@ Vdd = 3.0; 360ms LP mode
VDDS	Supply turn-on slope	100			V/s	Req'd for startup, w/o external reset ckt
VIL	Low input logic level			0.7	V	
VHL	High input logic level	3.5			V	
VOL	Low output voltage			0.5	V	7mA sink
VOH	High output voltage	Vdd-0.5			V	2.5mA source
IIL	Input leakage current			±1	µA	
AR	Acquisition resolution		8		bits	

***No spread spectrum circuit; Rosc = 18K ohms**

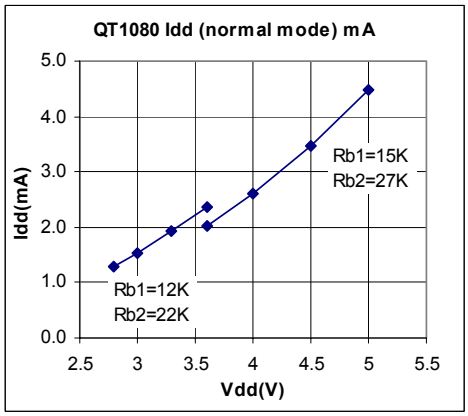
4.5 Signal Processing

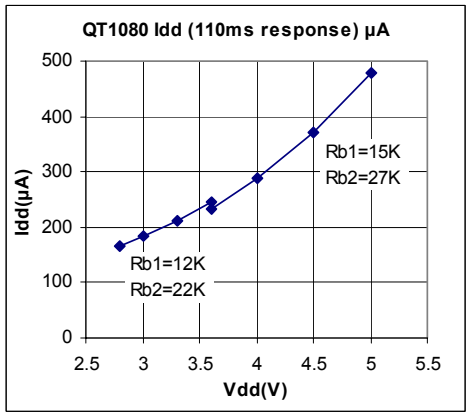
Vdd = 5.0, Ta = recommended, Cx = 5pF, Cs = 4.7nF

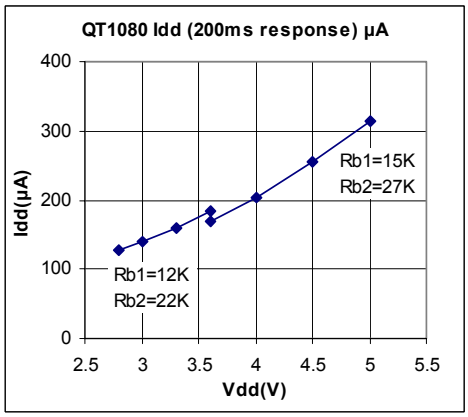
Description	Value	Units	Notes
Detection threshold	10	counts	Threshold for increase in Cx load
Detection hysteresis	2	counts	
Anti-detection threshold	6	counts	Threshold for decrease of Cx load
Anti-detection recalibration delay	2	secs	Time to recalibrate if Cx load has exceeded anti-detection threshold
Detect Integrator filter, normal mode	6	samples	Must be consecutive or detection fails
Detect Integrator filter, 'fast' mode	2	samples	Must be consecutive or detection fails
Max On-Duration	10, 60, ∞	secs	Option pin selected
Normal drift compensation rate	2,000	ms/level	Towards increasing Cx load
Anti drift compensation rate	500	ms/level	Towards decreasing Cx load

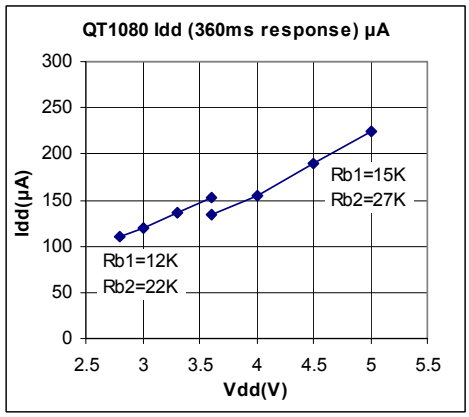
4.6 Idd Curves

Cx = 5pF, Cs = 4.7nF, Ta = 20°C, Spread spectrum circuit of Fig. 1.1.

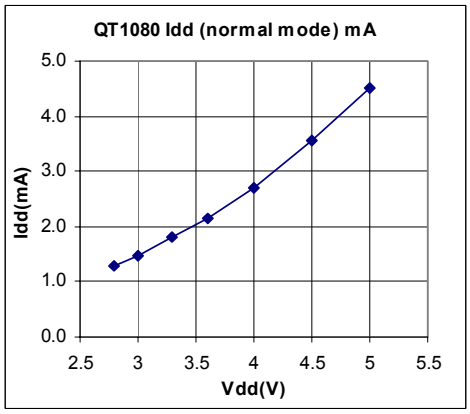


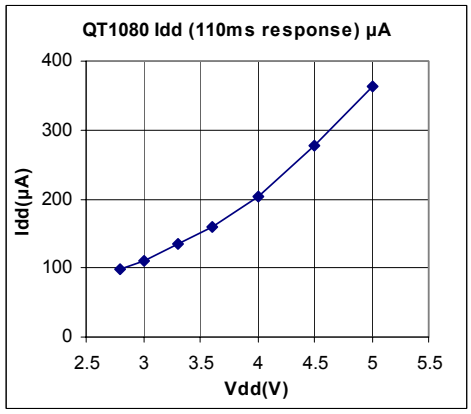


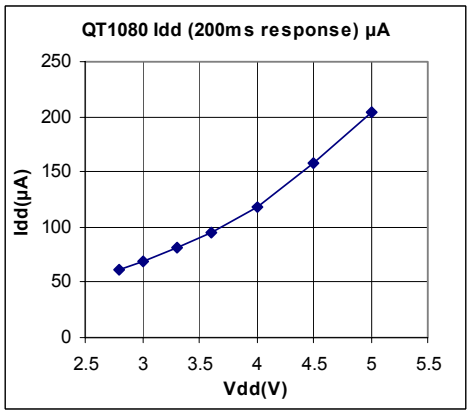


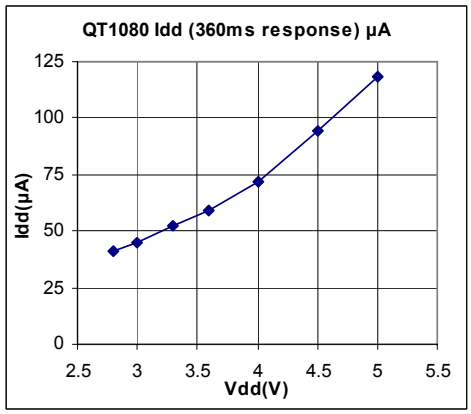


Cx = 5pF, Cs = 4.7nF, Ta = 20°C, Rosc = 18K ohms; no spread spectrum circuit

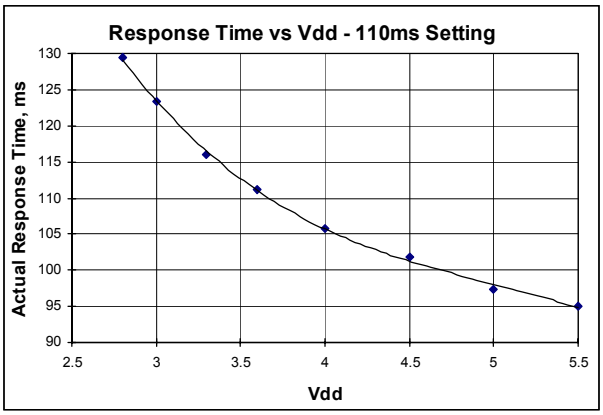


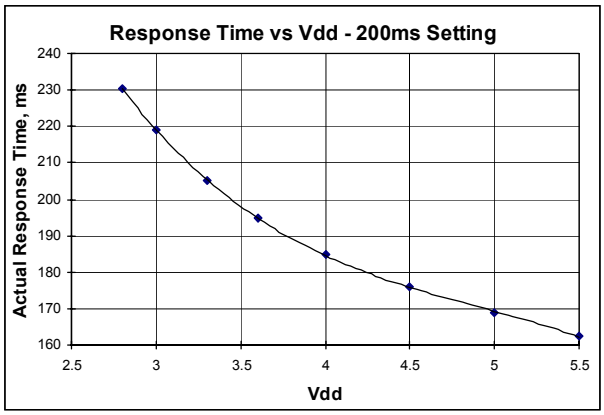


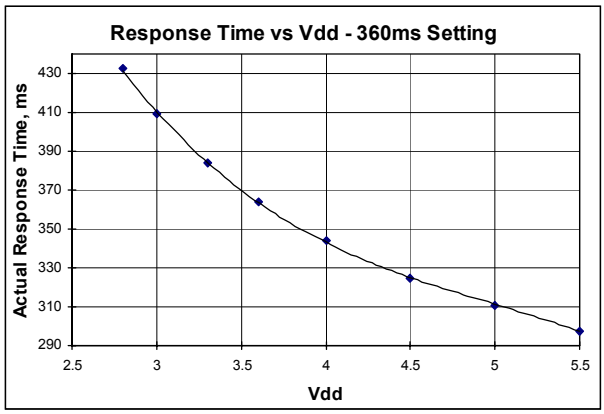




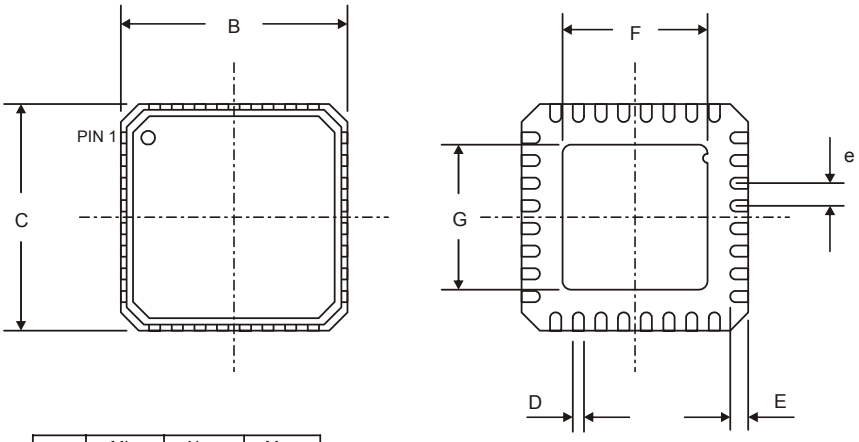
4.7 LP Mode Typical Response Times





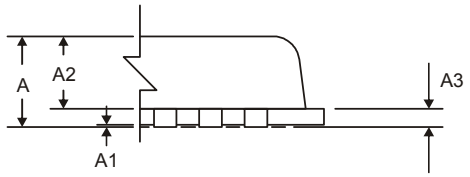


4.8 Mechanical - 32-QFN Package



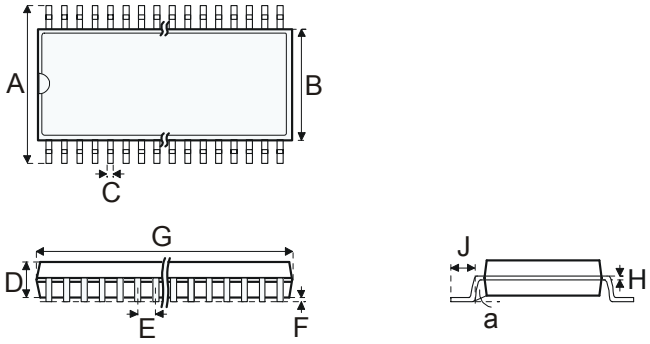
	Min	Nom.	Max
A			0.90
A1	0.00	0.01	0.05
A2		0.65	0.70
A3		0.20 Ref.	
B		5.00	
C		5.00	
D	0.20	0.25	0.32
E	0.30	0.40	0.50
F	3.35	3.50	3.65
G	3.35	3.50	3.65
e		0.50 bsc	

All dimensions in millimetres



Note that there is no functional requirement for the large pad on the underside of this package to be soldered. If the final application requires this area to be soldered for mechanical reasons, the pad to which it is soldered to must be isolated and contained under the footprint only.

4.9 Mechanical - 48-SSOP Package

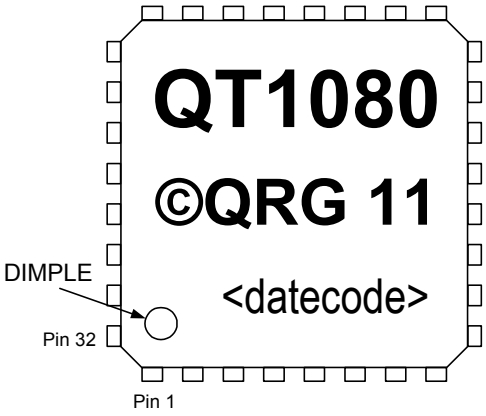


All dimensions in millimeters

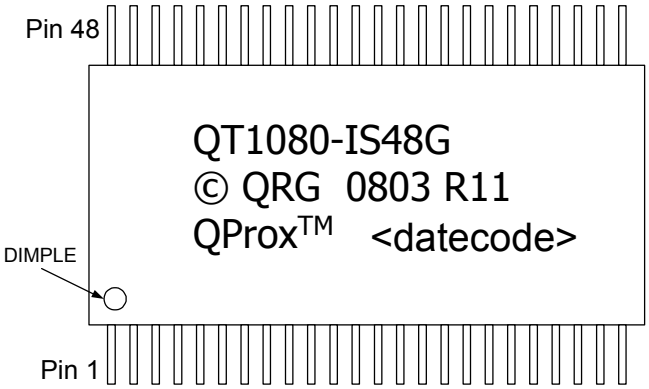
	A	B	C	D	E	F	G	H	J	a
Min	10.03	7.39	0.20	2.16	0.64 Typ	0.10	15.57	0.10	0.64	0°
Max	10.67	7.59	0.30	2.51		0.25	16.18	0.30	0.89	8°

4.10 Part Marking

32-QFN



48-SSOP



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