RF2442

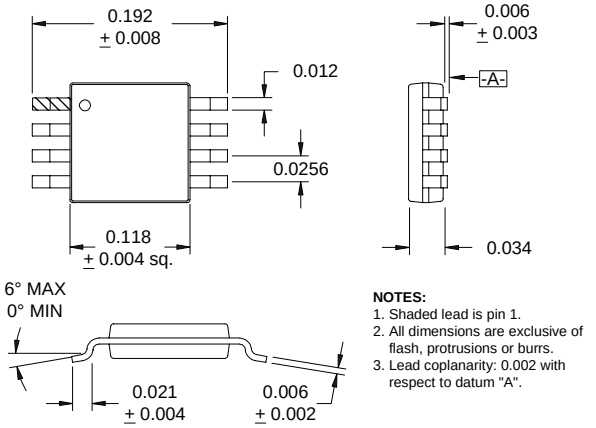
HIGH-LINEARITY LOW NOISE AMPLIFIER

Typical Applications

- TDMA/CDMA/FM Cellular Rx LNA
- TDMA/CDMA PCS Rx LNA
- Low Noise Transmit Driver Amplifier
- ISM Band LNA/Driver
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

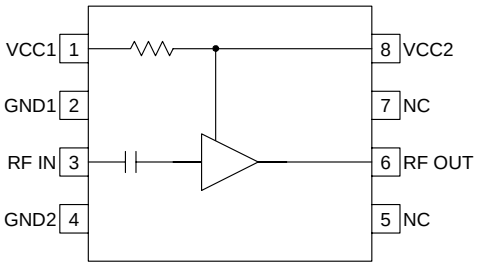
The RF2442 is a low noise amplifier with a very high dynamic range designed for the receive front end of digital cellular applications at 900MHz, 1900MHz, and 2400MHz. It is designed to amplify low level signals with minimum noise contribution while operating in the harsh, interference-rich environments of newly deployed digital subscriber units. The device also functions as an outstanding PA driver amplifier in the transmit chain of digital subscriber units where low transmit noise power is a concern. The device supports trade-offs between linearity and current drain. The designer has control of these trade-offs with the choice of an external bias resistor. The IC is featured in a standard miniature 8-lead plastic MSOP package.



Package Style: MSOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Low Noise and High Intercept Point
- External Bias Control
- Single 2.5V to 5.0V Power Supply
- 500MHz to 2500MHz Operation
- Extremely Small MSOP-8 Package

Ordering Information

RF2442	High-Linearity Low Noise Amplifier
RF2442 PCBA-L	Fully Assembled Evaluation Board (~900MHz)
RF2442 PCBA-M	Fully Assembled Evaluation Board (~1900MHz)
RF2442 PCBA-H	Fully Assembled Evaluation Board (~2400MHz)

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

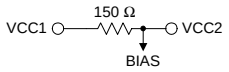
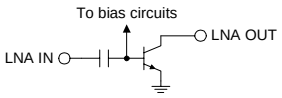
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

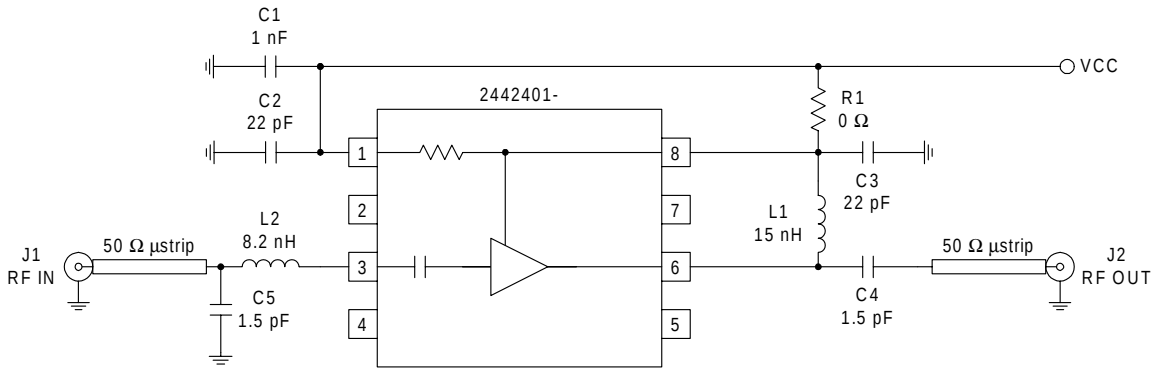
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
RF Frequency Range		500 to 2500		MHz	Requires input tuning inductor below 1GHz
881MHz Performance					Schematic Evaluation Board L (R_C=0), T=25°C, RF=881MHz
Gain	18	20	22	dB	V_{CC}=3.6V
	17	19	21	dB	V_{CC}=3.0V
	16	18	20	dB	V_{CC}=2.5V
Output P1dB		+13		dBm	V_{CC}=3.6V
		+11		dBm	V_{CC}=3.0V
Output IP3	+21	+27		dBm	V_{CC}=3.6V
	+16	+22		dBm	V_{CC}=3.0V
	+10	+16		dBm	V_{CC}=2.5V
Noise Figure		1.6	2.5	dB	V_{CC}=3.6V
		1.5	2.5	dB	V_{CC}=3.0V
		1.4	2.5	dB	V_{CC}=2.5V
Reverse Isolation	22	24		dB	V_{CC}=3.6V
	22	24		dB	V_{CC}=3.0V
	21	23		dB	V_{CC}=2.5V
1960MHz Performance					Schematic Evaluation Board M (R_C=0), T=25°C, RF=1960MHz
Gain	10	12	14	dB	V_{CC}=3.6V
	10	12	14	dB	V_{CC}=3.0V
	10	12	14	dB	V_{CC}=2.5V
Output P1dB		+16		dBm	V_{CC}=3.6V
		+13		dBm	V_{CC}=3.0V
Output IP3	+20	+26		dBm	V_{CC}=3.6V
	+15	+21		dBm	V_{CC}=3.0V
	+9	+15		dBm	V_{CC}=2.5V
Noise Figure		1.6	2.3	dB	V_{CC}=3.6V
		1.5	2.1	dB	V_{CC}=3.0V
		1.4	2.0	dB	V_{CC}=2.5V
Reverse Isolation	18	20		dB	V_{CC}=3.6V
	17	19		dB	V_{CC}=3.0V
	17	19		dB	V_{CC}=2.5V

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
2400MHz Performance					Schematic Evaluation Board H (R_C=0), T=25°C, RF=2400MHz
Gain	7	9	11	dB	V_{CC}=3.6V
	7	9	11	dB	V_{CC}=3.0V
	6	8	10	dB	V_{CC}=2.5V
Output IP3	+20	+26		dBm	V_{CC}=3.6V
	+15	+21		dBm	V_{CC}=3.0V
	+9	+15		dBm	V_{CC}=2.5V
Noise Figure		1.6	2.5	dB	V_{CC}=3.6V
		1.5	2.3	dB	V_{CC}=3.0V
		1.4	2.1	dB	V_{CC}=2.5V
Reverse Isolation	16	17		dB	V_{CC}=3.6V
	16	17		dB	V_{CC}=3.0V
	16	17		dB	V_{CC}=2.5V
Power Supply					T=25°C
Voltage		2.5 to 5.0		V	
Current Consumption	17	19	30	mA	V_{CC}=3.6V
	10	12	23	mA	V_{CC}=3.0V
	7	9	20	mA	V_{CC}=2.5V

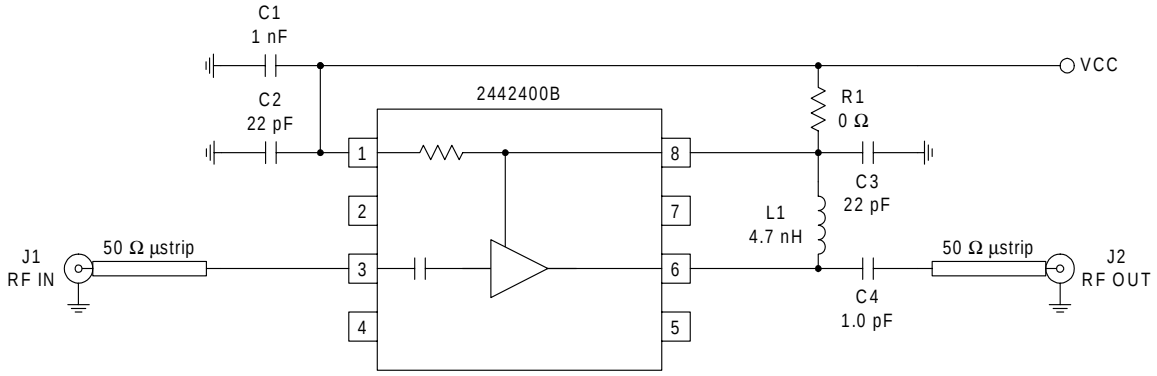
Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LNA. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. This pin connects to pin 8 through a 150Ω resistor. This allows for simple biasing of the collector at pin 6. Refer to Application Schematics 1 and 3.	
2	GND1	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
3	RF IN	RF input pin. This pin is internally DC-blocked and matched to 50Ω for frequencies above 1GHz. When using below 1GHz, it is recommended that this pin be matched with series inductance to series-resonate out the internal blocking capacitor. Refer to Application Schematics 1 and 2.	
4	GND2	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
5	NC	No connection. This pin is typically left unconnected or grounded.	
6	RF OUT	LNA Output pin. This pin is an open-collector output. It must be biased to either V_{CC} or pin 8 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	See pin 3.
7	NC	No connection. This pin is typically left unconnected or grounded.	
8	VCC2	Optional power supply connection for biasing pin 6. This pin connects to pin 1 through a 150Ω resistor. This allows for simple biasing of the collector at pin 6. When used, this pin should be RF bypassed. Refer to Application Schematics 1 and 3.	See pin 1.

Evaluation Board Schematic (L board) ~900 MHz

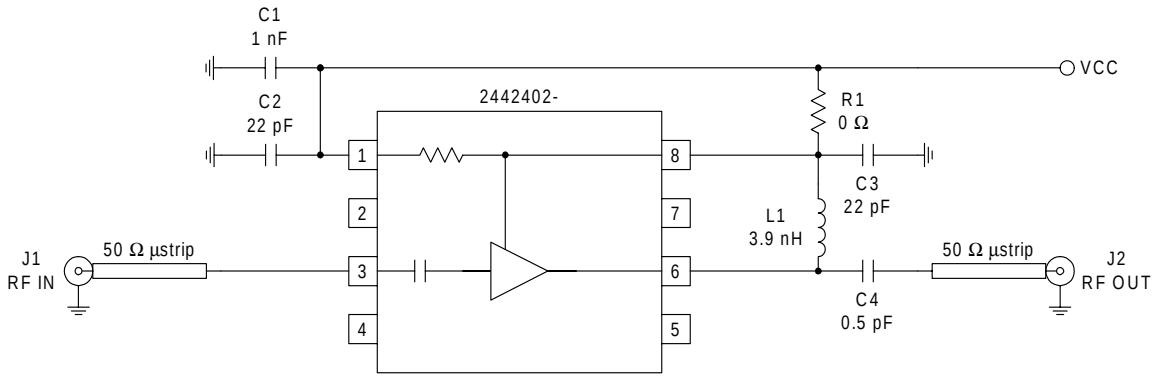
(Download Bill of Materials from www.rfmd.com.)



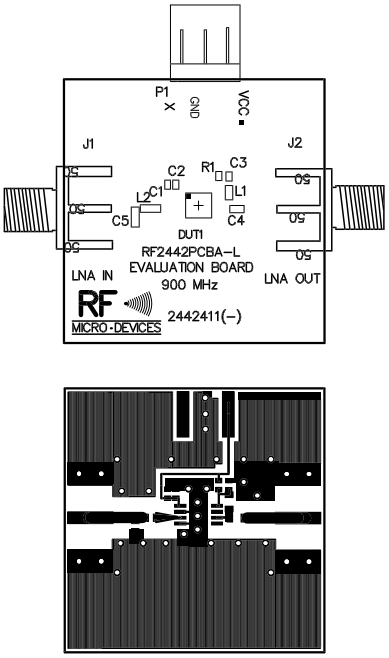
Evaluation Board Schematic (M board) ~1900 MHz



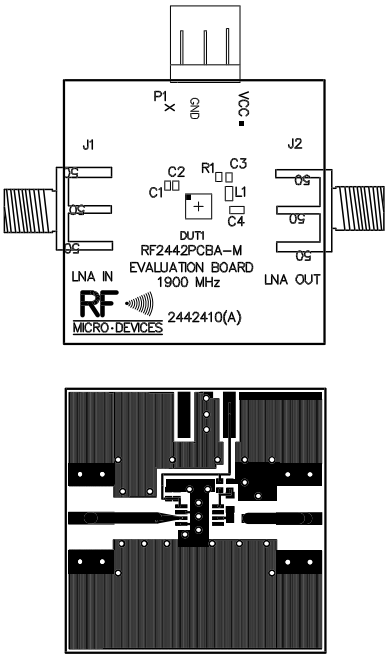
Evaluation Board Schematic (H board) ~2400 MHz



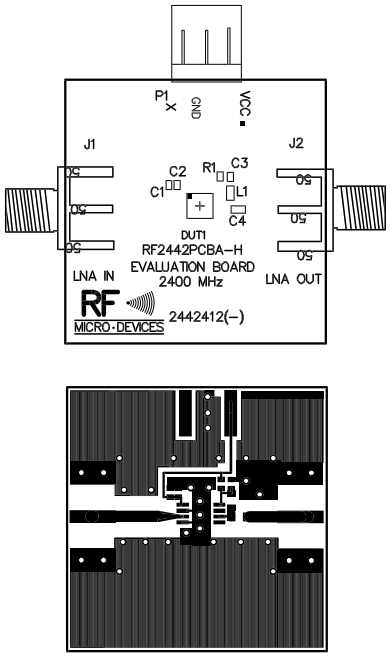
Evaluation Board Layout 900MHz
Board Size 1.150" x 1.165"



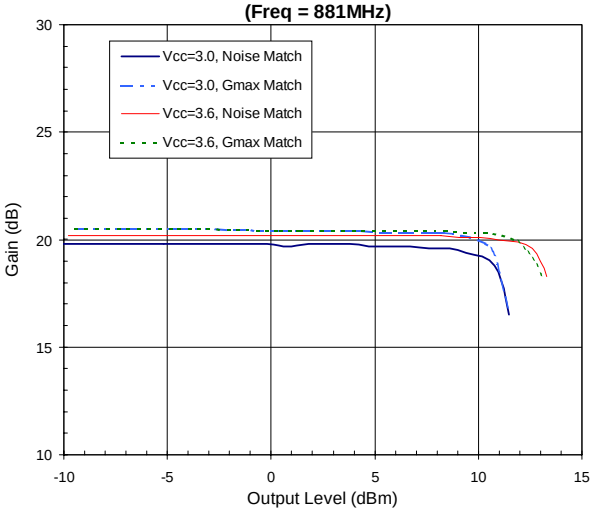
Evaluation Board Layout 1900MHz
Board Size 1.150" x 1.165"



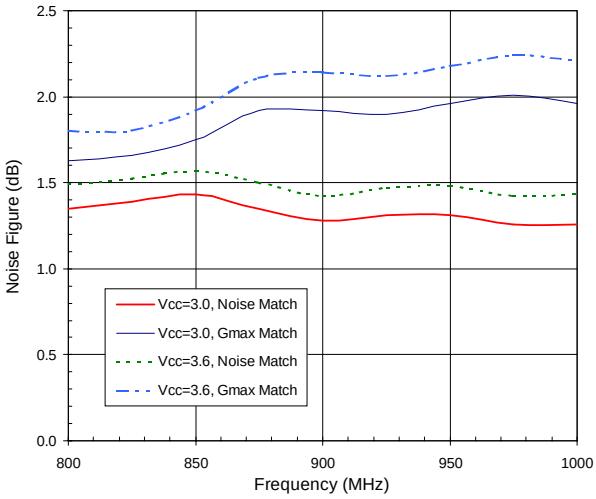
Evaluation Board Layout 2400MHz
Board Size 1.150" x 1.165"



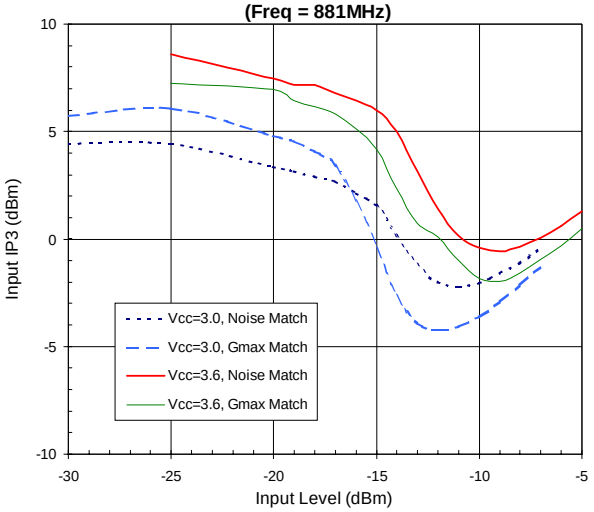
Gain vs. Output Level (Freq = 881MHz)



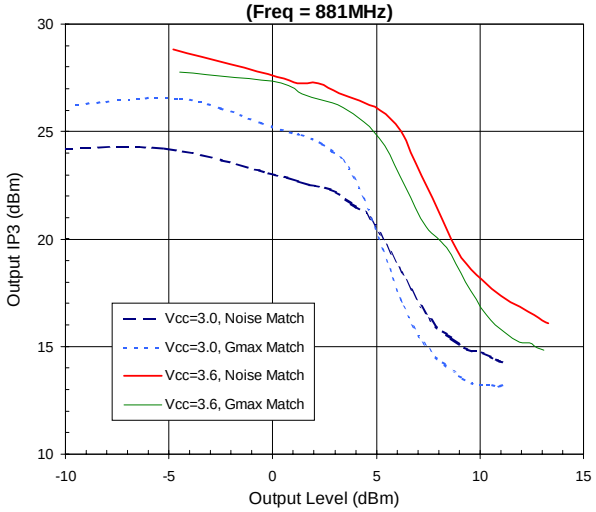
Noise Figure vs. Frequency



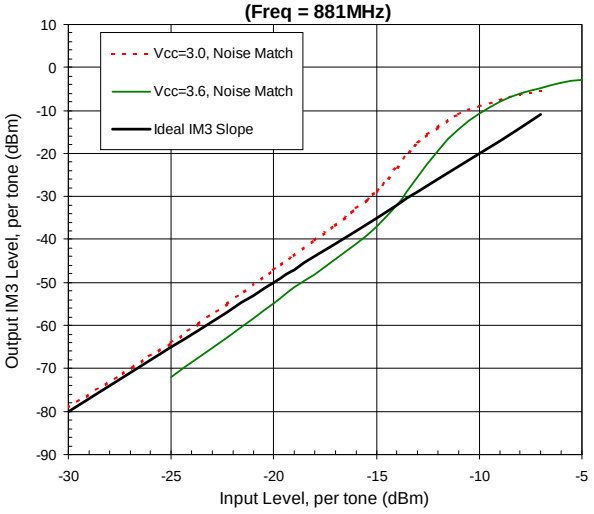
Input IP3 vs. Input Level (Freq = 881MHz)



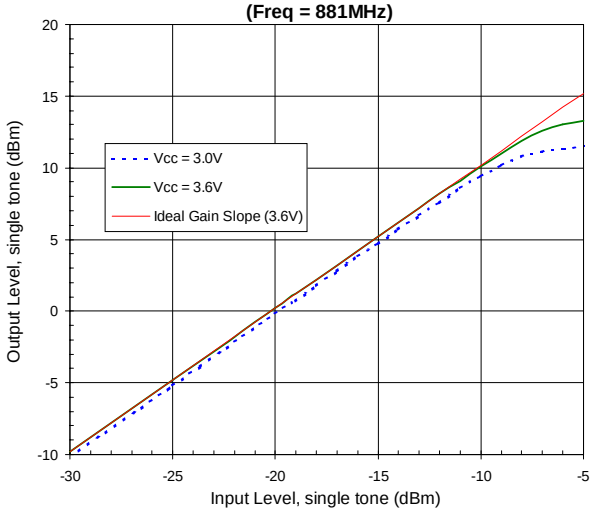
Output IP3 vs. Output Level (Freq = 881MHz)



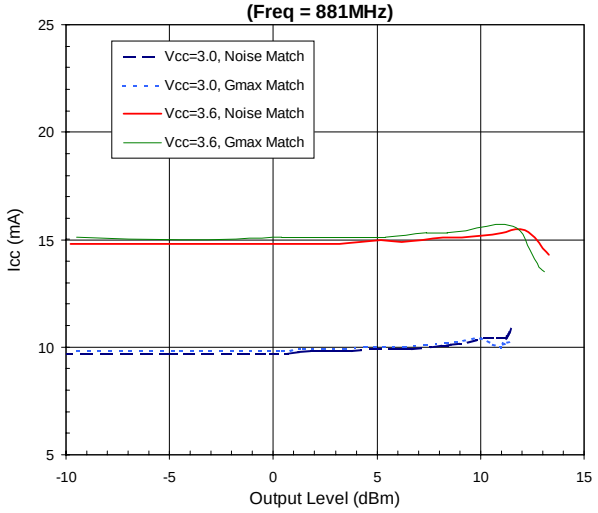
Output IM3 Level vs. Input Level (Freq = 881MHz)



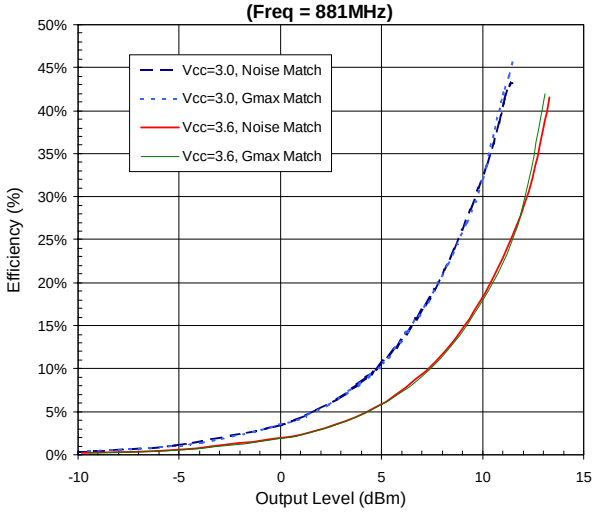
Power Out vs. Power In (Freq = 881MHz)



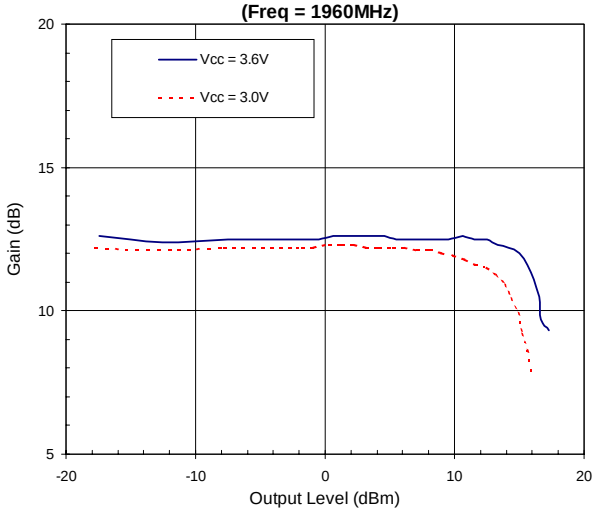
Icc vs. Output Level (Freq = 881MHz)



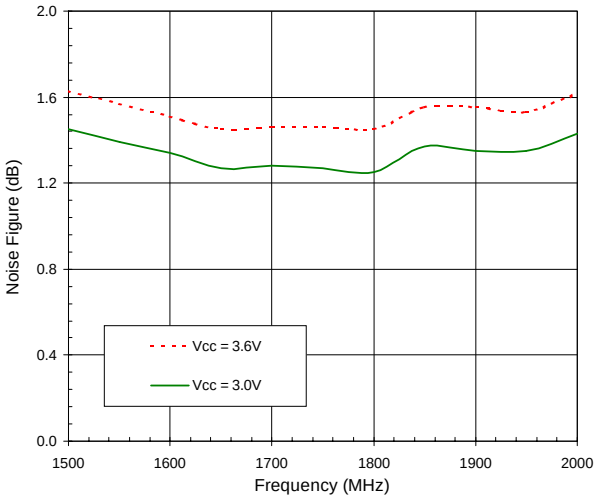
Efficiency vs. Output Level (Freq = 881MHz)



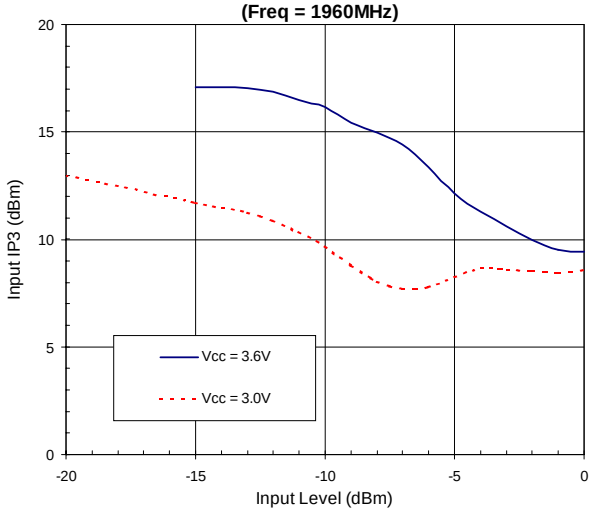
Gain vs. Output Level (Freq = 1960MHz)



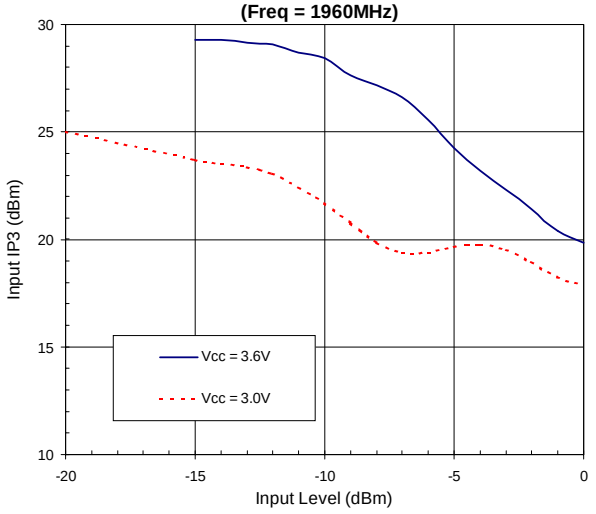
Noise Figure vs. Frequency



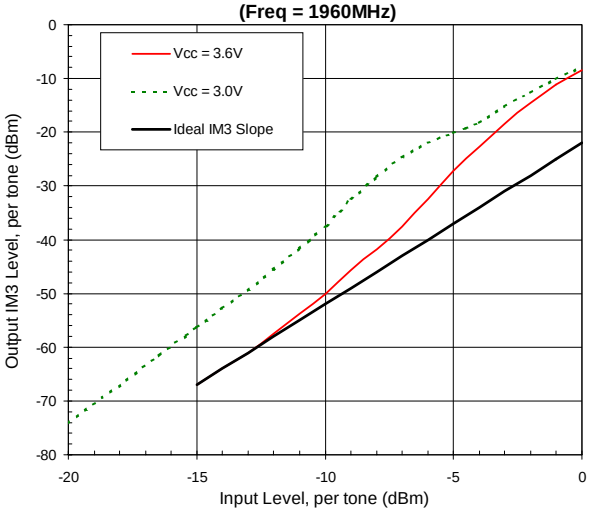
Input IP3 vs. Input Level (Freq = 1960MHz)



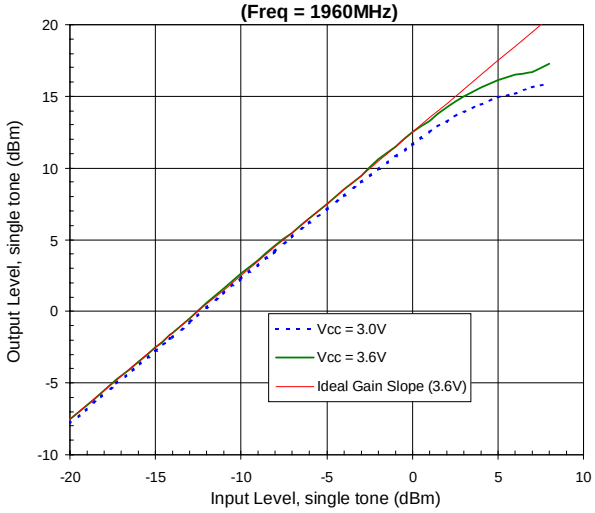
Output IP3 vs. Input Level (Freq = 1960MHz)



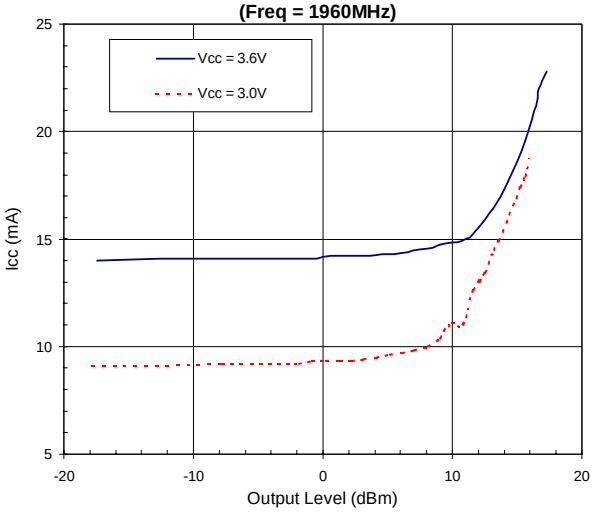
Output IM3 Level vs. Input Level (Freq = 1960MHz)



Power Out vs. Power In (Freq = 1960MHz)



Icc vs. Output Level (Freq = 1960MHz)



Efficiency vs. Output Level (Freq = 1960MHz)