# Preliminary

# RF2460

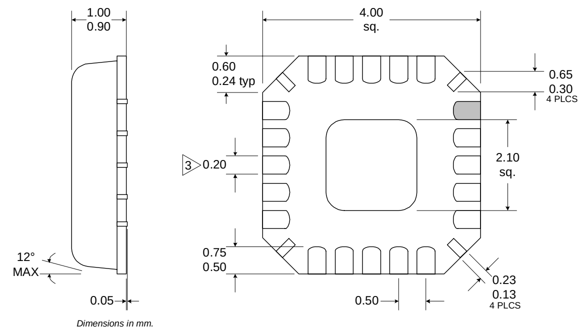
PCS CDMA LOW NOISE AMPLIFIER/MIXER
1500MHZ TO 2200MHZ DOWNCONVERTER

## Typical Applications

- CDMA PCS Handsets
- GPS Receiver
- W-CDMA Handsets
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

## Product Description

The RF2460 is a receiver front-end designed for the receive section of PCS CDMA and W-CDMA applications. It is designed to amplify and downconvert RF signals while providing 29dB of stepped gain control range and features digital control of LNA gain, mixer gain, and power down mode. A further feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. Noise Figure, IP3, and other specs are designed to be compatible with the IS-98B for CDMA PCS communications. The IC is manufactured on a SiGe HBT process and packaged in a 20-pin leadless chip carrier with an exposed die flag.

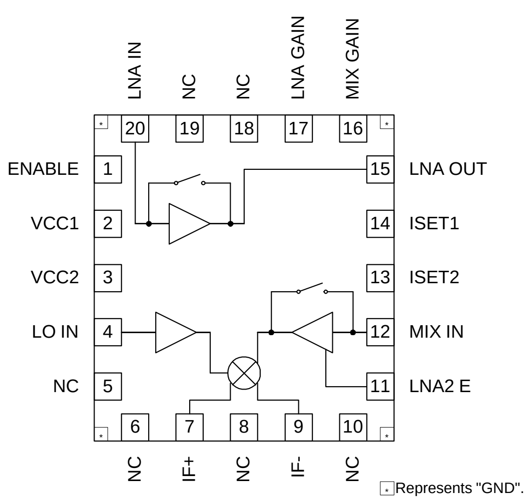



NOTES:
1 Shaded lead is Pin 1.
2 Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
3 Dimension applies to plated terminal: to be measured between 0.02 mm and 0.25 mm from terminal end.
4 Package Warpage: 0.05 mm max.
5 Die Thickness Allowable: 0.305 mm max.

Package Style: LCC, 20-Pin, 4x4

## Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☑ SiGe HBT
- ☐ Si CMOS




Functional Block Diagram

## Features

- Complete Receiver Front-End
- Stepped LNA/Mixer Gain Control
- Adjustable LNA/Mixer Bias Current
- 24dB Gain and 2.2dB Noise Figure at Maximum Cascade Gain

## Ordering Information

| | |
|---|---|
| RF2460 | PCS CDMA Low Noise Amplifier/Mixer 1500MHz to 2200MHz Downconverter |
| RF2460 PCBA | Fully Assembled Evaluation Board |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## Absolute Maximum Ratings

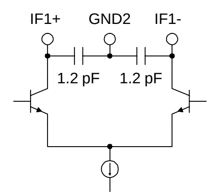
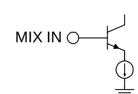
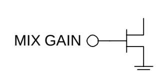
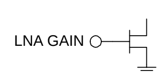
| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage | -0.5 to +5.0 | $V_{DC}$ |
| Input LO and RF Levels | +6 | dBm |
| Operating Ambient Temperature | -40 to +85 | °C |
| Storage Temperature | -40 to +150 | °C |

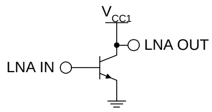
**Caution!** ESD sensitive device.



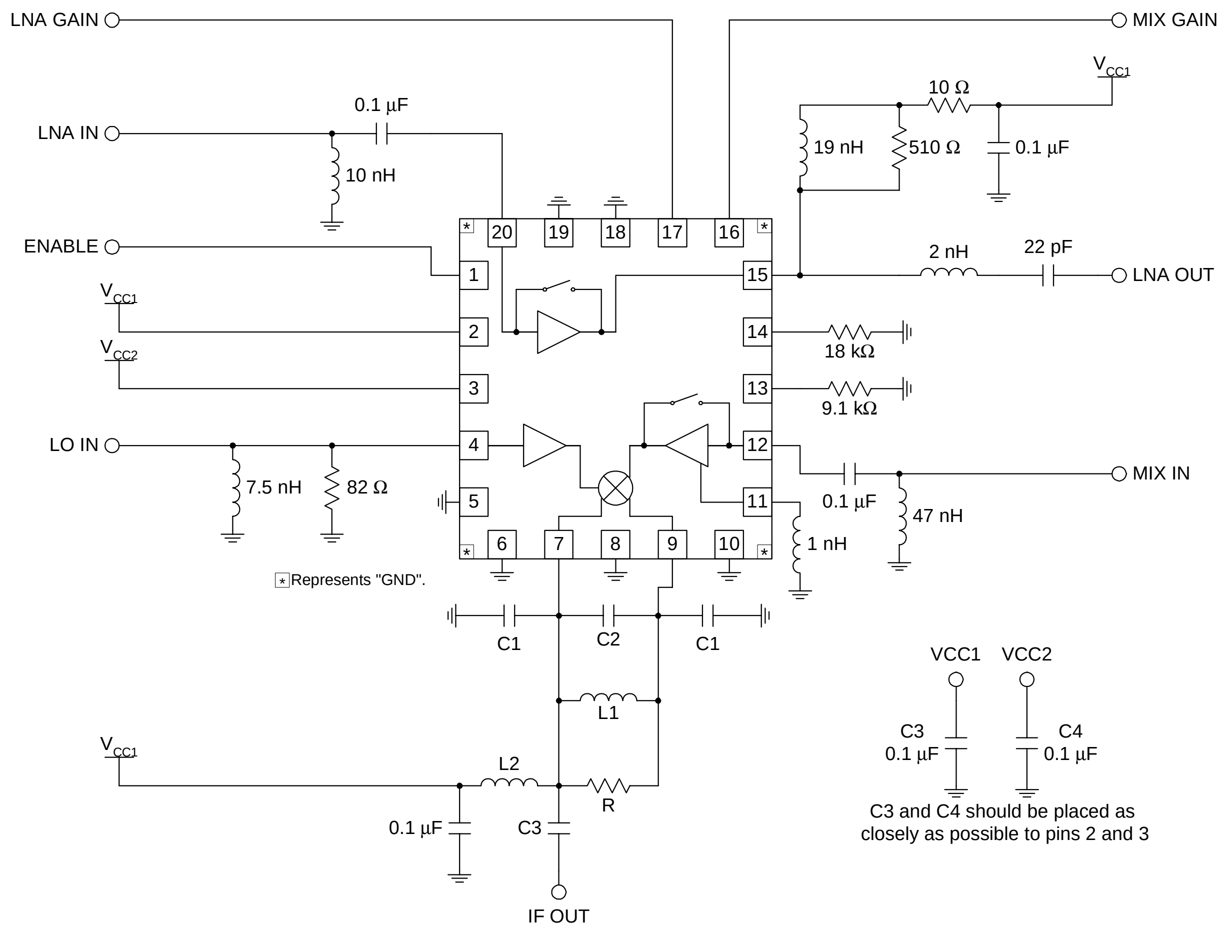
| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Overall** | | | | | T=25°C, $V_{CC}$=2.75V, RF=1.96GHz, LO=2170MHz@-7dBm, IF=210MHz |
| RF Frequency Range | | 1500 to 2200 | | MHz | |
| LO Frequency Range | | 1200 to 2600 | | MHz | |
| IF Frequency Range | | 0.1 to 250 | | MHz | |
| Bias Current | | 2.5 | 2.8 | mA | LNA, mixer and preamp for bias circuitry. |
| **LNA** | | | | | |
| Gain | 13.5 | 15.0 | | dB | |
| Noise Figure | | 1.4 | 1.8 | dB | |
| Input IP3 | +6.0 | +7.0 | | dBm | IIP3 is adjustable (see plots for setting). ISET1 (pin 14) external resistor sets current consumption and performance. |
| Input VSWR | | | 2:1 | | |
| Output VSWR | | | 2:1 | | |
| Current at Input IP3 | | 7 | 7.5 | mA | |
| **LNA Bypass** | | | | | |
| Gain | -6 | -5 | | dB | |
| Noise Figure | | 5 | 5.5 | dB | |
| Input IP3 | +23.0 | +26.0 | | dBm | |
| Input VSWR | | | 2:1 | | |
| Output VSWR | | | 2:1 | | |
| Current | | 0 | | mA | |
| **Mixer - High Gain Mode** | | | | | 1kΩ balanced load. |
| Gain | 10 | 12 | | dB | |
| Noise Figure | | 6.5 | 7.5 | dB | |
| Input IP3 | +3.0 | +4.0 | | dBm | IIP3 is adjustable (see plots for setting). |
| RF to IF Isolation | | >45 | | dB | ISET2 (pin 13) external resistor sets current consumption and performance. |
| Input VSWR | | | 2:1 | | |
| Output VSWR | | | 2:1 | | |
| Current | | 12 | 13 | mA | |
| **Mixer - Low Gain Mode** | | | | | 1kΩ balanced load. |
| Gain | 0 | 1.5 | | dB | |
| Noise Figure | | 15 | 16 | dB | |
| Input IP3 | +13.0 | +14.0 | | dBm | IIP3 is adjustable |
| RF to IF Isolation | | >45 | | dB | ISET2 (pin 13) external resistor sets current consumption and performance. |
| Input VSWR | | | 2:1 | | |
| Output VSWR | | | 2:1 | | |
| Current | | 7.5 | 8.0 | mA | |

| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **GPS - LNA** | | | | | |
| Gain | | 16 | | dB | |
| Noise Figure | | 1.4 | | dB | |
| Input IP3 | | +7.0 | | dBm | IIP3 is adjustable. ISET1 (pin 14) external resistor sets current consumption and performance. |
| Current at Input IP3 | | 7 | | mA | |
| **GPS - Mixer** | | | | | |
| Gain | | 17 | | dB | |
| Noise Figure | | 6 | | dB | |
| Input IP3 | | -5.0 | | dBm | IIP3 is adjustable. ISET1 (pin 14) external resistor sets current consumption and performance. |
| Current at Input IP3 | | 16 | | mA | |
| **GPS - Cascaded** | | | | | |
| Gain | | 31 | | dB | |
| Noise Figure | | 2.0 | | dB | |
| Input IP3 | | -1.0 | | dBm | IIP3 is adjustable. ISET1 (pin 14) external resistor sets current consumption and performance. |
| Current at Input IP3 | | 23 | | mA | |
| **Local Oscillator Input** | | | | | |
| Input Level | -10 | -7 | 0 | dBm | |
| LO to RF Isolation | | >40 | | dB | Any gain state. |
| LO to LNA Isolation | | >60 | | dB | Any gain state. |
| LO Current Buffer | | 4.5 | 5.0 | mA | $I_{CC2}$ when LO signal is present |
| **Cascade - LNA High/Mixer High** | | | | | LNA High Gain/Mixer High Gain<br>Assuming 3dB loss of filter |
| Gain | | 24 | | dB | IF 1, 1kΩ balanced load. |
| Noise Figure | | 2.2 | | dB | |
| Input IP3 | | -8.0 | | dBm | Single sideband. |
| Total Current | | 26 | | mA | |
| **Cascade - LNA High/Mixer Low** | | | | | LNA High Gain/Mixer Low Gain<br>Assuming 3dB loss of filter |
| Gain | | 13.5 | | dB | IF 1, 1kΩ balanced load. |
| Noise Figure | | 5.3 | | dB | |
| Input IP3 | | +1.0 | | dBm | Single sideband. |
| Total Current | | 21 | | mA | |
| **Cascade - LNA Low/Mixer High** | | | | | LNA Low Gain/Mixer High Gain<br>Assuming 3dB loss of filter |
| Gain | | 4 | | dB | IF 1, 1kΩ balanced load. |
| Noise Figure | | 14.5 | | dB | |
| Input IP3 | | +12.0 | | dB | Single sideband. |
| Total Current | | 19 | | mA | |
| **Cascade - LNA Low/Mixer Low** | | | | | LNA Low Gain/Mixer Low Gain<br>Assuming 3dB loss of filter |
| Gain | | -6.5 | | dB | IF 1, 1kΩ balanced load. |
| Noise Figure | | 23 | | dB | |
| Input IP3 | | +20.5 | | dB | Single sideband. |
| Total Current | | 14 | | mA | |
| **Power Supply** | | | | | |
| Voltage | 2.7 | 3.0 | 3.3 | V | |

| Pin | Function | Description | Interface Schematic |
|---|---|---|---|
| 1 | **ENABLE** | Power down pin. A logic “low” turns the part off. A logic “high” (>1.6V) turns the part on. | |
| 2 | **VCC1** | Supply Voltage for the LNA, mixer, bias, and logic circuitry. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. | See pin 20. |
| 3 | **VCC2** | Supply Voltage for the LO buffer amplifier. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. | |
| 4 | **LO IN** | Mixer LO Input Pin. | |
| 5 | **NC** | No connection. For isolation purposes, this pin is connected to the ground plane. | |
| 6 | **NC** | No connection. For isolation purposes, this pin is connected to the ground plane. | |
| 7 | **IF+** | CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to $V_{CC}$, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The part is designed to drive a 1kΩ load. Because this pin is biased to $V_{CC}$, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic. |   |
| 8 | **NC** | No connection. For isolation purposes, this pin is connected to the ground plane. | |
| 9 | **IF-** | Same as pin 7, except complementary output. | See pin 6. |
| 10 | **NC** | No connection. For isolation purposes, this pin is connected to the ground plane. | |
| 11 | **LNA2 E** | Emitter for LNA2. Increasing the inductance on this pin will reduce the mixer gain, increase IP3 and noise figure. | |
| 12 | **MIX IN** | Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance. |   |
| 13 | **ISET2** | This pin is used to set the bias current and IIP3 of the mixer amplifier using a resistor to ground. See plots for values and current settings. | |
| 14 | **ISET1** | This pin is used to set the bias current and IIP3 of the LNA amplifier using a resistor to ground. See plots for values and current settings. | |
| 15 | **LNA OUT** | LNA output pin. Open collector. | See pin 20. |
| 16 | **MIX GAIN** | CMOS compatible signal controlling mixer gain mode. Setting this signal high places the mixer in the high gain mode. Setting this signal low places the mixer in low gain mode by bypassing and shutting off the mixer buffer amplifier current. |   |
| 17 | **LNA GAIN** | CMOS compatible signal controlling LNA gain mode. Setting this signal high places the LNA in the high gain mode. Setting this signal low bypasses the LNA and shuts off the LNA bias current. |   |
| 18 | **NC** | No connection. For isolation purposes, this pin is connected to the ground plane. | |
| 19 | **NC** | No connection. For isolation purposes, this pin is connected to the ground plane. | |

| Pin | Function | Description | Interface Schematic |
|---|---|---|---|
| 20 | LNA IN | RF Input pin. This pin is internally matched for optimum noise figure from a 50Ω source. |  |
| Pkg Base | GND | Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. | |

# Application Schematic - US PCS




| | C1 (pF) | C2 (pF) | C3 (pF) | L1 (nH) | L2 (nH) | R (Ω) |
|---|---|---|---|---|---|---|
| US PCS, IF = 210 MHz | 4 | 3 | 6 | 82 | 110 | 4.7 k |
| Korean PCS, IF = 220 MHz | 3.6 | 2 | 7 | 82 | 120 | 4.7 k |
| GPS, IF = 184 MHz | 4 | 3 | 5 | 150 | 82 | 3 k |
| US PCS, IF = 184 MHz | 8 | 3 | 6 | 82 | 110 | 4.7 k |

# Output Interface Network of the Mixer

L1, C1, C2, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C_1 + 2C_2 + C_{EQ})}}$$

Where $C_{EQ}$ is the equivalent stray capacitance and capacitance looking into pins 7 and 9. An average value to use for $C_{EQ}$ is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where $R_{OUT}$ is the desired output impedance and $R_P$ is the parasitic equivalent parallel resistance of L1.

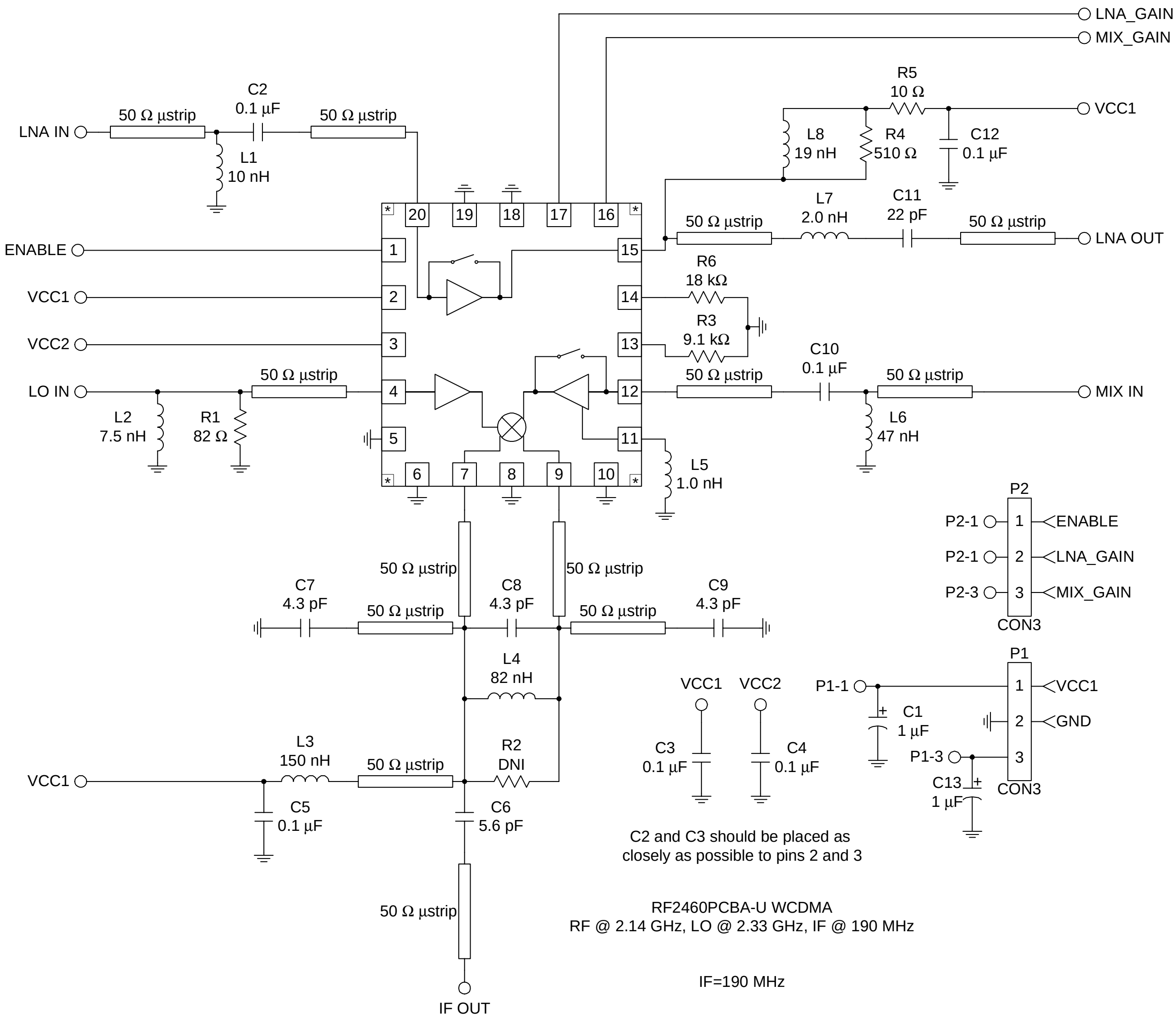
$C_2$ should first be set to 0 and C1 should be chosen as high as possible (suggested less than 20pF), while maintaining an $R_P$ of L1 that allows for the desired $R_{OUT}$. If the self-resonant frequencies of the selected C1 produce unsatisfactory linearity performance, their values may be reduced and compensated for by including C2 capacitor with a value chosen to maintain the desired $F_{IF}$ frequency.

L2 and C3 serve dual purposes. L2 serves as an output bias choke, and C3 serves as a series DC block.

In addition, L2 and C3 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to $R_{OUT}$. Otherwise, L2 is chosen to be large (suggested 120nH) and C3 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

# Application Schematic - W-CDMA

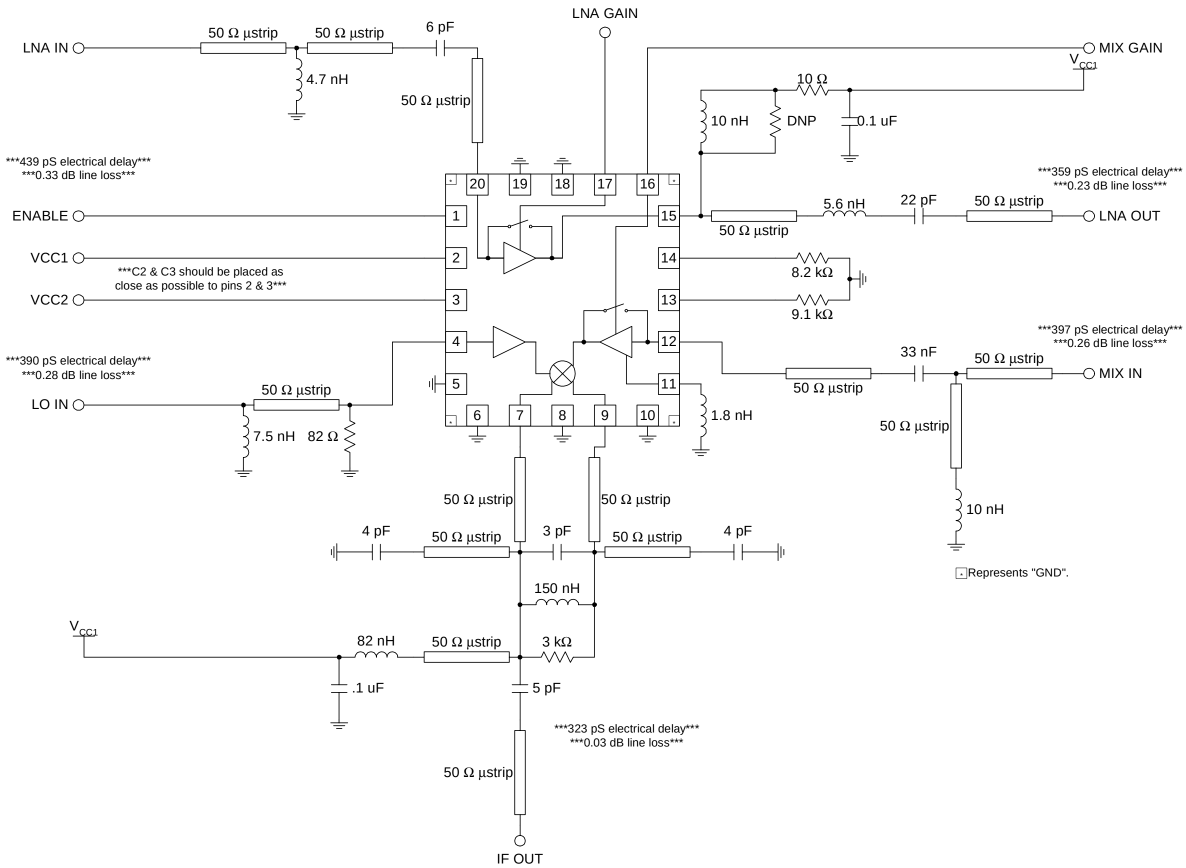
(See W-CDMA charts for lab measurements at the end of the data sheet)




8

FRONT-ENDS

# Application Schematic - GPS
## RF=1575MHz, IF=184MHz, LO=1759MHz

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FRONT-ENDS

# Current Measurement

To measure only the current of the different circuitry in the evaluation board, use the following procedure.

First, replace the bias choke inductor at the output of the mixer (L3 for US-PCS) with a 1Ω resistor. The voltage across the resistor will represent the mixer current. Terminate all SMA connections at 50Ω.

Second, follow the table below.

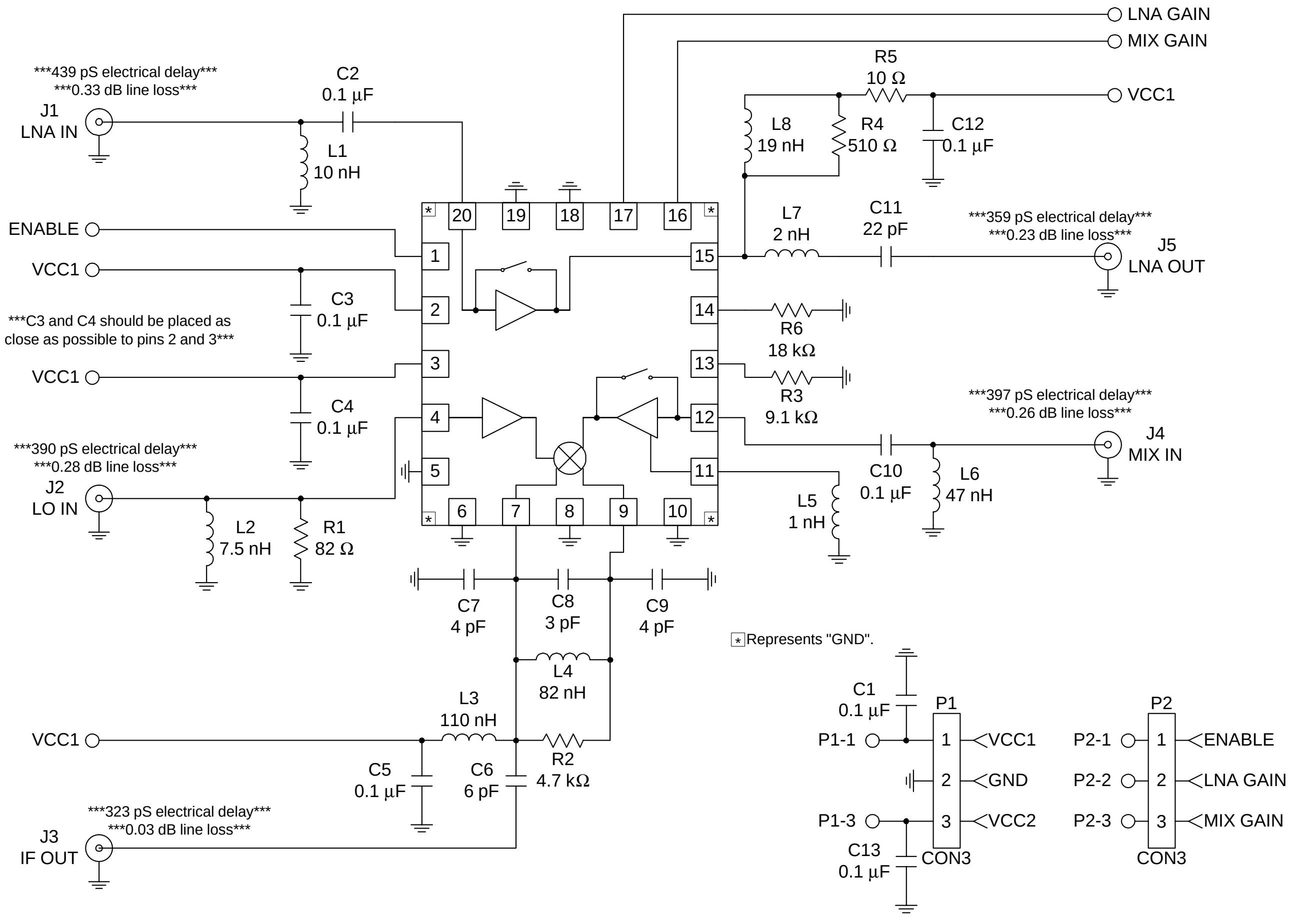
| | | CONDITION | | | | |
|---|---|---|---|---|---|---|
| | **Current (mA)** | $V_{CC1}$ | $V_{CC2}$ | **EN** | **LNA Gain** | **Mix Gain** |
| **$I_{CC}$ Total** | 25.82 | 1 | 1 | 1 | 1 | 1 |
| **LNA Off** | 18.77 | 1 | 1 | 1 | 0 | 1 |
| **Mixer Preamp Off** | 14.28 | 1 | 1 | 1 | 0 | 0 |
| **$V_{CC2}$ Off** | 10.05 | 1 | 0 | 1 | 0 | 0 |
| **Mixer Current** | 7.72 | 1 | 0 | 1 | 0 | 0 |

Therefore,

| | | | |
|---|---|---|---|
| LNA (Bypass) = | (Computer Simulation) | = | 0mA |
| LNA (High Gain) = | 25.82-18.77 | = | 7.05mA |
| Mixer (Preamp) = | 18.77-14.28 | = | 4.49mA |
| Mixer = | (Measured) | = | 7.70mA |
| Bias = | 10.05-7.7 | = | 2.35mA |
| LO Circuitry ($V_{CC2}$) = | 14.28-10.05 | = | 4.23mA |
| | | | 25.82mA |

# Evaluation Board Schematic
## US-PCS, IF=210MHz

(Download Bill of Materials from www.rfmd.com.)

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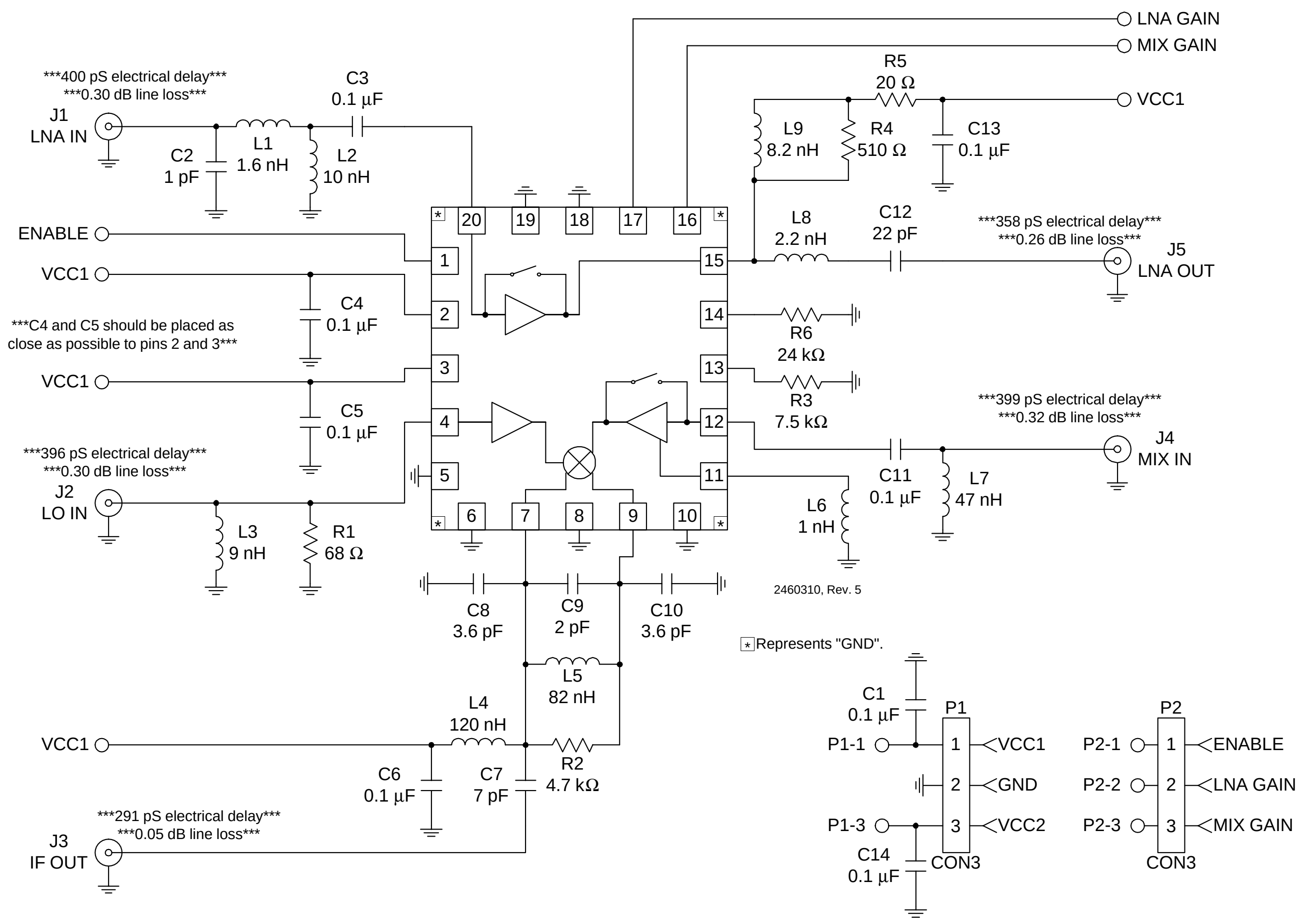
FRONT-ENDS

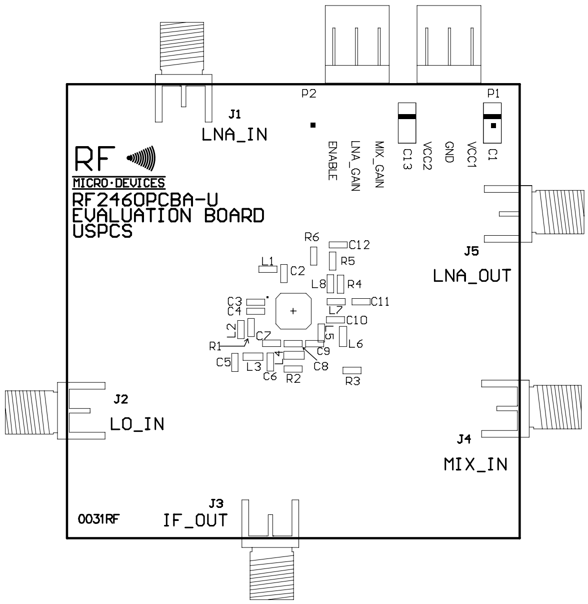
# Evaluation Board Schematic
## Korean-PCS, IF=220MHz



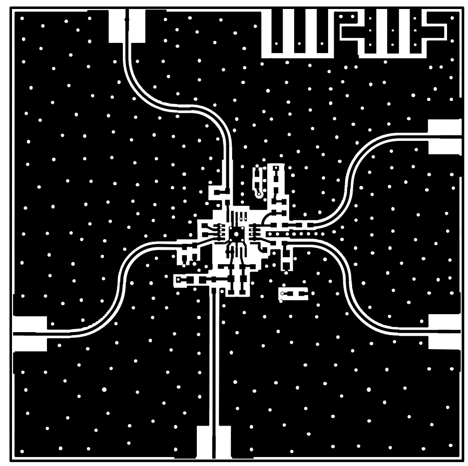
# Evaluation Board Layout - US PCS
## Board Size 2.0" x 2.0"

Board Thickness 0.034”, Board Material FR-4, Multi-Layer

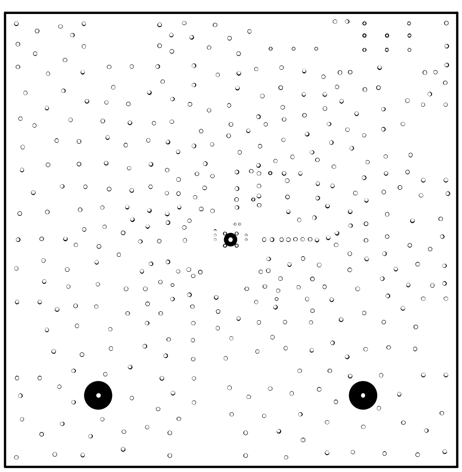
Assembly



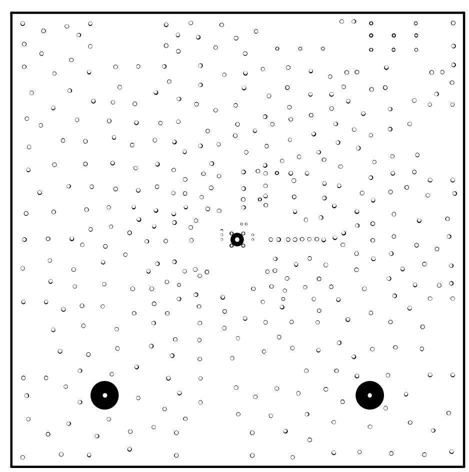

Top



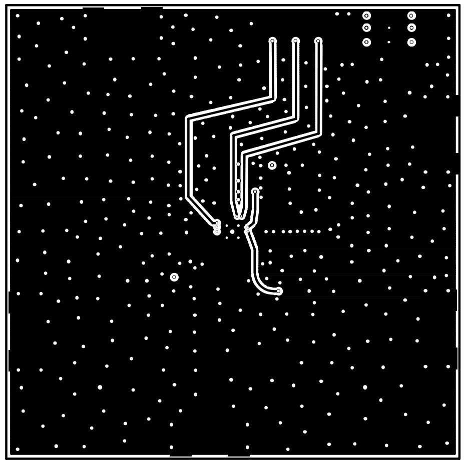
Power Plane 1



Power Plane 2

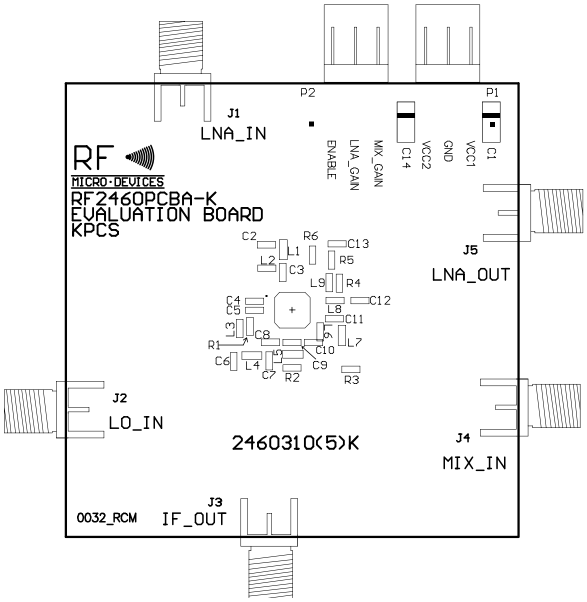


Back

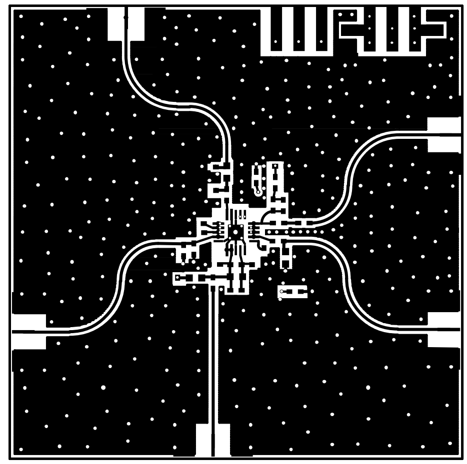


# Evaluation Board Layout - Korean PCS

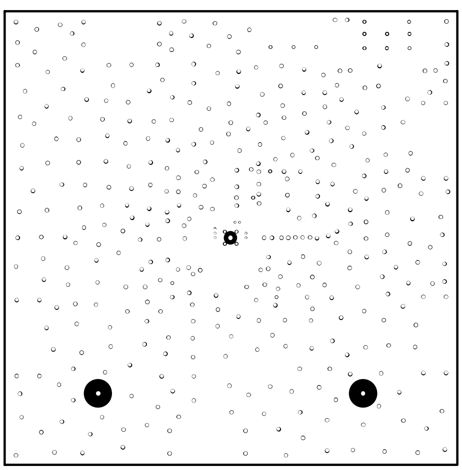
Assembly



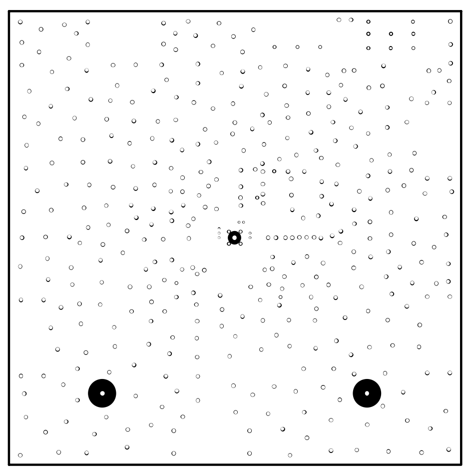

Top



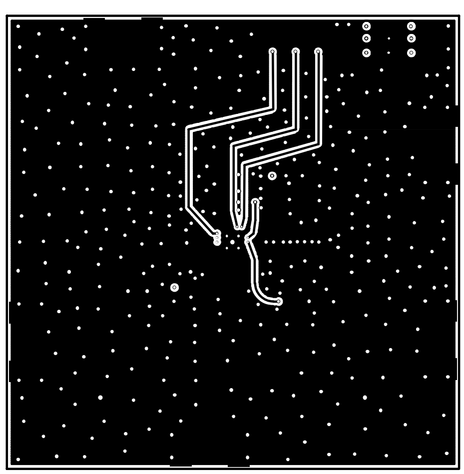
Power Plane 1



Power Plane 2

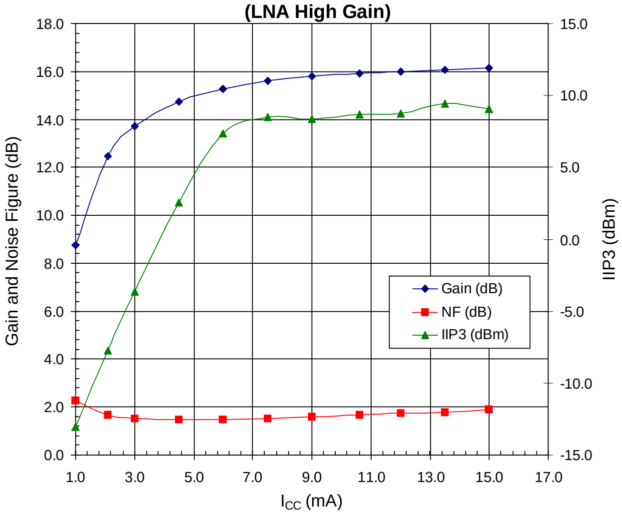


Back

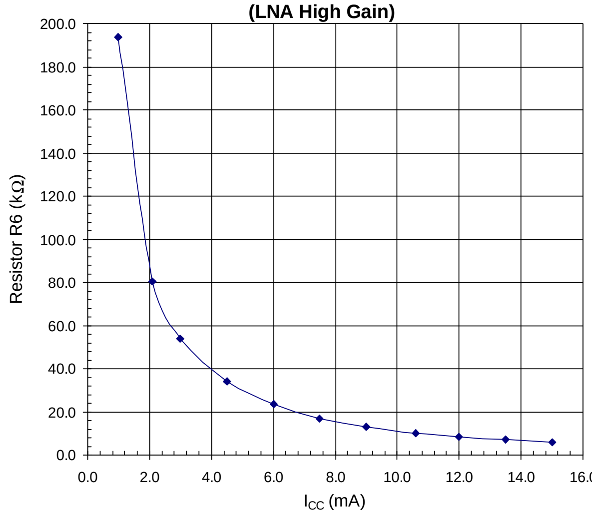


## US-PCS

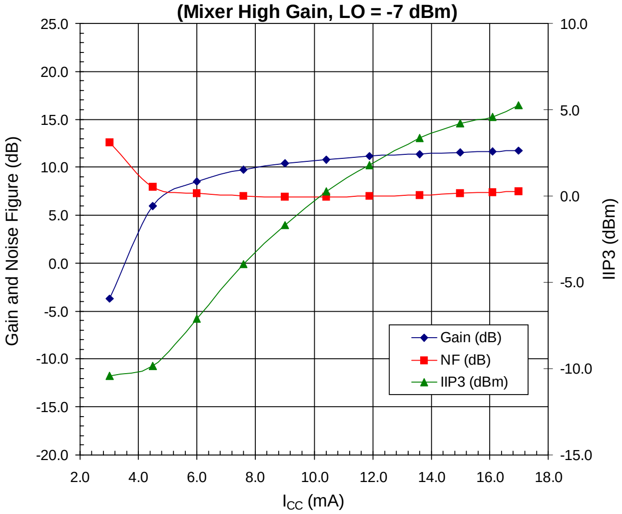
**LNA Gain, Noise Figure and IIP3 versus $I_{CC}$ - LNA Only (LNA High Gain)**



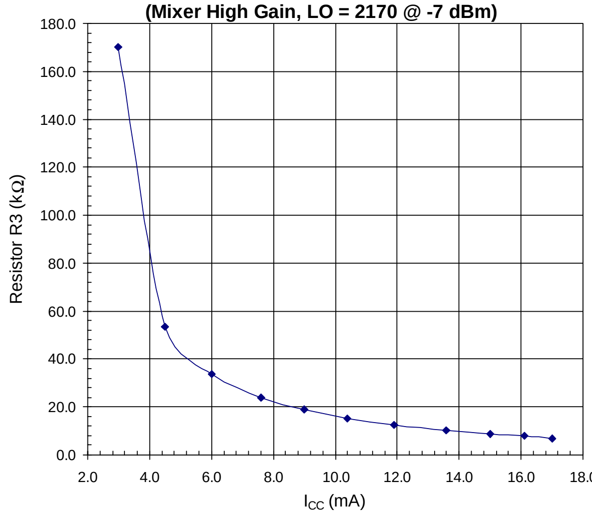

**Resistor (R6) versus $I_{CC}$ (mA) - LNA Only (LNA High Gain)**




**Mixer Gain, Noise Figure and IIP3 versus $I_{CC}$ - Mixer (Mixer High Gain, LO = -7 dBm)**




**Resistor (R3) versus $I_{CC}$ - Mixer (Mixer High Gain, LO = 2170 @ -7 dBm)**




**Special Instructions** (Board loss, taking into consideration description in the schematic)

LNA

$V_{CC1}$=$V_{CC2}$=Enable=2.75V; Mix Gain=0.0V

To measure $I_{CC}$ LNA only:

LNA Gain was switched between 0V and 2.75V, and record the delta current.

Mixer

$V_{CC1}$=$V_{CC2}$=Enable=Mix Gain=2.75V; LNA Gain=0.0V

To measure $I_{CC}$ Mixer (LNA should be in bypass mode and LO signal should be present):

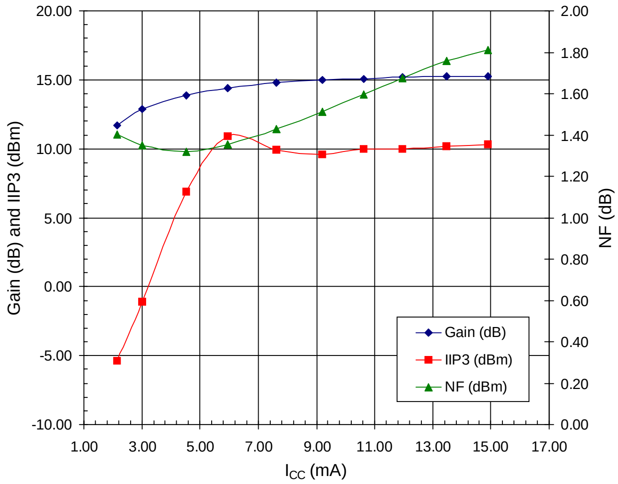
Total mixer current=$I_{CC1}$

$V_{CC2}$ only affects LO current buffer and R6 doesn't affect the mixer current.

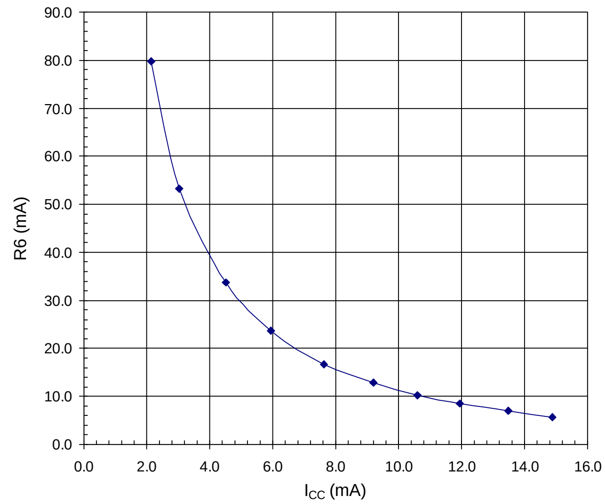
**W-CDMA**

(See W-CDMA Application Schematic)

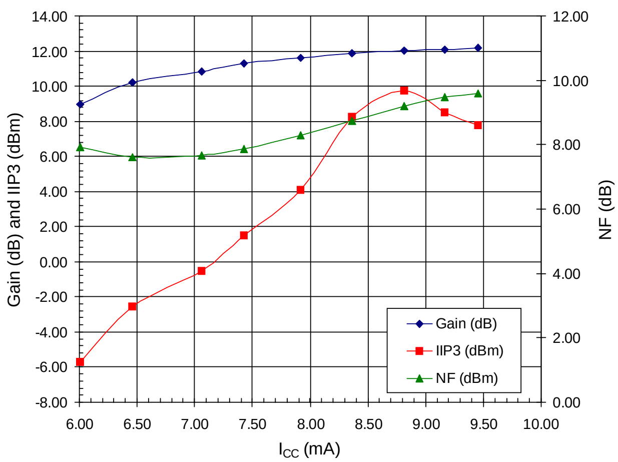
**LNA Gain, Noise Figure, and IIP3 versus $I_{CC}$ - LNA Only (LNA High Gain)**



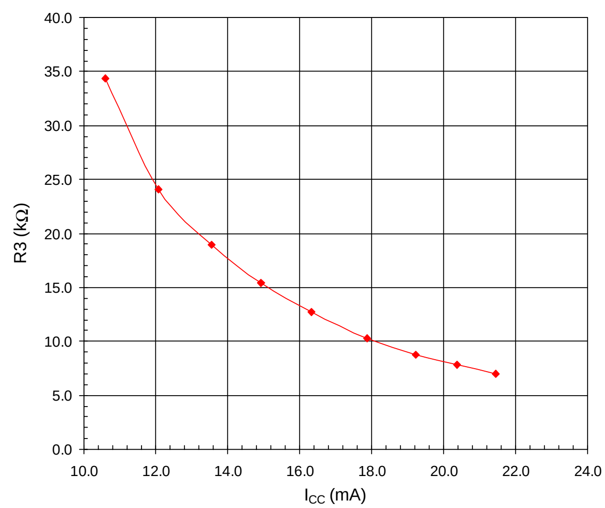

**R6 versus $I_{CC}$ for LNA**




**Mixer Gain, Noise Figure and IIP3 versus $I_{CC}$ - Mixer and Bias Circuits (Mixer High Gain, LO=-7dBm)**




**R3 versus $I_{CC}$ for Mixer and Bias Circuits**




**Instructions** (Board loss, taking into consideration description in the W-CDMA schematic)

<u>LNA</u>

$I_{CC}$ LNA current=total current ($V_{CC}$=LNA Gain=2.75)-total current ($V_{CC}$=2.75; LNA Gain=0)

To measure $I_{CC}$ LNA only:

LNA Gain was switched between 0V and 2.75V, and record the delta current.

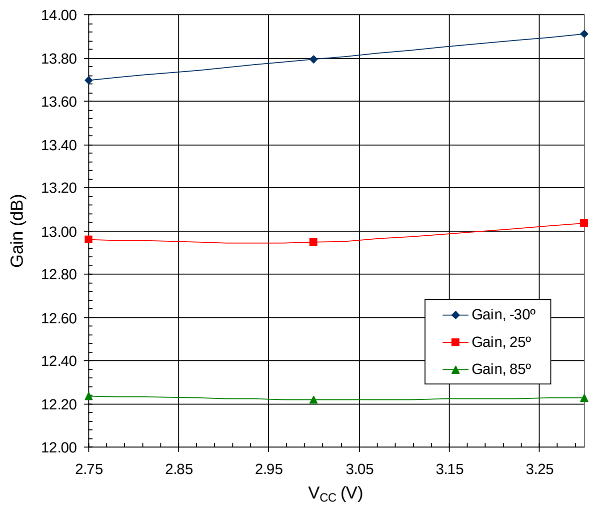
<u>Mixer</u>

$I_{CC}$ Mix and bias current=total current ($V_{CC}$;=EN=$V_{CC2}$=Mix Gain=2.75; LNA Gain=0)-total current ($V_{CC}$;=EN=2.75; Mix Gain=LNA Gain=$V_{CC2}$=0

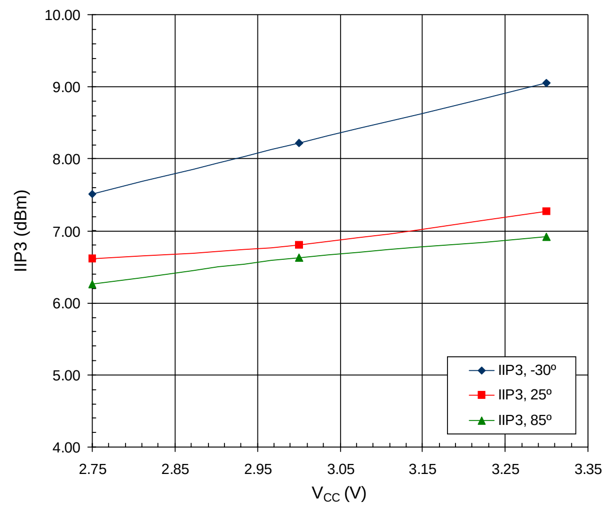
LO signal should be present. $V_{CC2}$ only affects LO current buffer and R6 doesn't affect the mixer current.

By using a R6=39kΩ and R3=24kΩ, the following results were obtained. RF=2140MHz, LO=2330MHz, IF=190MHz.

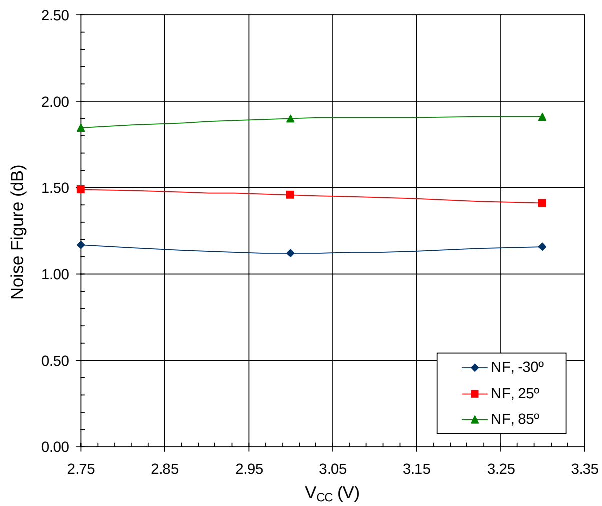
**LNA (High Gain Mode) WCDMA**



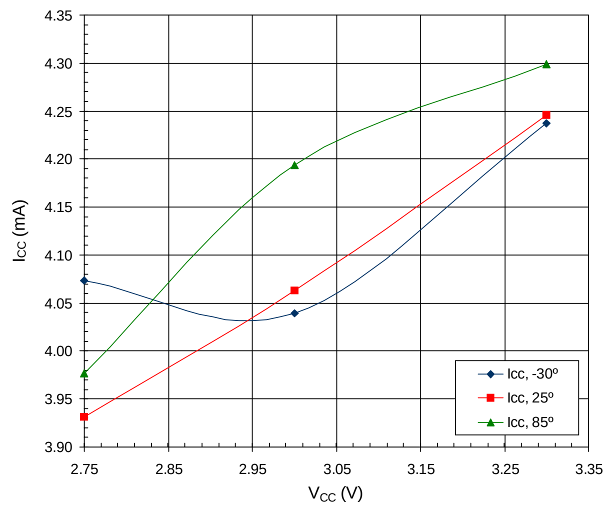

**LNA (High Gain Mode) W-CDMA**




**LNA (High Gain Mode) W-CDMA**



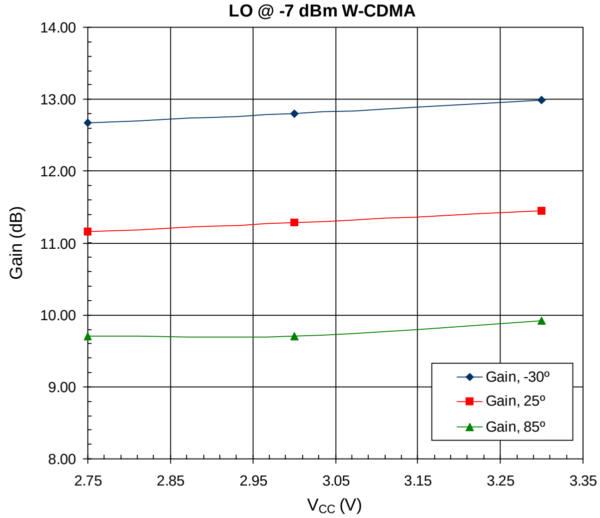

**LNA Current W-CDMA**



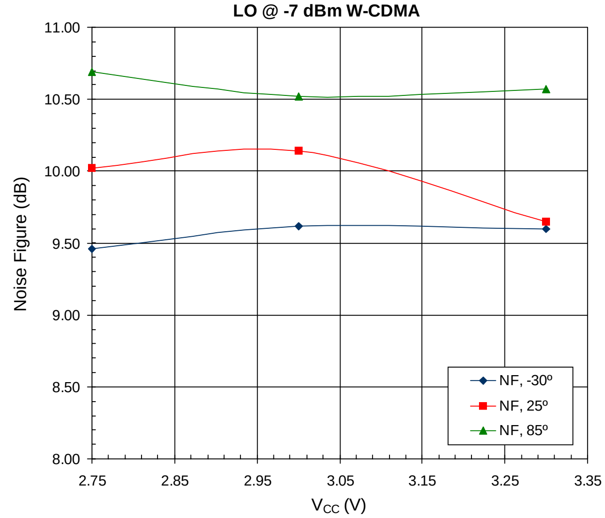

8

FRONT-ENDS

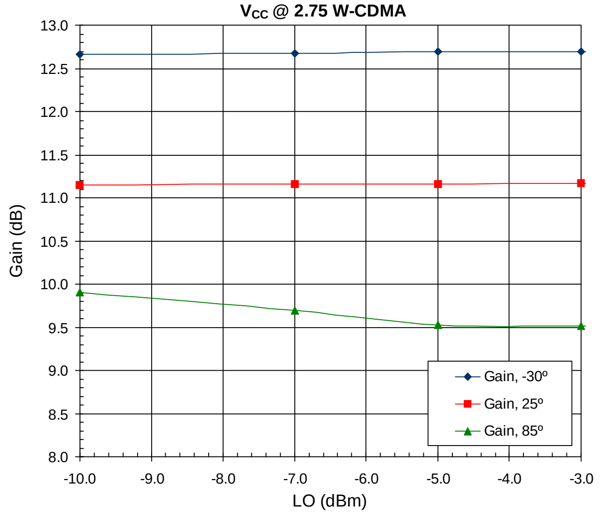
**Mixer High Gain Mode,**
**LO @ -7 dBm W-CDMA**



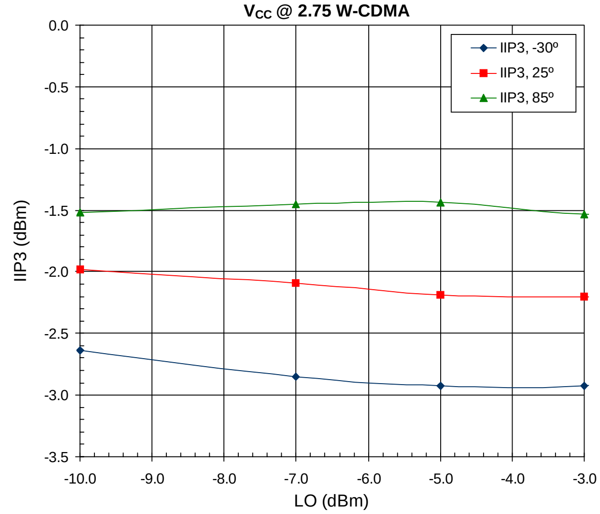

**Mixer High Gain Mode,**
**LO @ -7 dBm W-CDMA**



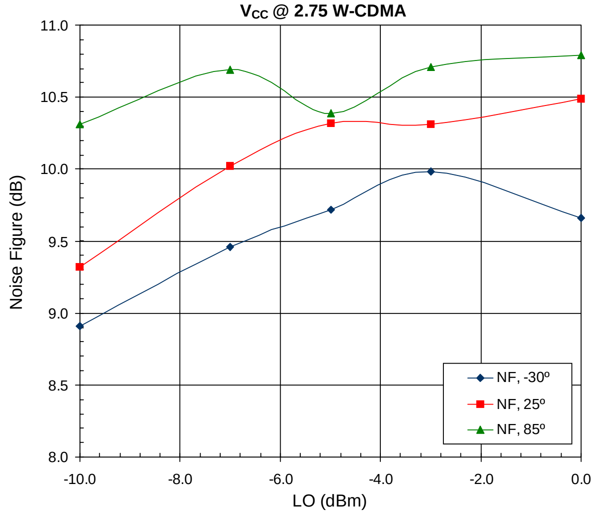

**Mixer High Gain Mode,**
**$V_{CC}$ @ 2.75 W-CDMA**



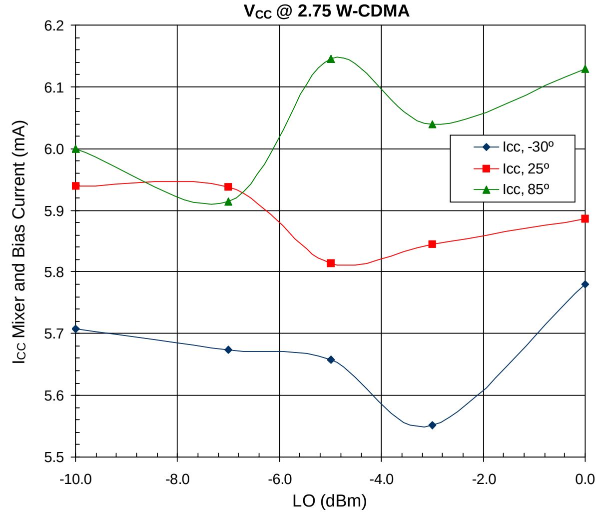

**Mixer IF High Gain Mode,**
**$V_{CC}$ @ 2.75 W-CDMA**

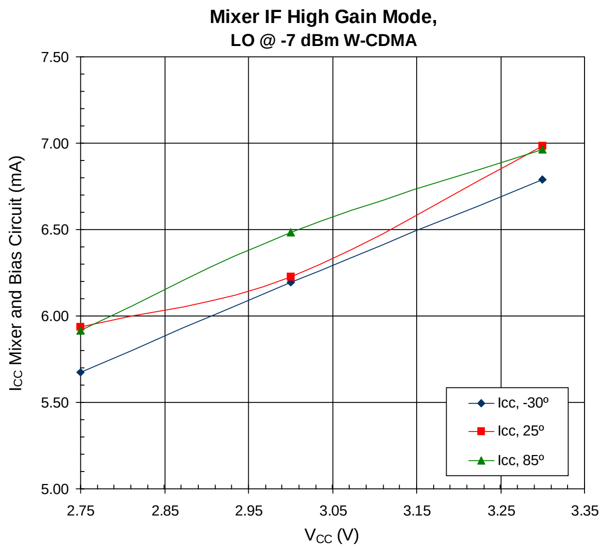



**Mixer IF High Gain Mode,**
**$V_{CC}$ @ 2.75 W-CDMA**




**Mixer IF High Gain Mode,**
**$V_{CC}$ @ 2.75 W-CDMA**




Mixer IF High Gain Mode,
LO @ -7 dBm W-CDMA
ICC Mixer and Bias Circuit (mA)
VCC (V)
7.50
7.00
6.50
6.00
5.50
5.00
2.75
2.85
2.95
3.05
3.15
3.25
3.35
Icc, -30º
Icc, 25º
Icc, 85º