RF2513

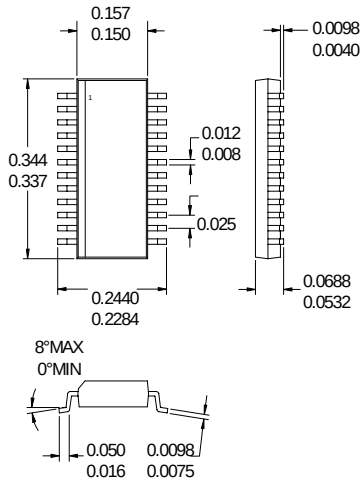
UHF TRANSMITTER

Typical Applications

- Single- or Dual-Channel LO Source
- FM/FSK Transmitter
- Wireless Data Transmitters
- 433/868/915MHz ISM Band Systems
- Wireless Security Systems

Product Description

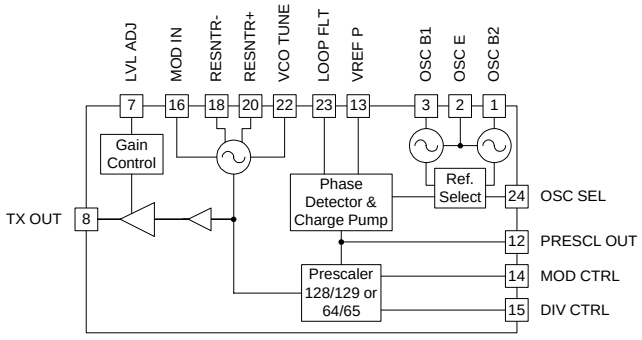
The RF2513 is a monolithic integrated circuit intended for use as a low-cost frequency synthesizer and transmitter. The device is provided in a 24 pin SSOP package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in FM or FSK applications in the U.S. 915MHz ISM band and European 433MHz or 868MHz ISM band. The integrated VCO, dual-modulus/dual-divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator. A second reference oscillator is available to support two channel applications.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS
- [ ] SiGe HBT
- [ ] Si CMOS



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- 10mW Output Power at 433MHz
- 2.7V to 5.0V Supply Voltage
- Low Current and Power Down Capability
- 300MHz to 1000MHz Frequency Range
- Narrowband and Wideband FM

Ordering Information

RF2513	UHF Transmitter
RF2513 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2513 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2513 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
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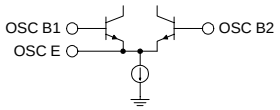
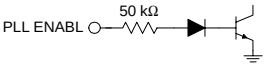
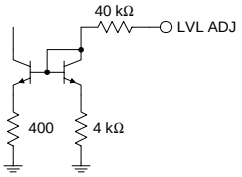
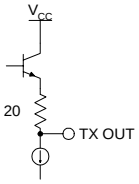
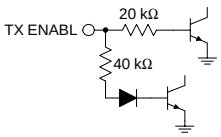
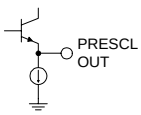
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

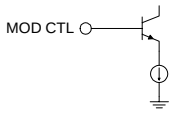
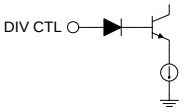
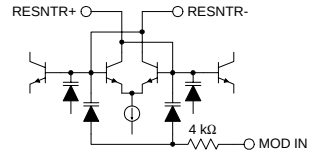
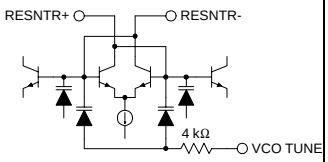
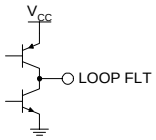
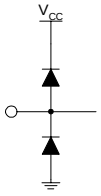
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		300 to 1000		MHz	
Modulation		FM/FSK			
Modulation Frequency			2	MHz	
Maximum FM Deviation	200			kHz	Dependent upon Supply Voltage
PLL and Prescaler					
Prescaler Divide Ratio		64/65 or 128/129			
PLL Lock TIme		4/PLL BW		ms	The PLL lock time, from power up, is set externally by the bandwidth of the loop filter.
PLL Phase Noise		-72		dBc/Hz	10kHz Offset, 10kHz loop bandwidth
		-95		dBc/Hz	100kHz Offset, 10kHz loop bandwidth
Reference Frequency			17	MHz	
Max Crystal R_S	TBD		100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Maximum Power Level	+3	+8		dBm	Freq=433MHz
		+2		dBm	Freq=915MHz
Power Control Range	15			dB	
Power Control Sensitivity		10		dB/V	
Antenna Port Impedance		50		Ω	TX ENABL="1"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Power Down Control					
Logic Controls "ON"	2.0			V	Voltage supplied to the input; device is "ON"
Logic Controls "OFF"			1.0	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	25			kΩ	
Turn On Time			5 + 4/PLL BW	ms	From Change in OSC SEL,7.075MHz XTAL
Turn Off Time			4	ms	From Change in OSC SEL,7.075MHz XTAL
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		27		mA	TX Mode, LVL ADJ=3.6V
		10		mA	TX Mode, LVL ADJ=0V
		8		mA	PLL Only
			1	µA	LVL ADJ=0V, PLL ENABL=0V, TX ENABL=0V, OSC SEL=0V

Pin	Function	Description	Interface Schematic
1	OSC B2	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 1 and pin 2.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. An appropriate capacitor as chosen by the customer should be connected from this pin to ground.	See pin 1.
3	OSC B1	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 3 and pin 2.	See pin 1.
4	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
5	GND1	Ground connection for the PA buffer amp. Keep traces physically short and connect immediately to ground plane for best performance.	
6	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
7	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
8	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
9	GND2	Ground connection for the Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
10	VCC1	This pin is used to supply DC bias to the PA buffer amp. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
11	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
12	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
13	VREF P	Bias voltage reference pin for bypassing the prescaler and phase detector. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin.	

Pin	Function	Description	Interface Schematic
14	MOD CTRL	This pin is used to select the prescaler modulus. A logic “high” selects 64 or 128 for the prescaler divisor. A logic “low” selects 65 or 129 for the prescaler divisor.	
15	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic “high” selects the 64/65 divisor. A logic low selects the 128/129 divisor.	
16	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. Because the modulation varactors are part of the resonator tank, the deviation is slightly dependent upon the components used in the external tank.	See pin 18.
17	VCC2	This pin is used to is supply DC bias to the VCO, prescaler, and PLL.	
18	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 20.	
19	NC	Not internally connected.	
20	RESNTR+	See pin 18.	See pin 18.
21	GND3	GND is the ground shared on chip by the VCO, prescaler, and PLL electronics. Keep traces physically short and connect immediately to ground plane for best performance.	
22	VCO TUNE	Loop filter input to VCO.	
23	LOOP FLT OUT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth.	
24	OSC SEL	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1-3, 9, 10,12-15, 17, 21-23.	

RF2513 Theory of Operation

Introduction

The RF2513 is a low-cost FM/FSK UHF transmitter designed for applications operating within the 300MHz to 1000MHz frequency range. It is particularly intended for 315/433/868MHz band systems, remote keyless entry systems, and FCC Part 15.231 periodic transmitters. It can also be used as a single- or dual-channel local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop.

The RF2513 is provided in a 24-pin SSOP-24 package and is designed to operate from a supply voltage ranging from 2.2V to 5.0V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to 10mW output power into a 50Ω load (+10dBm) and is intended to comply with FCC requirements for unlicensed remote control transmitters.

RF2513 Functional Blocks

A PLL consists of a reference oscillator, phase detector, loop filter, voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2513 includes all of these internally, except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillators** are Colpitts type oscillators. Pins 1 (OSC B2), 2 (OSC E), and 3 (OSC B1) provide connections to the internal transistors used as reference oscillators. The Colpitts configuration is a low parts-count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of either transistor. In either case, the drive level should be around $500mV_{PP}$. This level prevents overdriving the device and keeps phase noise and reference spurs minimal.

The user sets which oscillator is operational by setting pin 24 (OSC SEL) either high or low. This allows the implementation of two channel systems.

The **prescaler** divides the Voltage Controlled Oscillator (VCO) frequency down by either 64/65 or 128/129, using a series of flip-flops, depending upon the logic level present at pin 15 (DIV CTRL). A high logic level will select the 64/65 divisor. A low logic level will select the 128/129 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

In addition to the DIV CTRL setting, one also sets the prescaler modulus by setting pin 14 (MOD CTRL) either high or low. A high logic level will select the 64/128 divisor. A low logic level will select the 65/129 divisor.

Pin 12 (PRESCL OUT) provides access to the prescaler output. This is used for interfacing to an external PLL IC.

The RF2513 contains an onboard phase detector and charge pump. The **phase detector** compares the phase of the reference oscillator to the phase of the VCO. The phase detector is implemented using flip-flops in a topology referred to as either "digital phase/frequency detector" or "digital tri-state comparator". The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency.

When both inputs of the flip-flops are identical, the signals are both frequency and phase locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter or enter into a high impedance state. This is where the name "tri-state comparator" comes from.

The main benefit of this type of detector it's ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it will use the frequency error for correction. This type of detector will lock under all conditions.

The prescaler and the phase detector bias voltage is brought out through pin 13 (VREF P). This allows bypassing of the of these two circuits to filter the reference crystal frequency.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. It's inputs are the outputs of the phase detector flip-flops. Since there are two flip-flops, there are four possible states. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. The state where both inputs are high will not occur. The other states are either charging or discharging the loop filter. The loop filter integrates the pulses coming from

the charge pump to create a control voltage for the voltage controlled oscillator.

The **voltage controlled oscillator (VCO)** is a tuned differential amplifier with the bases and collectors cross-coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors. It is comprised of internal varactors and two external inductors. The designer selects the inductors for the desired frequency of operation. These inductors also provide DC bias for the VCO. The output of the VCO is buffered and applied to the prescaler circuit, where it is divided down and compared to the reference oscillator frequency.

The PLL and VCO circuitry can be enabled by setting applying a “high” logic level to pin 4 (PLL ENABL). Conversely, the PLL and VCO circuitry will be turned off if the level is tied “low”.

The **transmit amplifier** is a two stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 8dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The output power is adjustable by the setting of pin 7 (LVL ADJ). This analog input allows the designer a 15dB range of output power. As the LVL ADJ voltage is reduced, the output power and current consumption are reduced. LVL ADJ must be low when the transmitter is disabled.

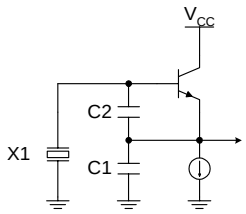
Additionally, the transmitter circuitry can be disabled entirely by applying a “low” logic level to pin 11 (TX ENABL). During transmission, this pin should be tied “high”. This pin controls all circuitry except for the PLL circuitry.

During transmission the transmitter is enabled and the impedance of the output pin, pin 8 (TX OUT), is low. When the transmitter is not enabled, the impedance becomes high.

The RF2513 contains onboard band gap reference voltage circuitry which provides a stable **DC bias** over varying temperature and supply voltages.

Designing with the RF2513

The **reference oscillator** is built around the onboard transistor at pins 1, 2 and 3. The intended topology is of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low cost solutions. The topology of this type of oscillator is as seen in the following figure.



This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C_1 and C_2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations.

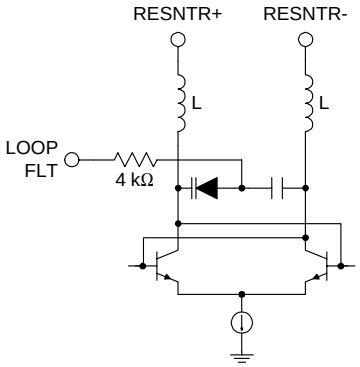
$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

The load capacitance is usually 32pF. The variable *freq* is the oscillator frequency in MHz. The frequency can be adjusted by either changing C_2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at pin 2 (OSC E). It has been found that the level at this pin should generally be around 500mV_{PP} or less. This will reduce the reference spur levels and reduce noise from distortion. If this level is higher than 500mV_{PP} then decrease the value of C_1. The values of these capacitors are usually tweaked during design to meet performance goals, such as minimizing the start-up time.

Additionally, by placing a variable capacitor in series with the crystal, one is able to adjust the frequency. This will also alter the drive level, so it should be checked again.

An important part of the overall design is the voltage controlled oscillator (VCO). The VCO is configured as a differential amplifier. The VCO is tuned via the external inductors, capacitor and varactor. The varactor capacitance is set by the loop filter output voltage through a 4kΩ resistor.



To tune the VCO the designer only needs to calculate the value of the inductors connected to pins 18 and 20 (RESNTR- and RESNTR+). The inductor value is determined by the following equation.

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C} \cdot \frac{1}{2}$$

In this equation, *f* is the desired operating frequency and *L* is the value of the inductor required. The value *C* is the amount of capacitance presented by the varactor, capacitor and parasitics. The factor of one half is due to the inductors being in each leg.

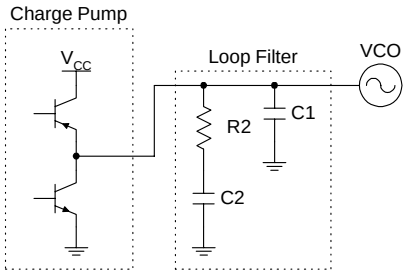
The setup of the VCO can be summarized as follows. First, open the loop. Next, get the VCO to run on the desired frequency by selecting the proper inductor and capacitor values. The capacitor value will need to include the varactor and circuit parasitics. After the VCO is running at the desired frequency, then set the VCO sensitivity.

The sensitivity is determined by connecting the control voltage input point to ground and noting the frequency. Then connect the same point to the supply and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sensitivity expressed in Hz/V. Increasing the inductor value while decreasing the capacitor value will increase the sensitivity. Decreasing the inductor value while increasing the capacitor value will lower the sensitivity.

When increasing or decreasing component values, make sure that the center frequency remains constant. Finally, close the loop.

External to the part, the designer needs to implement a **loop filter** to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through an internal 4kΩ resistor. The loop filter is then connected in parallel to this point at pin 23 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC. A passive filter is most common, as it is a low cost and low noise design. An additional pole could be used for reducing the reference spurs, however there is not a way to add the series resistor. This should not be a reason for concern however.

The schematic of the loop filter is as follows.



The transfer function is

$$F(s) = R_2 \cdot \left[\frac{s \cdot \tau_2 + 1}{s \cdot \tau_2 \cdot (s \cdot \tau_1 + 1)}\right]$$

where the time constants are defined as

$$\tau_2 = R_2 \cdot C_2 \quad \text{and} \quad \tau_1 = R_2 \cdot \left[\frac{C_1 \cdot C_2}{C_1 + C_2}\right]$$

The frequency at which unity gain occurs is given by

$$\omega_{LBW} = \frac{1}{\sqrt{\tau_1 \cdot \tau_2}}$$

This is also the loop bandwidth.

If the phase margin (PM) and the loop bandwidth (ω_{LBW}) are known, it is possible to calculate the time constants. These are found using the following equations.

$$\tau_1 = \frac{\sec(PM) - \tan(PM)}{\omega_{LBW}} \quad \text{and} \quad \tau_2 = \frac{1}{\omega^2_{LBW} \cdot \tau_1}$$

With these known, it is then possible to determine the values of the filter components.

$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_{PD} \cdot K_{VCO}}{\omega^2_{LBW} \cdot N} \cdot \sqrt{\frac{1 + (\omega_{LBW} \cdot \tau_2)^2}{1 + (\omega_{LBW} \cdot \tau_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1\right)$$

$$R_2 = \frac{\tau_2}{C_2}$$

As an example, consider a loop bandwidth of 50kHz, a phase margin of 45°, a divide ratio of 64, a K_{VCO} of 20MHz/V, and a K_{PD} of 0.01592mA/2πrad. Time constant τ_1 is 1.31848µs, time constant τ_2 is 7.68468µs, C_1 is 131.15pF, C_2 is 633.26pF, and R_2 is 12.14kΩ.

In order to perform these calculations, one will need to know the value of two constants, K_{VCO} and K_{PD}. K_{PD} is calculated by dividing the charge pump current by 2π. For the RF2513, the charge pump current is 40µA. K_{VCO} is best found empirically as it will change with frequency and board parasitics. By briefly connecting pin 23 (LOOP FLT) to VCC and then to ground, the frequency tuning range of the VCO can be seen. Dividing the difference between these two frequencies by the difference in the voltage gives K_{VCO} in MHz/V.

The control lines provide an **interface** for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 16 (MOD IN), pin 15 (DIV CTRL), pin 14 (MOD CTRL), pin 24 (OSC SEL), and pin 7 (LVL ADJ) as control pins whose voltage level can be set.

General **RF bypassing** techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias for connection to the ground plane allows one to connect to ground as close as possible to ground pins. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

Pre-compliance testing should be performed during the design process. This can be done with a GTEM cell or at a compliance testing laboratory. It is recommended that pre-compliance testing be performed so that there are no surprises during final compliance testing. This will help keep the product development and release on schedule.

Working with a laboratory offers the benefit of years of compliance testing experience and familiarity with the regulatory issues. Also, the laboratory can often provide feedback that will help the designer make the product compliant.

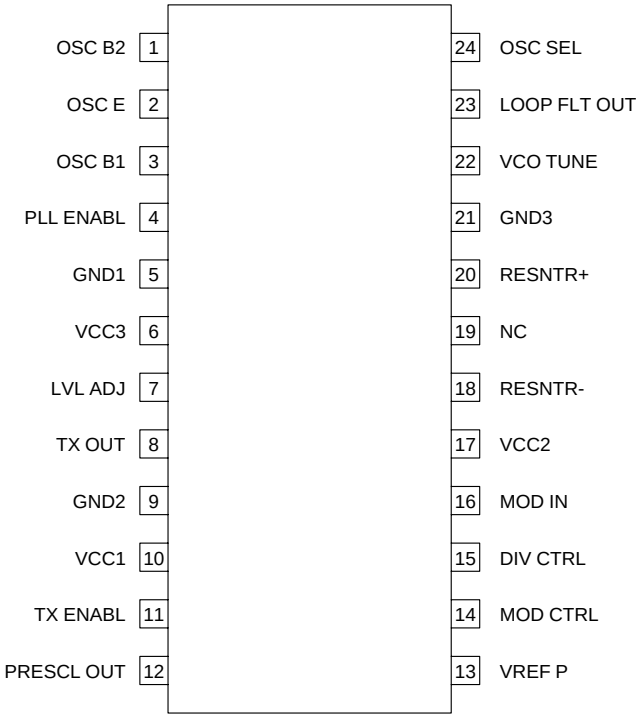
On the other hand, having a GTEM cell or an open air test site locally offers the designer the ability to rapidly determine whether or not design changes impact the product's compliance. Set-up of an open air test site and the associated calibration is not trivial. An alternative is to use a GTEM test cell.

After the design has been completed and passes compliance testing, application will need to be made with the respective regulatory bodies for the geographic region in which the product will be operated to obtain final certifications.

Conclusions

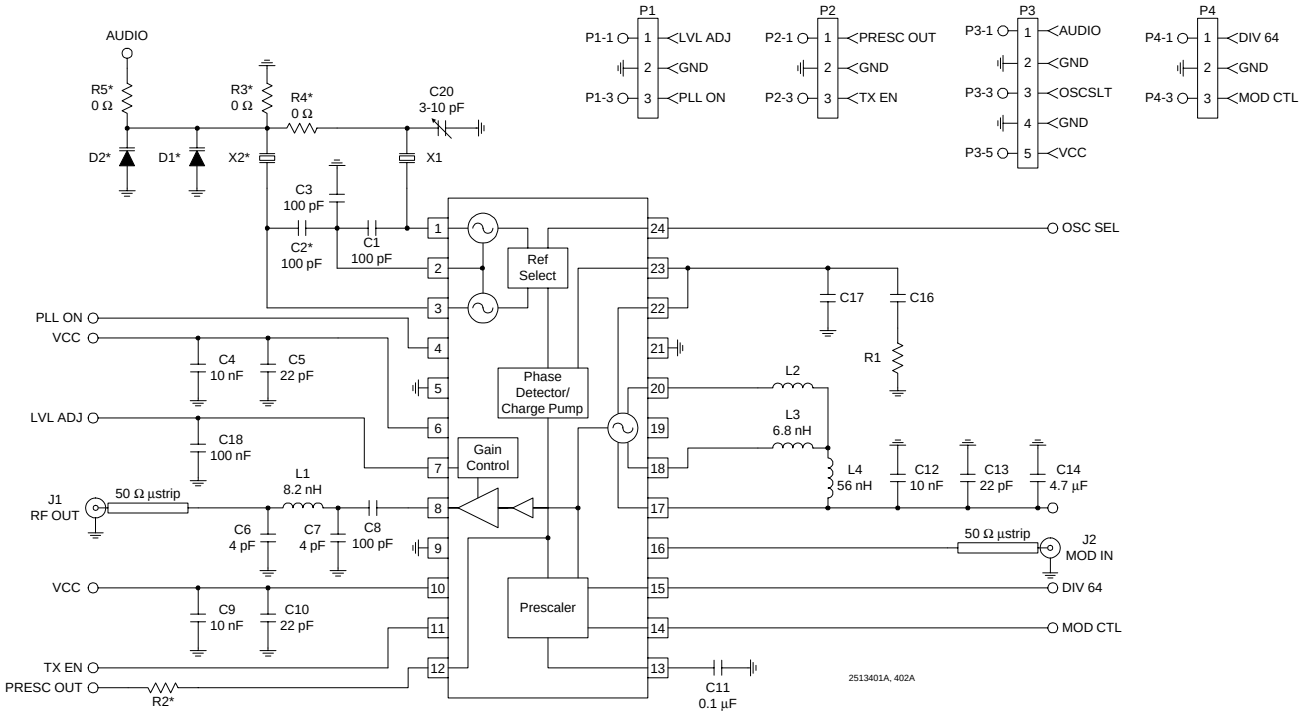
The RF2513 is an FM/FSK UHF transmitter that features a phase-locked output. This device is suitable for use in a CFR Part 15.231 compliant product as well as a local oscillator signal source. Two examples of showing these applications have been provided. Further, the RF2513 is packaged in a low cost SSOP-24 plastic package and requires few external parts, thus making it suitable for low cost designs.

Pin Out


OSC B2 1
OSC E 2
OSC B1 3
PLL ENABL 4
GND1 5
VCC3 6
LVL ADJ 7
TX OUT 8
GND2 9
VCC1 10
TX ENABL 11
PRESCL OUT 12
24 OSC SEL
23 LOOP FLT OUT
22 VCO TUNE
21 GND3
20 RESNTR+
19 NC
18 RESNTR-
17 VCC2
16 MOD IN
15 DIV CTRL
14 MOD CTRL
13 VREF P

Evaluation Board Schematic
H (915MHz) and M (868MHz) Boards

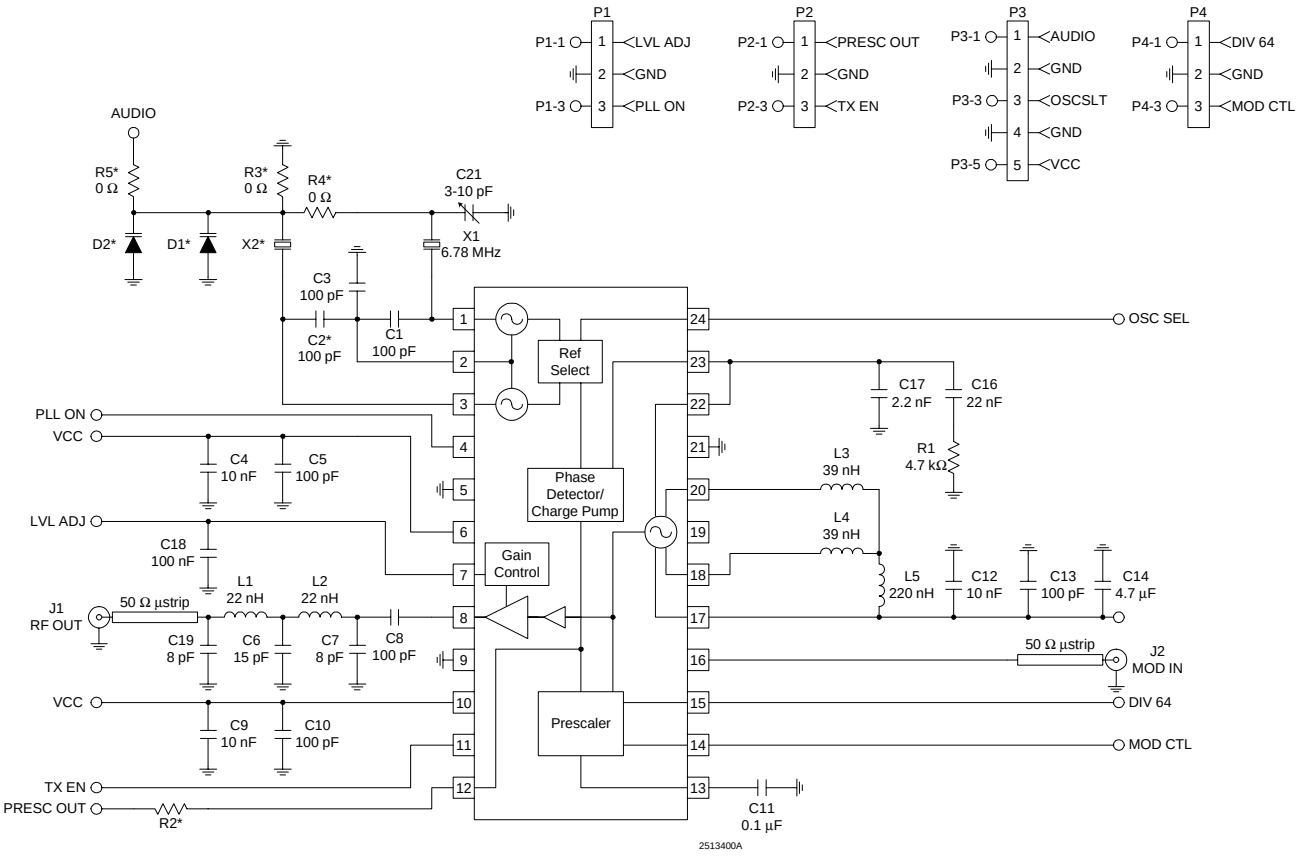
(Download Bill of Materials from www.rfmd.com.)



* Denotes optional. These parts are not normally populated.

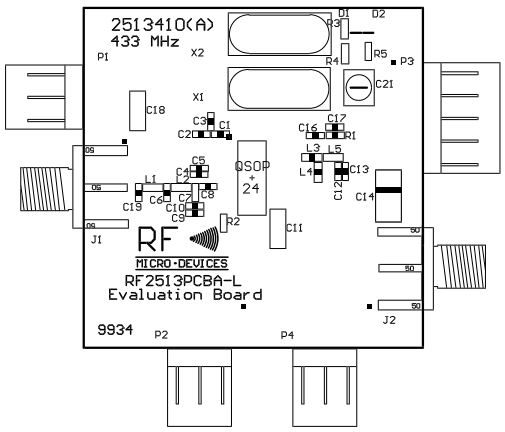
Board	X1 (MHz)	X2 (MHz)	R1 (kΩ)	L2 (nH)	C16 (nF)	C17 (nF)
M (868MHz)	13.57734	13.41015	2.2	8.2	47 nF	4.7
H (915MHz)	7.15909	7.07549	5.1	6.8	22 nF	2.2

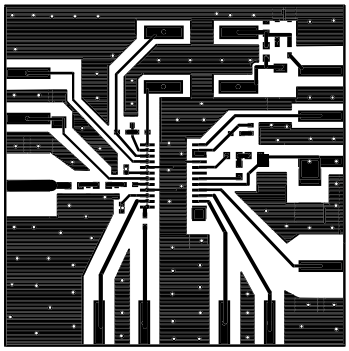
Evaluation Board Schematic
L (433MHz) Board

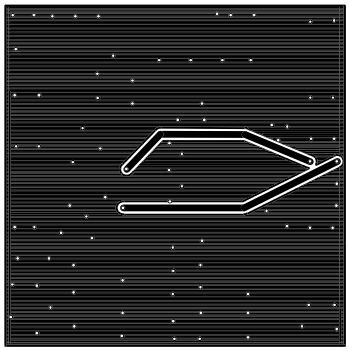


Evaluation Board Layout 433MHz
Board Size 2.0” x 2.0”

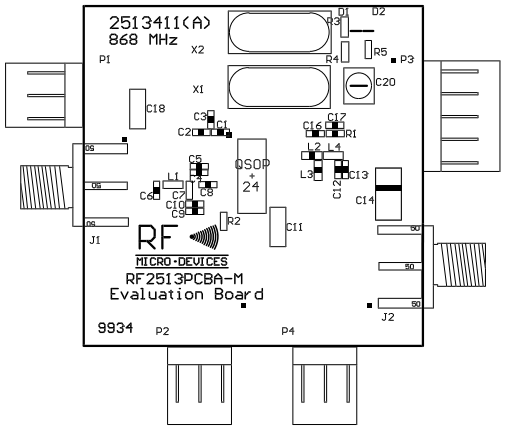
Board Thickness 0.031”, Board Material FR-4

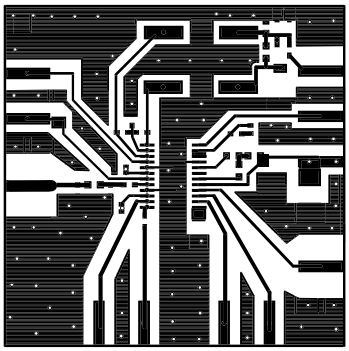


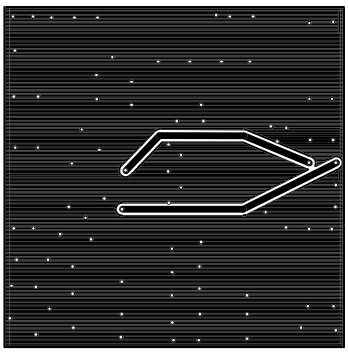




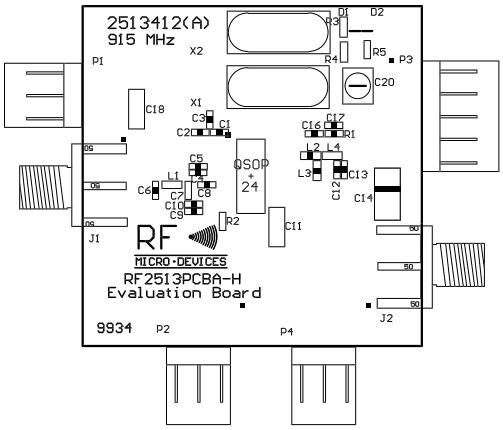
Evaluation Board Layout 868MHz
Board Size 2.0” x 2.0”

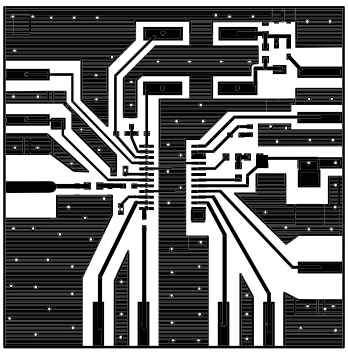


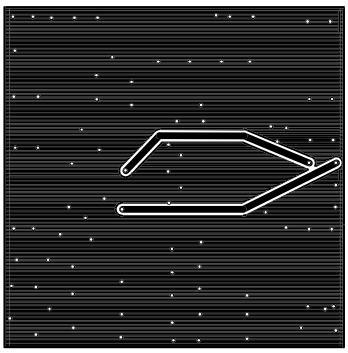


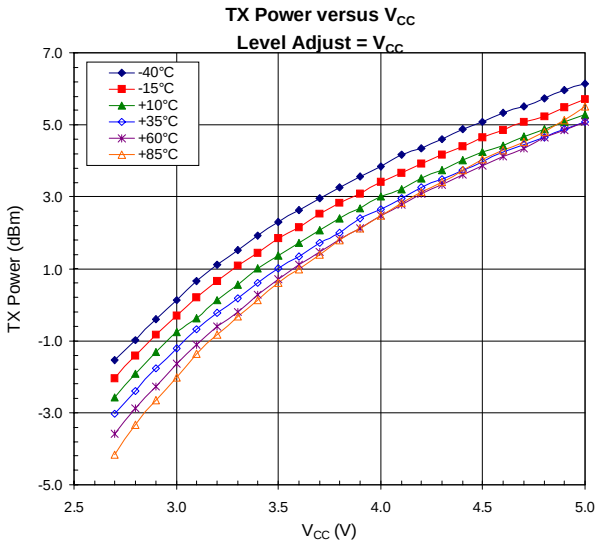


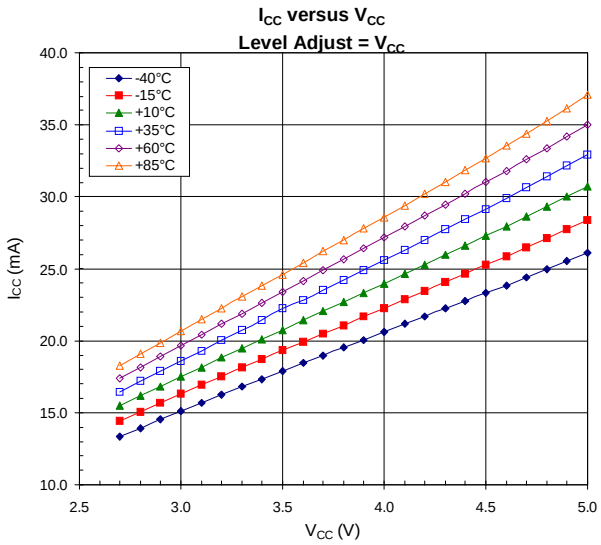
Evaluation Board Layout 915MHz
Board Size 2.0” x 2.0”








TX Power versus V_{CC}
Level Adjust = V_{CC}
-40°C
-15°C
+10°C
+35°C
+60°C
+85°C
TX Power (dBm)
7.0
5.0
3.0
1.0
-1.0
-3.0
-5.0
2.5
3.0
3.5
4.0
4.5
5.0
V_{CC} (V)


I_{CC} versus V_{CC}
Level Adjust = V_{CC}
-40°C
-15°C
+10°C
+35°C
+60°C
+85°C
I_{CC} (mA)
40.0
35.0
30.0
25.0
20.0
15.0
10.0
2.5
3.0
3.5
4.0
4.5
5.0
V_{CC} (V)