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Proposed

RF2722

GSM/GPRS/EDGE RECEIVER

Part of the POLARIS™ TOTAL RADIO™ Solution

RoHS Compliant & Pb-Free Product
Package Style: QFN, 32-Pin, 5x5

Features

- GSM850, EGSM, DCS & PCS Operation
- Supports Both VLIF & DCR Modes
- Integrated RF VCO
- Integrated LNA's Support up to Four RF Bands
- EDGE Receive Compatible

Applications

- EGSM/DCS Handsets
- EGSM/DCS/PCS Handsets
- GSM850/PCS Handsets
- GSM850/EGSM/DCS/PCS Handsets

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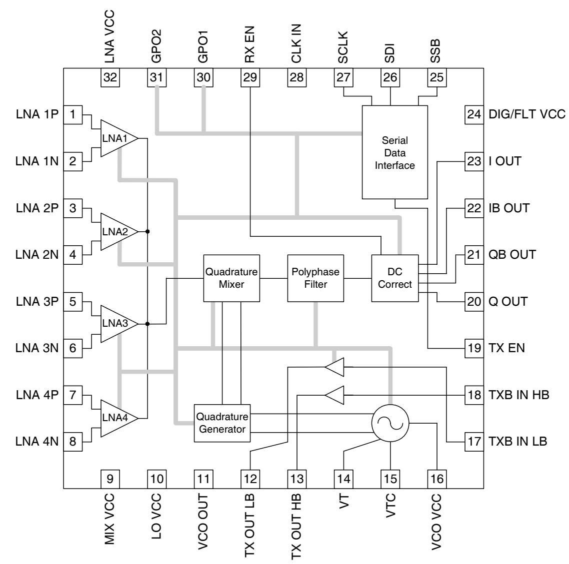

Functional Block Diagram

Product Description

The RF2722 is a highly-integrated receiver IC supporting GSM, GPRS, and EDGE cellular standards in the GSM850, EGSM, DCS, and PCS bands. The RF2722 supports both very-low intermediate frequency (VLIF) as well as direct conversion receive (DCR) architectures, reducing external component count and eliminating the need for IF SAW and RF interstage filters without compromising performance. The IC includes: four LNA's for multi-band support; an integrated voltage controlled oscillator (VCO); automatic gain control (AGC); a quadrature downconverting mixer; and, low and high band transmit buffers. Chip functionality, including IF AGC setting, is controlled through a three-wire serial data interface (SDI). The RF2722 is part of the POLARIS™ TOTAL RADIO™ solution.

Ordering Information

RF2722	GSM/GPRS/EDGE Receiver
RF2722PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V
Storage Temperature	-40 to +150	°C
Input Voltage, any pin	3.6	V

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Range					Temp=-30°C to +85°C, V_{CC}=2.7V to 3.0V, all specifications referenced to 50Ω, unless specified differently.
Temperature (T_{OP})	-30		+85	°C	
Frequency Range					
GSM850 RX	869		894	MHz	Low Band
GSM850 TX	824		849	MHz	Low Band
EGSM RX	925		960	MHz	Low Band
EGSM TX	880		915	MHz	Low Band
DCS RX	1805		1880	MHz	High Band
DCS TX	1710		1785	MHz	High Band
PCS RX	1930		1990	MHz	High Band
PCS TX	1850		1910	MHz	High Band
Supply Voltage (V_{CC})	2.7	2.75	3.0	V	Pins 9 (MIXVCC), 10 (LOVCC), 16 (VCOVCC), 24(DIG/FLTVCC), and 32 (LNAVCC).
Power Down Current			10	µA	RX EN=0
Active Current					
RX VLIF Mode					
Low Band (850/950MHz)	64	77	91	mA	All circuits on, (LNA_CURR=10, MIX_CURR=10)
High Band (1800/1900MHz)	63	76	90	mA	All circuits on, (LNA_CURR=00, MIX_CURR=00)
RX DCR Mode					
Low Band (850/950MHz)	62.5	75.5	89.5	mA	All circuits on, (LNA_CURR=10, MIX_CURR=10)
High Band (1800/1900MHz)	61.5	74.5	88.5	mA	All circuits on, (LNA_CURR=00, MIX_CURR=00)
TX Mode					
Low Band (850/950MHz)		19.5	25	mA	V_{CC}=2.8V, P_{IN}=+4dBm
High Band (1800/1900MHz)		24.5	32	mA	
Receiver System					Low side LO injection for all bands. Except where noted, receiver specifications defined from LNA input with I or Q channel differential as output.
Cascaded Noise Figure					
Low Band (850/950MHz)		2.8		dB	+25°C, LNA_BYP=0
High Band (1850/1950MHz)		3.2		dB	+25°C, LNA_BYP=0

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Low Band (850/950MHz)			4.8	dB	-30-85°C, LNA_BYP=0
High Band (1850/1950MHz)			5.2	dB	-30-85°C, LNA_BYP=0
Noise Figure with 3MHz Blocker					
Low Band (850/950MHz)		3.8	4.8	dB	+25°C; -26dBm at LNA input.
High Band (1800/1900MHz)		4.7	5.7	dB	+25°C; -29dBm at LNA input.
Cascaded IIP3					
Low Band (850/950MHz)		-12		dBm	+25°C; LNA_BYP=0; Interferers at 0.8MHz and 1.6MHz
High Band (1850/1950MHz)		-11		dBm	
Low Band (850/950MHz)	-15			dBm	-30-85°C; LNA_BYP=0; Interferers at 0.8MHz and 1.6MHz
High Band (1850/1950MHz)	-14			dBm	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Receiver System, cont'd					
Cascaded IIP2 (VLIF Improvement not included)					1 tone ($IIP2_1$)/2 tone ($IIP2_1$) LNA_BYP=0
Low Band (850/950MHz)	50	58		dBm	1 tone
	44	52		dBm	2 tone
High Band (1850/1950MHz)	50	58		dBm	1 tone
	44	52		dBm	2 tone
Cascaded P1dB					
Low Band (850/950MHz)	-22	-20		dBm	Minimum Gain
High Band (1850/1950MHz)	-23	-21		dBm	Minimum Gain
Cascaded Gain					
Low Band (850/950MHz)	54.5	57.5	60.5	dB	LNA_BYP=0; Polyphase Gain=0/12.6/7.4/1/8.4dB
High Band (1850/1950MHz)	53.5	56.5	59.5	dB	LNA_BYP=0; Polyphase Gain=0/12.6/7.4/1/8.4dB
Gain Compression with 3MHz Blocker					
Low Band (850/950MHz)			1.5	dB	+25°C; LNA_BYP=0; -26dBm at LNA input, with gain settings for a -99dBm wanted signal.
High Band (1850/1950MHz)			1.0	dB	+25°C; LNA_BYP=0; -29dBm at LNA input, with gain settings for a -99dBm wanted signal.
LNA Gain Step					
Low Band (850/950MHz)	15	16	17	dB	LNA_BYP=1
High Band (1850/1950MHz)	17	18	19	dB	LNA_BYP=1
LO Leakage					
Low Band (850/950MHz)		-110	-100	dBm	At the LNA input.
High Band (1850/1950MHz)		-110	-100	dBm	At the LNA input.
2LO Suppression					LNA_BYP=0
Low Band (850/950MHz)		-22	-20	dB	
High Band (1850/1950MHz)		-24	-22	dB	
3LO Suppression					LNA_BYP=0
Low Band (850/950MHz)		-6	-4	dB	
High Band (1850/1950MHz)		-16	-14	dB	
5LO Suppression					LNA_BYP=0
Low Band (850/950MHz)		-22	-20	dB	
High Band (1850/1950MHz)		-45	-43	dB	
Image Balance					
Low Band (850/950MHz)	32	36		dB	
High Band (1850/1950MHz)	32	36		dB	
LNA Input Impedance					
Low Band (850/950MHz)		82-j156		Ω	
High Band (1850/1950MHz)		38-j66		Ω	
LNA Input Return Loss					
Low Band (850/950MHz)			-10	dB	With external match to 100Ω
High Band (1850/1950MHz)			-10	dB	With external match to 100Ω
Absolute Gain Accuracy	-3.2		+3.2	dB	For any recommended AGC setting across frequency and temperature in a single band, for power levels between -110dBm and -48dBm, assuming 1 gain calibration point per band.

Relative Gain Accuracy	-1		+1	dB	For any 20dB gain step, using recommended AGC gain settings for receive power levels in the range -110dBm and -48dBm.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
VCO+LO Chain					Buffers, divide-by-2, divide-by-4, divide-by-8
LO Frequency	869		960	MHz	VCOHL=0
	1805		1990	MHz	VCOHL=1
Output Level to Synth	-18.6	-17.4	-16.2	dBm	2kΩ//5pF load
Output Frequency to Synth	434.5		497.5	MHz	VCO_OUT=VCO/8
Tuning Voltage	0.5		2.0	V	
Tuning Line Input Impedance		12		MΩ	DC measurement
K_{VCO}*	-27		-107	MHz/V	
LO Phase Noise, Low Band					GSM850/EGSM
0.6MHz		-129.2	-127.2	dBc/Hz	
1.6MHz		-138.4	-136.4	dBc/Hz	
3.0MHz		-142.8	-140.8	dBc/Hz	
10.0MHz		-145.0	-143.0	dBc/Hz	
LO Phase Noise, High Band					DCS/PCS
0.6MHz		-123.0	-121.0	dBc/Hz	
1.6MHz		-133.1	-131.1	dBc/Hz	
3.0MHz		-137.9	-135.9	dBc/Hz	
10.0MHz		-140.0	-138.0	dBc/Hz	
* When used with an RF600X, the product of K_{VCO} x Charge Pump Current is calibrated to be within 5% of nominal value.					

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Polyphase Filter (4th Order)					
VLIF Mode					
Center Frequency	99.5	107.0	114.5	kHz	
Half-Bandwidth	180	200	220	kHz	
In-Band Ripple			0.35	dB	130kHz Half-Bandwidth
Group Delay			1.3	us	130kHz Half-Bandwidth
Integrated Attenuation					
200kHz	5.0			dB	
400kHz	23.0			dB	
600kHz	38.0			dB	
>600kHz	38.0			dB	
I/Q Phase Error		1.0	1.8	°	Entire RX chain
I/Q Amplitude Error		0.1	0.25	dB	Entire RX chain
Output Capacitive Load			20	pF	
Output Resistive Load		30		kΩ	30kΩ RF6001/3 RX A/D input impedance.
Maximum Output Voltage Swing	1			V_{P-P}	Differential
Output Common Mode Voltage	1.23	1.26	1.29	V	
Static DC Offset	-160		+160	mV	Uncorrected
Direct Conversion (DCR) Mode					
Center Frequency	-7.5	0	+7.5	kHz	
Half-Bandwidth	180	200	220	kHz	
In-Band Ripple			0.35	dB	130kHz Half-Bandwidth
Group Delay			1.3	us	130kHz Half-Bandwidth
Integrated Attenuation					
200kHz	5.0			dB	
400kHz	23.0			dB	
600kHz	38.0			dB	
>600kHz	38.0			dB	
I/Q Phase Error		1.0	1.8	°	Entire RX chain
I/Q Amplitude Error		0.1	0.25	dB	Entire RX chain
Output Capacitive Load			20	pF	
Output Resistive Load		30		kΩ	30kΩ RF6001/3 RX A/D input impedance.
Maximum Output Voltage Swing	1			V_{P-P}	Differential
Output Common Mode Voltage	1.20	1.23	1.26	V	
DC Offset (Uncorrected)	-160		+160	mV	Uncorrected

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Polyphase Filter (4th Order), cont'd					
Polyphase Input Attenuator (DCR) (Midband Gain)					
Gain	-0.3	0	+0.3	dB	C_G1_1:0=11
	-6.1	-5.5	-4.9	dB	C_G1_1:0=10
	-14.0	-13.0	-12.0	dB	C_G1_1:0=00
First Pole (DCR) (Midband Gain)					
Gain	18.6	18.7	18.8	dB	F_G1_3:0=0111
	17.5	17.6	17.7	dB	F_G1_3:0=0110
	16.5	16.6	16.7	dB	F_G1_3:0=0101
	15.5	15.6	15.7	dB	F_G1_3:0=0100
	14.5	14.6	14.7	dB	F_G1_3:0=0011
	13.5	13.6	13.7	dB	F_G1_3:0=0010
	12.5	12.6	12.7	dB	F_G1_3:0=0001
	11.5	11.6	11.7	dB	F_G1_3:0=0000
	10.4	10.5	10.6	dB	F_G1_3:0=1111
	9.4	9.5	9.6	dB	F_G1_3:0=1110
	8.4	8.5	8.6	dB	F_G1_3:0=1101
	7.4	7.5	7.6	dB	F_G1_3:0=1100
	6.4	6.5	6.6	dB	F_G1_3:0=1011
	5.4	5.5	5.6	dB	F_G1_3:0=1010
	4.4	4.5	4.6	dB	F_G1_3:0=1001
	3.4	3.5	3.6	dB	F_G1_3:0=1000
Second Pole (DCR) (Midband Gain)					
Gain	7.3	7.4	7.6	dB	S_G2_0=1
	-0.9	-0.7	-0.5	dB	S_G2_0=0
Third Pole (DCR) (Midband Gain)					
Gain	0.9	1.0	1.1	dB	S_G2_1=1
	-6.9	-6.8	-6.7	dB	S_G2_1=0
Fourth Pole (DCR) (Midband Gain)					
Gain	13.9	14.3	14.7	dB	S_G3_1:0=11
	8.1	8.4	8.7	dB	S_G3_1:0=01
	2.2	2.5	2.8	dB	S_G3_1:0=00

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Offset Correction					
Residual DC Error	-20		+20	mV	Following DC offset correction. Differential measurement.
DC Correction Time			20	µs	
DC Offset Drift Referred to the LNA Input			-126	dBm	Max gain measured in a window 150µs to 730µs after RXEN is activated.
CLK IN Frequency		26		MHz	CLKF=0
TX Buffer					
Low Band					
Input Power	3		6	dBm	
Saturated Output Power	6.6	7.7	8.8	dBm	P_{IN}=+4dBm
Output Power Variation	-1.1		1.1	dB	
DC Current Drain	5.2	7.2	9.3	mA	DC with no RF input
RF Current Drain	14	19.5	25	mA	P_{IN}=+4dBm
Phase Noise	-167			dBc/Hz	20MHz offset
Input VSWR		3:1			P_{IN}=+4dBm
Output VSWR			2:1		P_{IN}=+4dBm
Load VSWR			3:1		P_{IN}=+4dBm
Reverse Isolation	20			dB	TXEN=H
Forward Isolation	20			dB	TXEN=L
High Band					
Input Power	3		6	dBm	
Saturated Output Power	4.9	6.5	8.1	dBm	P_{IN}=+4dBm
Output Power Variation	-1.6		1.6	dB	
DC Current Drain	8	11	13.8	mA	DC with no RF input
RF Current Drain	18	24.5	32	mA	P_{IN}=+4dBm
Phase Noise	-160			dBc/Hz	
Input VSWR		3:1			P_{IN}=+4dBm
Output VSWR			2:1		P_{IN}=+4dBm
Load VSWR			3:1		P_{IN}=+4dBm
Reverse Isolation	35			dB	TXEN=H
Forward Isolation	28			dB	TXEN=L

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Serial Interface					Applies to pins SCLK, SDI and SSB.
Input High Voltage (V_{IH})	$0.7*V_{CC}$			V	
Input Low Voltage (V_{IL})			$0.3*V_{CC}$	V	
Input High Current (I_{IH})			5	μA	
Input Low Current (I_{IL})			5	μA	
Setup Time (T_{SU})	25			ns	
Hold Time (T_H)	10			ns	
Rise/Fall Time (T_{RF})			10	ns	
Clock to Select Time (T_{CS})	10			ns	
Clock Pulse Width High (T_{CWH})	50			ns	
Clock Pulse Width Low (T_{CWL})	50			ns	
Digital Output Drivers					Apply to pins: GPO1, GPO2
Output High Voltage (V_{OH})	V_{CC}-0.05			V	1mA load
	V_{CC}-0.50			V	10mA load
Output Low Voltage (V_{OL})			0.05	V	1mA load
			0.50	V	10mA load
Output Rise/Fall Time (T_{RFO})			5	ns	
26MHz Reference Clock Input					Applies to CLKIN.
Frequency Range (F_R)		26		MHz	
Input Level (V_{INR})	600			mV_{P-P}	AC-coupled mode
Input Impedance (Z_{INR})		49kΩ// 480fF			
Interface Voltage		$V_{CC}/2$		V	Internal bias
Transient Startup Time		250		ns	
Input High Voltage (V_{IH})	$0.7V_{CC}$			V	DC-coupled mode
Input Low Voltage (V_{IL})			$0.3V_{CC}$	V	DC-coupled mode

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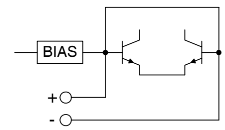
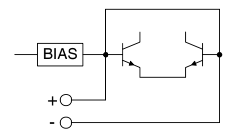
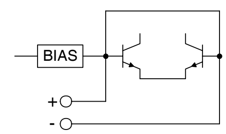
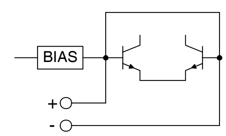
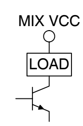
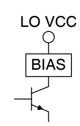
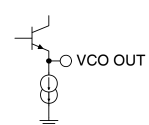
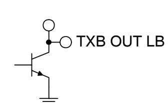
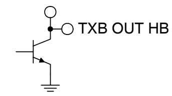
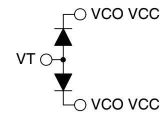
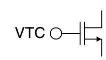
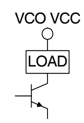
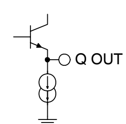
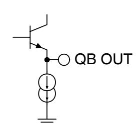
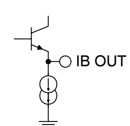
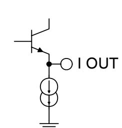
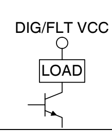
Pin	Function	Description	Interface Schematic
1	LNA 1P	RF input to LNA 1. Internally matched for 800MHz to 1000MHz operation. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	
2	LNA 1N	Complementary input to pin 1. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	See Pin 1.
3	LNA 2P	RF input to LNA 2. Internally matched for 800MHz to 1000MHz operation. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	
4	LNA2N	Complementary input to pin 3. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	See Pin 3.
5	LNA 3P	RF input to LNA 3. Internally matched for 1800MHz to 2000MHz operation. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	
6	LNA 3N	Complementary input to pin 5. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	See Pin 5.
7	LNA 4P	RF input to LNA 4. Internally matched for 1800MHz to 2000MHz operation. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	
8	LNA 4N	Complementary input to pin 7. This pin possesses a DC voltage with respect to ground, and a series blocking cap may be required in some applications.	See Pin 7.
9	MIX VCC	Supply for the quadrature mixer.	
10	LO VCC	VCO divider supply.	
11	VCO OUT	Output from the VCO to drive the synthesizer input. This is the VCO divided by 8.	
12	TXB OUT LB	Low band TX buffer output.	

Pin	Function	Description	Interface Schematic
13	TXB OUT HB	High band TX buffer output.	
14	VT	Tuning control line for the VCO. Analog input.	
15	VTC	Coarse VCO tuning control driven by RF6001. Digital input.	
16	VCO VCC	Supply for the RF VCO.	
17	TXB IN LB	TX buffer low band input. This is a high impedance voltage-driven input designed to be driven by the RF6001/3 TXVCO output.	
18	TXB IN HB	TX buffer high band input. This is a high impedance voltage-driven input designed to be driven by the RF6001/3 TXVCO output.	
19	TX EN	TX buffer enable. If the TX SEL (CRX1[2]) bit is set high, the TX buffers are enabled by this pin. If the TX SEL bit is set low, this pin has no effect on the activation of the TX buffers. (See register map for more information.) The TX buffers are enabled by setting this pin high. The TX buffers are disabled by setting this pin low.	
20	Q OUT	Q-channel differential IF output.	
21	QB OUT	Complementary output to Q OUT.	
22	IB OUT	Complementary output to I OUT.	
23	I OUT	I-channel differential IF output.	
24	DIG/FLT VCC	Supply for all digital circuitry. Supply for the filter.	

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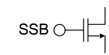
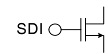
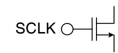
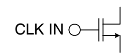
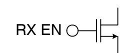
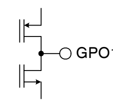
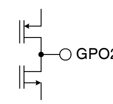
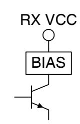
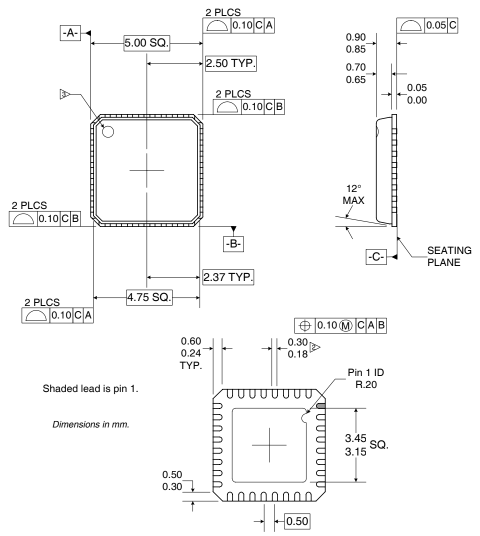
Pin	Function	Description	Interface Schematic
25	SSB	SDI enable input (active low).	
26	SDI	SDI data input.	
27	SCLK	SDI clock input.	
28	CLK IN	Clock input for the DC offset correction system. A 26MHz clock must be applied to this pin for proper operation of the DC offset correction system.	
29	RX EN	Set to VCC to activate the IC. Set to GND to deactivate.	
30	GPO1	General purpose digital output 1. Controlled via SDI programming.	
31	GPO2	General purpose digital output 2. Controlled via SDI programming.	
32	RX VCC	Supply for the LNA's.	

Package Drawing



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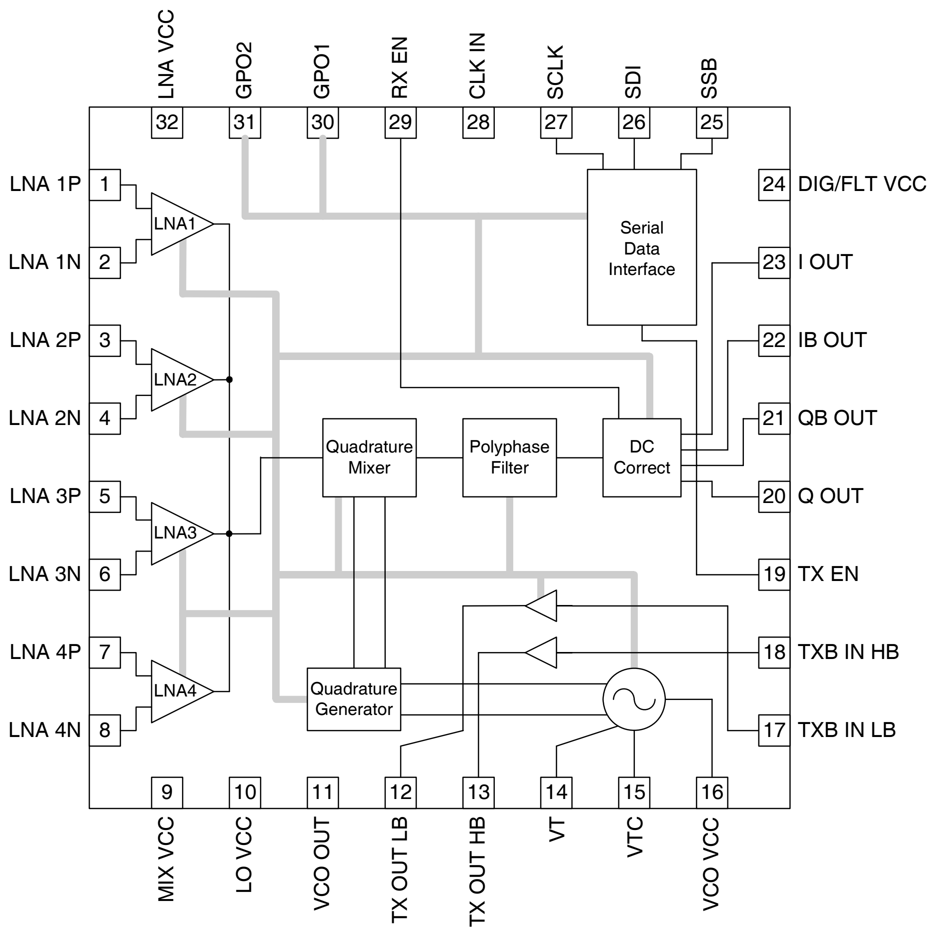
Detailed Functional Block Diagram



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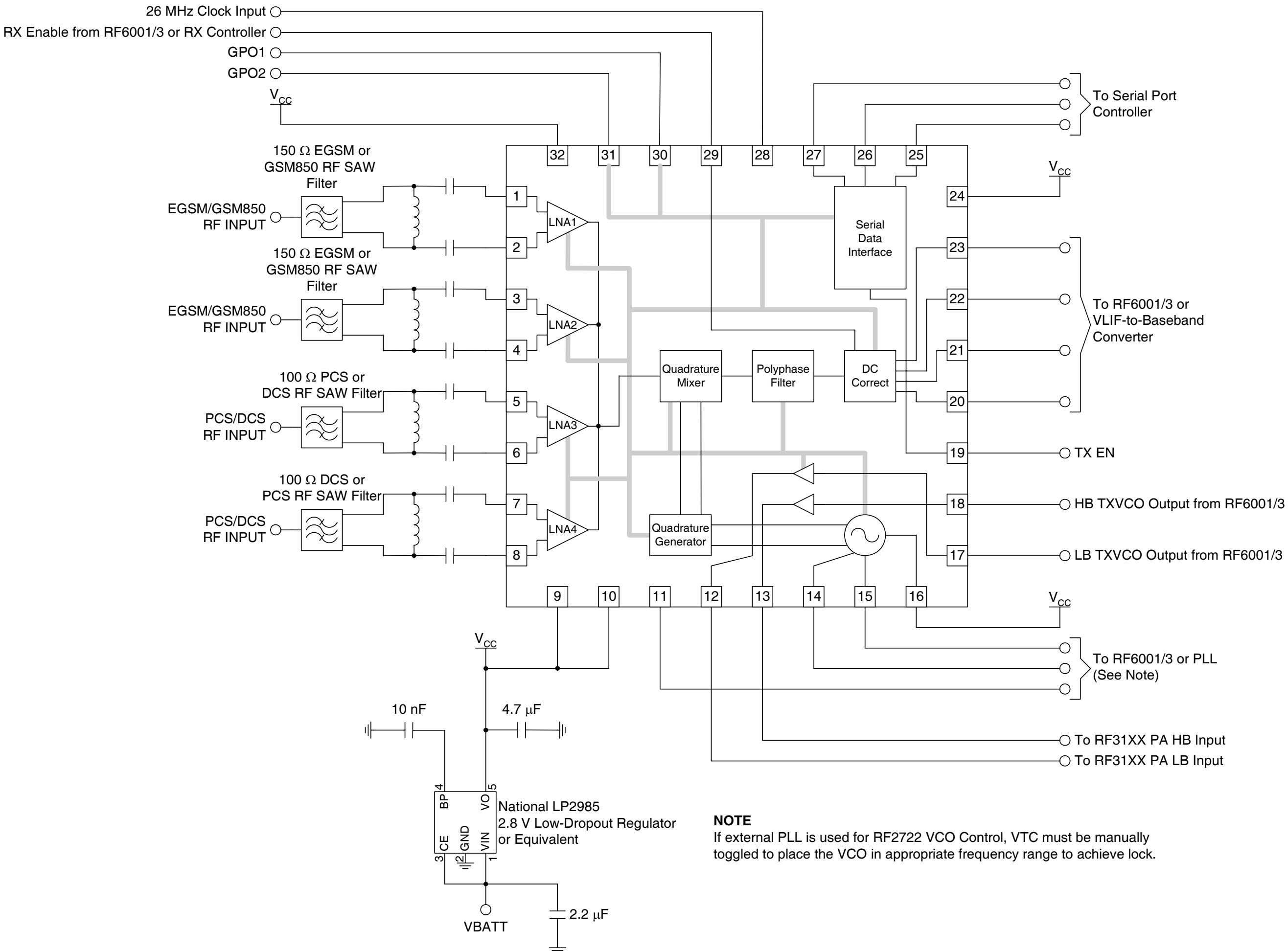
Application Schematic



NOTE
If external PLL is used for RF2722 VCO Control, VTC must be manually toggled to place the VCO in appropriate frequency range to achieve lock.

Application Information

Functional Description

The RF2722 receiver IC will support GSM and EDGE cellular standards.

Four Low Noise Amplifiers (LNA's) are provided to accommodate various combinations of up to four bands. The four LNA's share a common quadrature mixer. The active LNA is selected and may be bypassed through the Serial Data Interface (SDI).

An RX Local Oscillator (VCO) is provided. The VCO is fully integrated including an internal resonator and is band-selectable to cover the GSM850, EGSM, DCS, and PCS bands.

The desired signal is converted to either a VLIF (100kHz/120kHz) or directly to DC, as determined by the setting of bit 1 in SDI register CF.

Once downconverted, the signal is filtered by an active RC Polyphase bandpass filter. The purpose of this filter is to provide some rejection to interfering signals such that the dynamic range of the A/D converters will not be compromised.

The RF2722 also includes two reverse isolation dual-band buffer amplifiers. These buffers are suitable for use in the transmit path between the VCO output and the PA input to improve transmit performance. The RF2722 accepts single-ended inputs from the RF6001/3 and provides single-ended outputs to the PA.

DC Correction Operation

The Polaris RF2722 VLIF/DCR IC will reduce the residual DC error of the I and Q channels to less than 20mV within 20usec assuming that no input signal is present during the DC adapt time. The DC correction system will activate on the rising edge of RX_EN if the SDI bit DC_EN is programmed true. Programming the SDI bit DC_ST true can also activate the DC correction system. In this case the SDI bit DC_ST will automatically return to a false state once the DC correction system is activated.

The RF6001/3 also has an RX_EN pin that normally is set high at the same time as the RX_EN of the RF2722.

The DC correction system of the RF2722 will run for DC_TIME1 cycles of the clock present on CLK_IN divided by 16. This should be set for approximately 20usec. With a 26MHz clock on CLK_IN the setting of DC_TIME1 will be 20H. Given the low levels of LO leakage to the LNA inputs of the RF2722, the coarse DC adapt will be performed when RX_EN rises with the LNAs disabled. The residual DC error due to LO leakage when the LNAs are enabled will be less than 5mV. Once completed the DC correction outputs of the RF2722 will be held until power is removed from the IC or until another DC correction command is issued.

During operation of the DC correction system the input signal should be muted so that the coarse DC correction system does not attempt to lock to the instantaneous signal level. This can be accomplished by disabling all LNAs. This mode is selected if the LND SDI bit is programmed true. This is performed for DC_TIME2 clock cycles of CLK_IN divided by 16 beginning at the DC correction command time so that the RF2722 will have sufficient time to complete DC correction.

If the radio employs a T/R switch then the T/R switch can also be used to disable the signal instead of or in addition to disabling the LNAs. The RF2722 can be used to automatically disable the T/R switch if the SDI bit TRD is programmed true. In this case it is assumed that GPO1 and GPO2 provide on/off control for each of the possible bands of the receive side of the T/R switch. During the DC control time interval set by DC_TIME2 the outputs of GPO1 and GPO2 will be overridden by the SDI register TRDC. The bits of this register can be set to 0 or 1 as needed by the particular T/R switch implementation to deactivate the receiver inputs. After DC_TIME2 has expired the normally programmed GPO states will return.

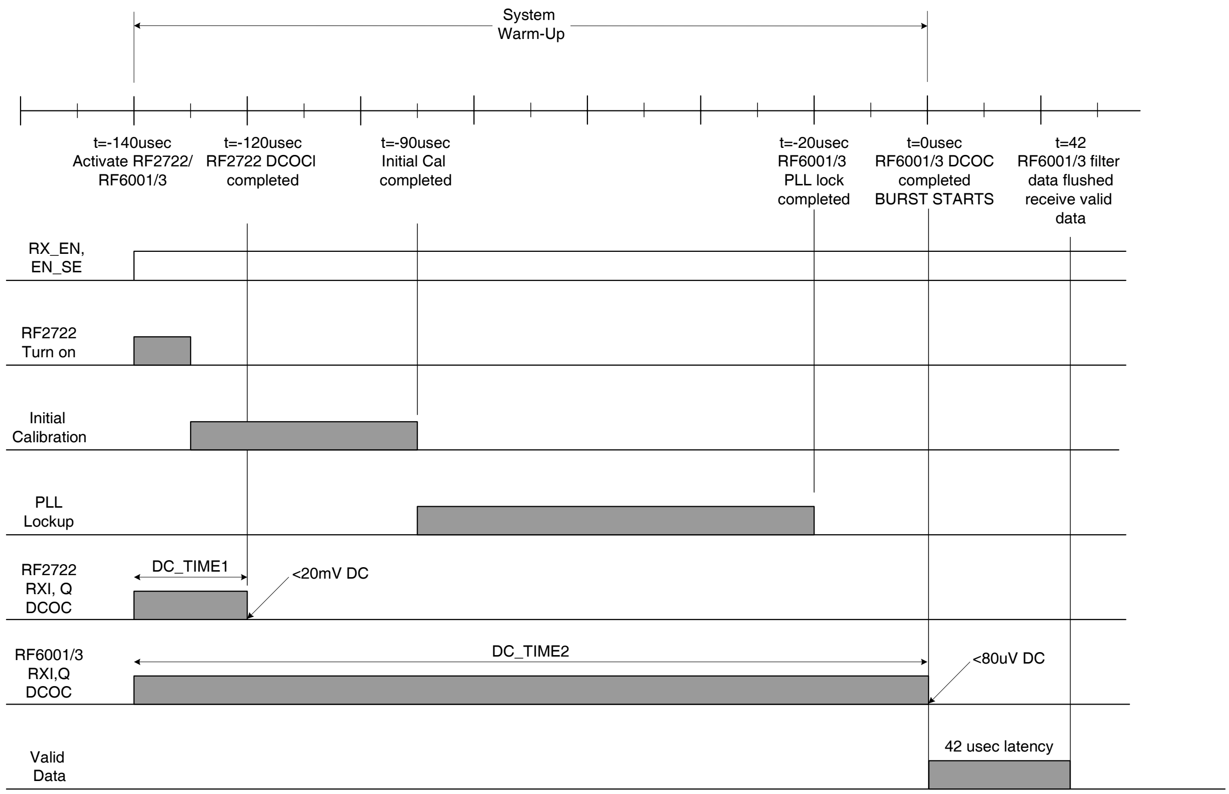
After the coarse DC adapt time has elapsed then the RF6001/3 will require an additional time of approximately 50usec to complete the fine digital DC correction.

Note that the input signal may be present during the final DC correction time of the RF6001/3. For VLIF modes this will not cause a DC problem since the RF6001/3 does an averaging of the DC error and there will be few components of the signal near DC. In addition, the RF6001/3 will notch out 100kHz converted DC components for channel bandwidths less than or equal to 85kHz. The RF6003 will also notch out 120kHz converted DC components for channel bandwidth of 90kHz. This is only useful in VLIF mode.

In DCR mode there may be significant spectral content near DC during the final adapt of the RF6001/3. This may result in a significant DC component that will track the input desired signal level. It is assumed that the baseband DSP will be able to remove any such static DC error. In addition, if the DC adapt of the RF6001/3 is performed during the guard times then the spectral content of the input signal should be a tone in the region of 50kHz to 70kHz and should not interfere with the DC adapt process.

If DC_TIME2 is extended to encompass the fine DC adapt time of the RF6001/3 then the input signal will not interfere with the adapt process as the LNAs will be muted. However, if there is any residual LO leakage into the LNA input then this error will remain after the DC correction process. This may be a smaller residual error than that due to the input signals.

A diagram depicting the composite DC correction and RX startup of the RF2722 and RF6001/3 is presented below.



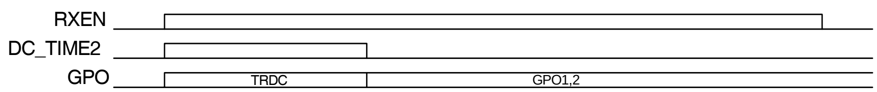
GPO Control

The RF2722 allows the GPOs to switch to an alternate setting defined by TRDC during RX DC offset correction when TRD is programmed high. This is triggered by the rising edge of RX_EN pin and terminated by the expiration of DC_TIME2 in the RF2722. This mode of operation is used to turn off the LNAs or redirect the T/R switch to TX mode during the DCOC time interval so that the signal present from the previous time slot or LO leakage will not cause an error in the DCOC.

In TX mode the RF2722 can also switch to an alternate set of GPO settings defined by TRTXA at the rising edge of TX_EN pin when TRTX_EN is programmed high. This functionality is used to redirect the T/R switch to RX mode during the synthesizer lock time so that the PA output due to feed-through from the VCO will not violate the ETSI time-mask specification.

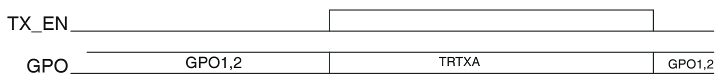
RX Mode

When RXEN rises, DC_TIME2 starts in the RF2722 and the part switches to the alternate GPO settings defined in TRDC. Once the timer expires then the settings of the GPO's revert back to the originally programmed GPO SDI fields.



TX Mode

When TXEN rises, the RF2722 GPOs switch to the alternate GPO settings defined in TRTXA. When TXEN falls, the RF2722 GPO settings revert back to the originally programmed GPO SDI fields.



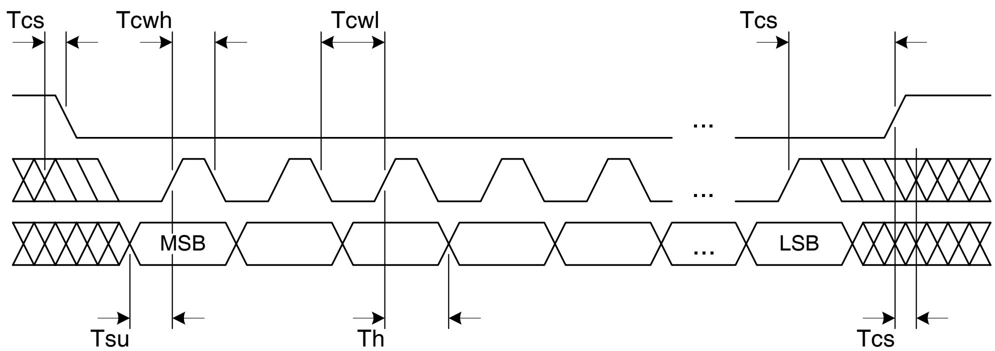
Device Control and Programming

The Polaris RF2722 VLIF/DCR IC provides a serial interface for programming the control settings. The interface consists of eight registers that are accessed individually via a six-bit address word. (Two registers are unused at this time and are included for future expansion.) The register map is shown below. Each register plus the six address bits requires an 18-bit transfer (except register CF, which has 18 bits and so requires a 24-bit transfer). Additional 'padding' bits can be added between the address bits and the data bits, if longer transfer lengths are needed. Since the RF2722 will be most likely used with the RF6001/3 then it is expected that six such padding bits will be used in each transfer to bring the total number of bits up to 24. This will then match the programming width of the RF6001/3.

Address	Register	Description
100000	CRX1	AGC, standby modes, LO phase cal
100001	CRX2	DCOC and GPO
100010	CRX3	DCOC
100011	CRX4	DCOC
100100	CRX5	LNA, VCO, mixer current settings, Gain cal
100101	CF	Gain settings for the polyphase filters and LNA's.
100110	Reserved	Reserved for future use.
100111	Reserved	Reserved for future use.
011111	Reset	Writing this address resets all SDI bits to their default states.

At power up the SDI address 011111 should be written to set up the default reset states of all registers. Note that programmed settings will be lost if power to the part is removed.

The figure below shows a timing diagram for the serial interface. The slave select (SS) pin is normally high. A serial transfer is initiated by taking SS low. The address and data bits on the serial data in (SDI) pin are shifted in on rising edges of the serial clock (SCLK) pin. Twelve data bits follow the four address bits. The data is latched and changes take effect on the rising edge of SS. Refer to the Electrical Specifications for the timing requirements.



Receiver Configuration Register 1 (CRX1) - Address 100000

Location	Bit Name	Default	Description
CRX1(11)	reserved	0	Reserved
CRX1(10:7)	LO_PH_CAL	0000	I/Q Phase Calibration
CRX1(6)	CLK BYP	1	If set to zero, then the CLK_IN pin is AC-coupled. If set to one, then the CLK_IN pin is DC-coupled.
CRX1(5)	CLKF	0	Input clock frequency select. (Must be set to 26MHz for normal operation.) Programming this bit high activates a divide-by-two function on the CLK_IN pin. Programming this bit low deactivates the divide-by-two function. The DC offset correction circuitry requires a 26MHz clock for proper operation. Therefore, CLKF should be programmed low if a 26MHz clock is provided to the CLK_IN pin. 0=CLK_IN frequency is 26MHz 1=CLK_IN frequency is 52MHz
CRX1(4)	VCOSEL	0	When set to zero, the VCO is turned on and off by RX_EN. When programmed high, the VCO is controlled by the VCOEN bit instead of RX_EN.
CRX1(3)	VCOEN	0	When VCOSEL is set to one, then VCOEN turns on and off the VCO. When VCOEN is set to zero, the VCO is off. When VCOEN is set to one, the VCO is turned on.
CRX1(2)	TXSEL	1	If programmed high, the TX buffers are enabled by the TX_EN pin. If programmed low, the TX buffers are enabled by CF[16].
CRX1(1:0)	TEST	00	Test Output Selection Bits: The GPO1 pin provides test signal outputs as well as the activation signal for the RF6001 RX system. The available signals are shown below. 00 Normal output of GPO1 pin 01 Serial data shifting through Configuration Registers 10 MSB bit of the VCO calibration counter 11 dcadapt counter 2 output

Receiver Configuration Register 2 (CRX2) - Address 100001

Programming Bits	# of Bits	Default	Description
CRX2(11)	DC_ST	0	If programmed high, the DC correction system is activated when the SDI word is loaded. DC_ST will revert low once the DC correction system is activated. RX EN needs to be high for DC_ST to operate correctly.
CRX2(10)	DC_EN	1	If programmed high, the DC correction system is activated on the rising edge of RX_EN (default=1).
CRX2(9)	LND	0	If programmed high, the LNA's are disabled during the time interval of the DC correction system.
CRX2(8)	TRD	0	If programmed high, GPO1 and GPO2 follow TRDC instead of the normal GPO programming during the time interval defined by DC_TIME2.
CRX2(7)	TRTX_EN	0	If programmed high, the functionality defined by TRTXA is active.
CRX2(6)	reserved	0	Reserved
CRX2(5:4)	TRDC	00	If TRD is set true, then during the time interval defined by DC_TIME2, GPO1 and GPO2 are reassigned as follows. GPO1=TRDC[0] GPO2=TRDC[1]
CRX2(3:2)	TRTXA	00	If TRTX_EN is programmed high, while TXEN pin is high the GPO outputs are reassigned as follows: GPO1=TRTXA[0] GPO2=TRTXA[1]
CRX2(1:0)	GPO	00	The states of each bit within this word are transferred to the corresponding GPO pin as follows. GPO1=GPO[0] GPO2=GPO[1]

Receiver Configuration Register 3 (CRX3) - Address 100010

Programming Bits	# of Bits	Defaults	Description
CRX3(11:10)	reserved	00	Reserved
CRX3(9:2)	DC_TIME1	20H	Sets the number of 26MHz/16 clock cycles from activation until the RF2722 DCOC system is frozen.
CRX3(1:0)	reserved	00	Reserved

Receiver Configuration Register 4 (CRX4) - Address 100011

Programming Bits	# of Bits	Defaults	Description
CRX4(11:10)	reserved	00	Reserved
CRX4(9:0)	DC_TIME2	124H	Sets the number of 26MHz/16 clock cycles from activation until the LNA's and/or the RX T/R switch are reactivated.

Receiver Configuration Register 5 (CRX5) - Address 100100

Programming Bits	# of Bits	Defaults	Description
CRX5(11:9)	Gain_Cal	011	I/Q Gain Calibration
CRX5(8:6)	Reserved	000	Reserved
CRX5(5:4)	Reserved	00	Reserved
CRX5(3:2)	LNA_CURR	10	These bits control the LNA current as shown below. Low Band High Band 00 11mA 13.2mA 01 12.8mA 15mA 10 14.6mA 16.9mA 11 16.4mA 18.7mA
CRX5(1:0)	MIX_CURR	10	These bits control the Mixer current as shown below. 00 12.5mA 01 13.5mA 10 14.4mA 11 15.6mA

Polyphase Filter Gain Register (CF) - Address 100101

Programming Bits	# of Bits	Defaults	Description
CF(17)	TX_HL	0	If programmed low, enables Cellular/GSM TX buffer. If programmed high, enables PCS/DCS TX buffer.
CF(16)	TX_EN	0	If TX_SEL is set false, TX buffers are controlled by this bit.
CF(15:13)	LNA_SEL	101	Selects the active LNA. 000 LNA1 (US/GSM) 001 LNA2 (US/GSM) 010 LNA3 (DCS/PCS) 011 LNA4 (DCS/PCS) 100 All LNA's off 101 All LNA's off
CF(12)	VCOHL	0	If programmed low, divides the VCO by 2 and routes signal through US Cellular/GSM filter path. If programmed high, the VCO signal is routed through PCS/DCS filter path.
CF(11:8)	F_G1	0000	Selects the fine gain setting of the first pole of the filter. The gain in dB at the mid-band (0Hz for DCR) is as shown below. 0000=11.6dB0001=12.6dB0010=13.6dB0011=14.6dB 0100=15.6dB0101=16.6dB0110=17.6dB0111=18.7dB 1000=3.5dB1001=4.5dB1010=5.5dB1011=6.5dB 1100=7.5dB1101=8.5dB1110=9.5dB1111=10.5dB
CF(7:6)	C_G1	11	Selects the coarse input attenuation setting of the first pole of the filter. 00=-13dB01=N/A10=-5.5dB11=0dB

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CF(5)	S_G2_0	1	Selects the gain setting at midband of the second filter stage. 0=-0.7dB1=+7.4dB
CF(4)	S_G2_1	1	Selects the gain setting at midband of the the third filter stage. 0=-6.8dB1=+1dB
CF(3:2)	S_G3	00	Selects the gain setting at midband of the output buffer. 00=2.5dB01=8.4dB10=N/A11=14.3dB
CF(1)	VDS	0	Selects VLIF mode if programmed low. Selects DCR mode if programmed high.
CF(0)	LNA_BYP	0	If set to zero, the LNA is active. If set to one, the LNA is bypassed with a front end gain reduction of: 11.9dB in low band; 10.4dB in high band.

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

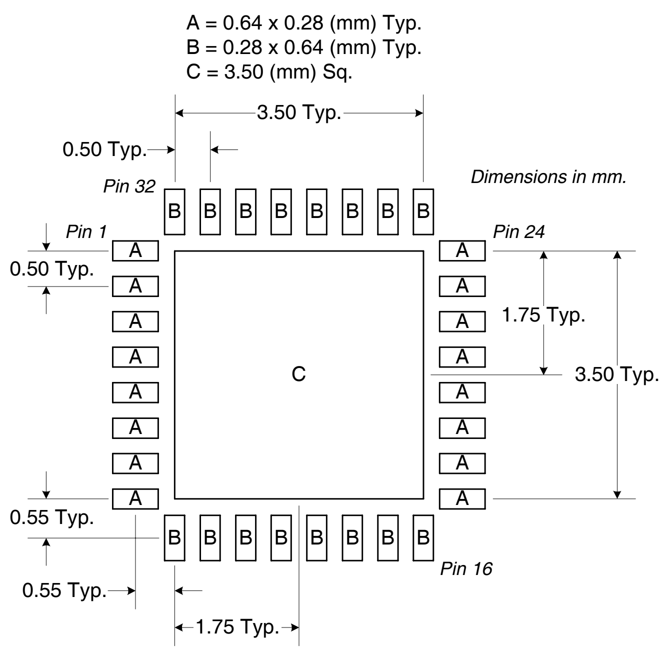

Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

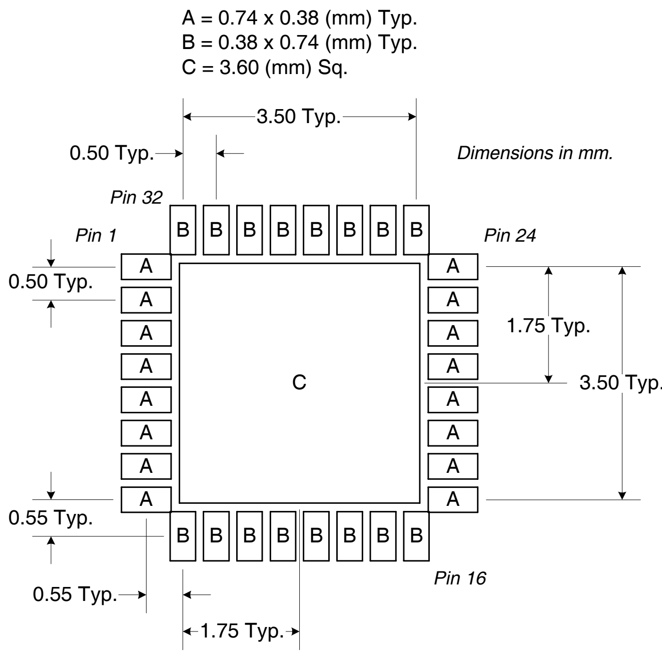

Figure 2. PCB Solder Mask (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern shown has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

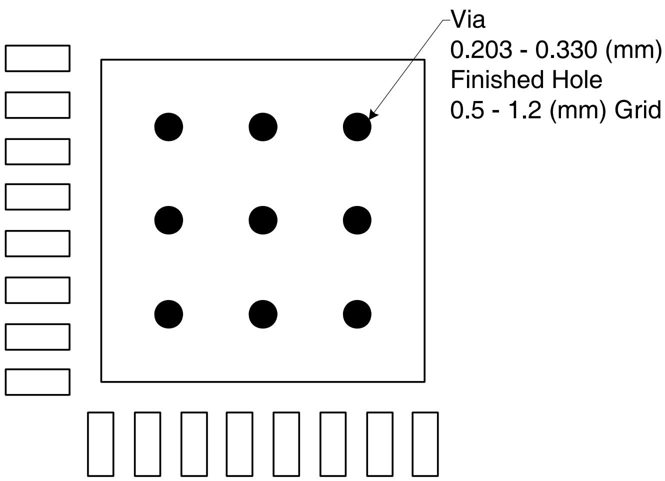

Figure 3. Thermal Pad and Via Design (RFMD Qualification)

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