RF2905

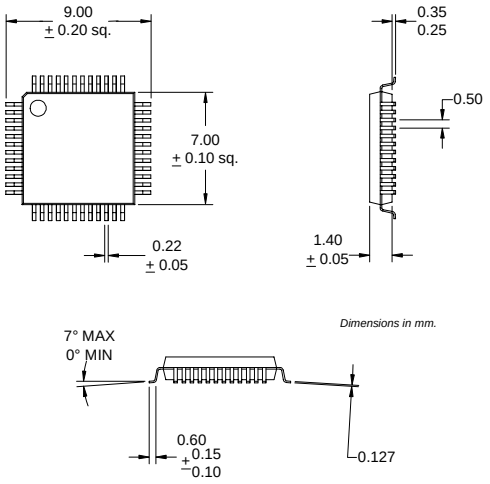
433/868/915MHZ FM/FSK/ASK/OOK TRANSCEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

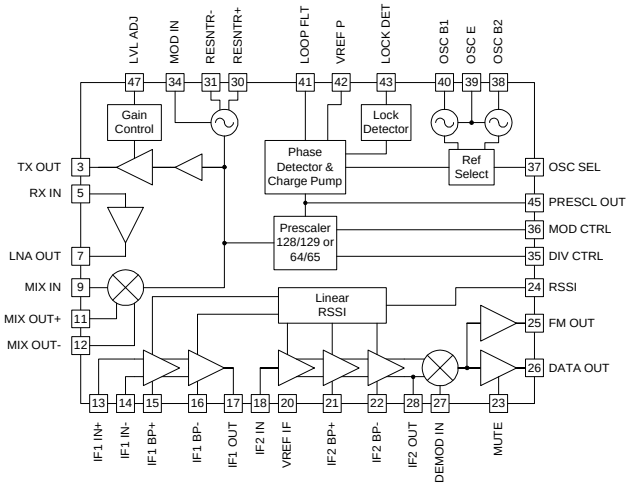
The RF2905 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 7mmx7mm, 48-lead plastic LQFP packaging and is designed to provide a fully functional FM transceiver. The chip is intended for linear (AM, FM) or digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433MHz and 868MHz ISM bands. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator.



Package Style: LQFP-48, 7x7

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS
- [ ] SiGe HBT
- [ ] Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Transceiver
- 2.7V to 5.0V Supply Voltage
- Narrow Band and Wide Band FM/FSK
- 300MHz to 1000MHz Frequency Range
- 10dB Cascaded Noise Figure
- 10mW Output Power at 433MHz

Ordering Information

RF2905	433/868/915MHz FM/FSK/ASK/OOK Transceiver
RF2905 PCBA-L	Fully Assembled Evaluation Board (433MHz)
RF2905 PCBA-M	Fully Assembled Evaluation Board (868MHz)
RF2905 PCBA-H	Fully Assembled Evaluation Board (915MHz)

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

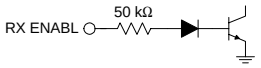
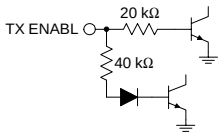
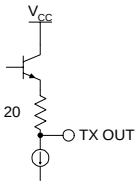
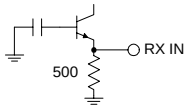
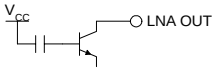
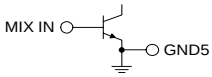
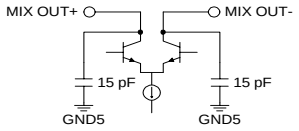
Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

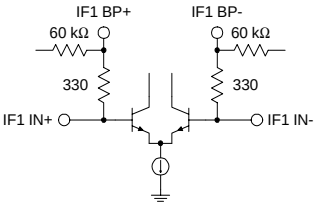
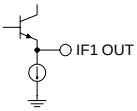
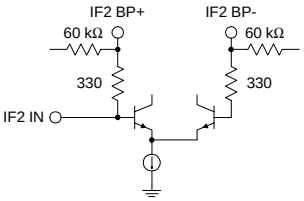
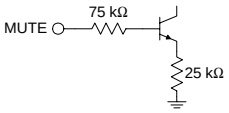
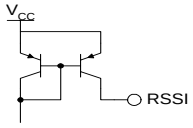
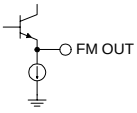
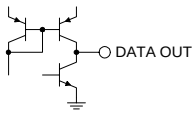
Caution! ESD sensitive device.

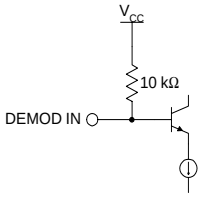
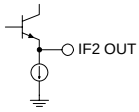
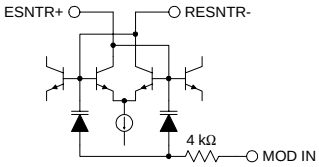
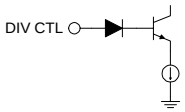
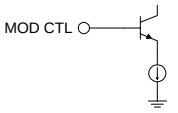
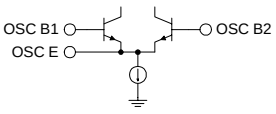
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
Prescaler divide ratio		64/65 or 128/129			
Prescaler Output Impedance		50		Ω	
PLL Phase Noise		-75		dBc/Hz	Freq=915MHz, 10kHz Offset, 5kHz Loop Bandwidth
		-100		dBc/Hz	Freq=915MHz, 100kHz Offset, 5kHz loop Bandwidth
Reference Frequency	TBD		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+10		dBm	Freq=433MHz
	0	+3	8	dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instantaneous frequency deviation is inversely proportional with the modulation voltage
Antenna Port Impedance		50		Ω	TX ENABL="1". RX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity	-95	-101		dBm	IF BW=180kHz, Freq=915MHz, S/N=8dB
LO Leakage			-70	dBm	
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		25		mV/dB	
RSSI Dynamic Range	70	80		dB	

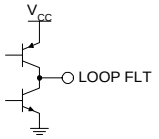
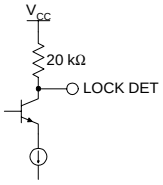
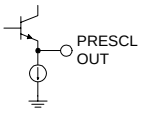
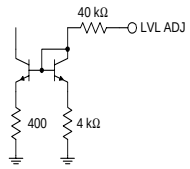
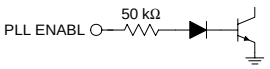
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1". TX ENABL="0"
Antenna Port VSWR			1.5:1		RX Mode
Output Impedance		Open Collector		Ω	433MHz
		Open Collector		Ω	915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		10		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
Maximum Output Voltage				V_{PP}	Balanced
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin
Demod Input Impedance		10		kΩ	
FM Output Impedance		500		Ω	
Data Output Impedance		>1		MΩ	
FM Output Bandwidth	500			kHz	3dB Bandwidth, Dependent upon IF bandwidth and Discriminator.
Data Output Bandwidth	500			kHz	3dB Bandwidth, Z_{LOAD}=1MΩ || 3pF; Dependent upon IF bandwidth and Discriminator.
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ || 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	Z_{LOAD}>10kΩ
FM Output AC Level		200		mV_{PP}	Z_{LOAD}>10kΩ

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Turn On Time			4	ms	Reference Crystal=7.075MHz
Turn Off Time			4	ms	Dependent upon reference crystal. Higher
RX to TX and TX to RX Time			4	ms	frequencies reduce turn on/off times
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption	22	25	34.5	mA	TX Mode, LVL ADJ=3.6V
	8	10	13.5	mA	TX Mode, LVL ADJ=0V
	7	9	12	mA	RX Mode
			1	µA	Power Down Mode which sets: PLL ENABL, TX ENABL, RX ENABL, LVL ADJ, OSC SEL, and MUTE=0V
	5.3	8	10	mA	PLL Only Mode

Pin	Function	Description	Interface Schematic
1	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	
2	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
3	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
4	GND2	Ground connection for the 40dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
5	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
6	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
7	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output.	
8	GND3	Same as pin 4.	
9	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
10	GND5	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
11	MIX OUT+	Complementary (with respect to pin 12) IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
12	MIX OUT-	IF output from the RF mixer. For a balanced mixer output, pull-up inductors from pin 11 and 12 to V_{CC} and a capacitor between the pins should be used. The sum of the total pull-up inductance should be used to resonate the capacitor between pins 11 and 12. DC blocking capacitors of 10nF can then be used to connect the balanced output to IF1 IN+ (pin 13) and IF1 IN- (pin 14).	See pin 11.

Pin	Function	Description	Interface Schematic
13	IF1 IN+	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
14	IF1 IN-	Functionally the same as pin 13 except inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 13.
15	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
16	IF1 BP-	Same as pin 15.	See pin 13.
17	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 IN	Balanced IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
19	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
20	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	
21	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 18.
22	IF2 BP-	Same as pin 21.	See pin 18.
23	MUTE	This pin is used to mute the data output (DATA OUT). MUTE>2.0V turns the DATA OUT signal on. MUTE<1.0V turns the DATA OUT signal off. The MUTE signal should be logic low in the Sleep Mode.	
24	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.5V, into 51kΩ load, and increases with increasing signal strength.	
25	FM OUT	Linear output from the FM demodulator. This pin is used in analog applications when signal fidelity is important. This output is inverted for low side injection of the LO and normal for high side injection.	
26	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater. When using a RF2905 transmitter and receiver back to back a data inversion will occur, when the LO is low side injected. A high side injection will add an inversion of the Rx data.	

Pin	Function	Description	Interface Schematic
27	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
28	IF2 OUT	Balanced IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 27 through a 4pF (suggested) capacitor and an FM discriminator circuit.	
29	VCC6	This pin is used is supply DC bias to the second IF amplifier, Demodulator and Data Slicer. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
30	RESNTR+	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 31 although a small imbalance can be used to tune in the proper frequency range.	
31	RESNTR-	See RESNTR+ description.	See pin 30.
32	VCC2	This pin is used is supply DC bias to the VCO, prescaler, and PLL. An RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
33	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	
34	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 30.
35	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic high (DIVCTRL>2.0V) selects the 64/65 divisor. A logic low (DIVCTRL<1.0V) selects the 128/129 divisor.	
36	MOD CTRL	This pin is used to select the prescaler modulus. A logic high (MOD CTRL>2.0V) selects 64 or 128 for the prescaler divisor. A logic low (MOD CTRL<1.0V) selects 65 or 129 for the prescaler divisor. Due to design timing constraints, the prescaler in the divide by 65 or 129 modes has a limited frequency range for accurate operation. These two modes are not recommended for use from 400MHz to 460MHz.	
37	OSC SEL	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
38	OSC B2	This pin is connected directly to the reference oscillator 2 transistor base. The intended reference oscillator configuration is a modified Colpitts.	

Pin	Function	Description	Interface Schematic
39	OSC E	This pin is connected directly to the emitter of the reference oscillator transistors.	See pin 38.
40	OSC B1	This pin is connected directly to the reference oscillator 1 transistor base. The intended reference oscillator configuration is a modified Colpitts.	See pin 38.
41	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
42	VREF P	Bypass pin for the prescaler reference voltage. A 33nF capacitor to ground is needed to suppress reference spurs in the device. This value may be different for different PCB arrangements.	
43	LOCK DET	This pin provides an analog output indicating the lock status of the PLL. The amplitude of this signal is typically 200mV$_{PP}$ around a DC level of V_{CC}-0.1V.	
44	VCC1	This pin is used to supply DC bias to the LNA, Mixer, first IF Amp, and Bandgap reference. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
45	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
46	VCC3	This pin is used to supply DC bias and collector current to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 68pF capacitor is recommended for 433MHz applications.	
47	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
48	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLLENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLLENABL<1.0V) powers down the PLL and VCO.	

RF2905 Theory of Operation and Application Information

The RF2905 is a part of a family of low-power RF transceiver IC's that was developed for wireless data communication devices operating in the European 433/868MHz ISM bands or 915MHz US ISM band.This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products.

In its basic form, the RF2905 can implement a two-way half duplex FSK transceiver with the addition of some crystals, filters, and passive components. There are two reference crystals that allow for the transmit carrier and the receiver LO to be independently generated with a common PLL and VCO. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters but has a -3dB bandwidth of 25MHz and can still be used (with lower gain) at higher frequency with the other type of filters. The PA output and LNA input are available on separate pins and are designed to be connected together through a DC blocking capacitor. In the Transmit mode, the PA will have a 50Ω impedance and the LNA will be a high impedance. In Receive mode, the LNA will have a 50Ω interface and the PA will have a high impedance. This eliminates the need for a TX/RX switch and allows a single RF filter to be used in transmit and receive modes. Separate access to the PA and LNA allow the RF2905 to interface with external components such as higher power PA's, lower NF LNA's, upconverters, and downconverters for a variety of implementations.

FM/FSK SYSTEMS

The MOD IN pin drives an internal varactor for modulating the VCO. This pin can be driven with a voltage level needed to generate the desired deviation. This voltage can be carried on a DC bias to select the desired slope (deviation/volt) for FM systems. Or, a resistor divider network referenced to Vcc or ground can divide down logic level signals to the appropriate level for a desired deviation in FSK systems.

On the receiver demod, two outputs are available, an analog FM output and a digital FSK output. The FM output is a buffered signal coming off of the quadrature demodulator. The digital output is generated by a data slicer that is DC coupled differentially to the demodulator. An on-chip 1.6MHz RC filter is provided at the demodulator output to filter the undesired 2xIF product. This balanced data slicer has a speed advantage over a conventional adaptive data slicer where a large capacitor is used to provide DC reference for bit decision. Since the balanced data slicer does not have to charge a large capacitor, the RF2905 exhibits a very fast response time. For best operation of the on-chip data slicer, FM deviation needs to exceed the carrier frequency error anticipated between the receiver and transmitter with margin.

The data slicer itself is a transconductance amp and the DATA OUT pin is capable of driving rail to rail output only into a very high impedance and small capacitance. The amount of capacitance will determine the bandwidth of the DATA OUT. At a 3pF load, the bandwidth is in excess of 500kHz. The rail to rail output of the data slicer is also limited by the frequency deviation and bandwidth of the IF filters. With the 180kHz bandwidth filters on the eval boards, the rail to rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation vs. data rate (mod index) is important in evaluating the applicability of the RF2905 for a given data rate.

While this type of data slicer is best for wideband deviation, it can also work for narrowband if care is taken to minimize frequency differences. By loading down the DATA OUT pin, the output will be limited to a small data signal on a DC carrier. With this signal, an external data slicer can be used to achieve higher data rates or improve performance in narrow deviations. Alternatively, an AFC loop can be added to correct for frequency errors with a few external components.

For FM or FSK modulation, an internal varactor is used to directly modulate the VCO with the baseband data. The primary consideration when directly modulating the VCO is the data rate verses PLL loop bandwidth. The PLL will track out the modulation to the extent of its loop bandwidth which distorts the modulating data. Therefore, the lower frequency components of the modulating data should be 5 to 10 times the loop bandwidth to minimize the distortion. The lower frequency components are generated by long strings of 1's or 0's in the data stream. By limiting the number of consecutive, same bits, the lower frequency component can be set. In addition, the data stream should be balanced to minimize distortion. Using a coding pattern such as Manchester is highly recommended to optimize system performance.

The PLL loop bandwidth is important in several other system parameters. For example, switching from transmit to receive requires the VCO to retune to another frequency. The switching speed is proportional to the loop bandwidth, the higher the loop bandwidth, the

faster the switching times. Phase noise of the VCO is another factor. Phase noise outside of the loop bandwidth is due to the noise of the VCO itself rather than the crystal reference. A design trade-off must be made here in selecting a PLL loop bandwidth with acceptable phase noise and switching characteristics and minimal distortion of the modulation data.

AM/ASK SYSTEMS

The transmitter of the RF2905 has an output power level adjustment (LVL ADJ) that can be used to provide approximately 18dB of power control for amplitude modulation. The RSSI output of the receiver section can be used to recover the modulation. The RSSI output is from a current source and needs to have a resistor to convert to a voltage. A 51kΩ resistive load will produce an RSSI voltage of 0.7V to 2.5V, typically. A parallel capacitor is suggested to limit the bandwidth and filter noise. For ASK applications, the 18dB range of the LVL ADJ does not produce enough voltage swing in the RSSI for reliable communication. The On-Off keying (OOK) is suggested to provide reliable communications. To achieve this, both the LVL ADJ and TX ENABL need to be controlled together (please note that LVL ADJ cannot be left high when TX ENABL is low). This will provide a on/off ratio of >50dB. One unfortunate consequence of modulating this way is VCO pulling by the power amp. This results in a spurious output outside the desired transmit band as the PLL momentarily loses lock and reacquires. This can be avoided by pulse shaping the TX data to slow the change in the VCO load to a pace that the PLL can track with its given loop bandwidth. The loop bandwidth can also be increased to allow it to track faster changes due to load pulling.

For the ASK/OOK receiver demodulator, an external data slicer is required. The RSSI output is used to provide both the filtered data and a very low pass filtered (relative to the data rate) DC reference to a data slicer. Because the very low pass filter has a slow time constant, a longer preamble may be required to allow for the DC reference to get to a stable state. Here, as in the case of the FSK transmitter, the data pattern also affects the DC reference and the reliability of the received data. Again, a coding scheme such as Manchester such should be used to improve data integrity.

APPLICATION AND LAYOUT CONSIDERATIONS

Both the RX IN and TX OUT have a DC bias on them. Therefore, DC blocking caps are required. If the RF filter has DC blocking characteristics like a ceramic dielectric filter, then only 1 DC blocking capacitor would be needed to separate the DC of RX IN and TX OUT. These are RF signals and care should be taken to route these signals keeping them physically short. Because of the 50Ω/high impedance nature of these two signals, they may be connected together into a signal 50Ω device such as a filter. An external LNA or PA can be used, if desired, but an external RX/TX switch may be required.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO either radiated or coupled by traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2905 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible. Figure 1 is a recommended layout pattern for the VCO components. When using loop bandwidths lower than the 5kHz shown on the eval board, better filtering of the Vcc at the resonators (and lower Vcc noise as well) will help reduce phase noise of the VCO. A series resistor of 100Ω to 200Ω and a 1μF or larger capacitor can be used.

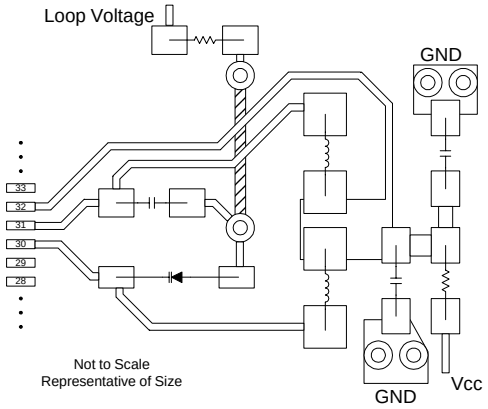


Figure 1. Recommended VCO Layout

For the interface between the LNA/mixer, the coupling capacitor should be as close to the RF2905 pins as possible with the bias inductor being further away. Once again, the value of the inductor can be changed to compensate to trace inductance. The output impedance of the LNA is in the order of several kΩ which makes matching to 50Ω very hard. If image filtering is desired, a high impedance filter is recommended.

The quad tank of the discriminator can be implemented with ceramic discriminators available from a couple of sources. This design works well for wideband applications and where the temperature range is limited. The temperature coefficient of a ceramic discriminator can be in the order of +/- 50ppm per degree C. An automatic frequency control loop can be implemented using the DC level of the FM OUT for feedback to an external varactor on the reference crystal. An alternative to the ceramic discriminator is a LC tank. Figure 2 shows a schematic implementation of a LC tank.

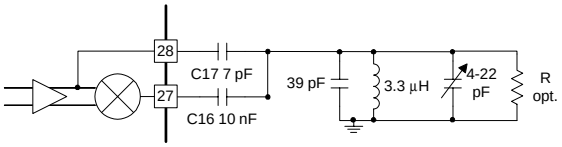


Figure 2. LC Type Discriminator Circuit

The DEMOD IN pin has a DC bias on it and must be DC blocked. This can be done either at the pin or at the ground side of the LC tank (this must also be done if a parallel resistor is used with a ceramic discriminator). The decision whether to used a LC or a ceramic discriminator should be based upon the frequency deviation in the system, discriminator Q needed, and frequency and temperature tolerances. Tuning of the LC tank is required to overcome the component tolerances in the tank.

PREDICTING AND MINIMIZING PLL LOCK TIME

The RF2905 implements a conventional PLL on chip, with a VCO followed by a prescaler dividing the output frequency down to be compared with a signal from the reference oscillator. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF29.5 is:

$$\text{Lock time} = D/fc + 35000*C*dV$$

Where D is a factor to account for the loop damping. For loops with low phase margin (30° to 40°), use D=2 whereas for loops with better phase margin (50° to 60°), use D=1. fc is the loop cut frequency. C is the sum of all shunt capacitors in the loop filter. dV is the required step voltage change to produce the desired frequency change during the transient.

To lock faster, we need to minimize C.

1. To this end, use the divide by 128 rather than the 64, and a correspondingly lower frequency reference crystal to achieve the desired output frequency.
2. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.
3. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

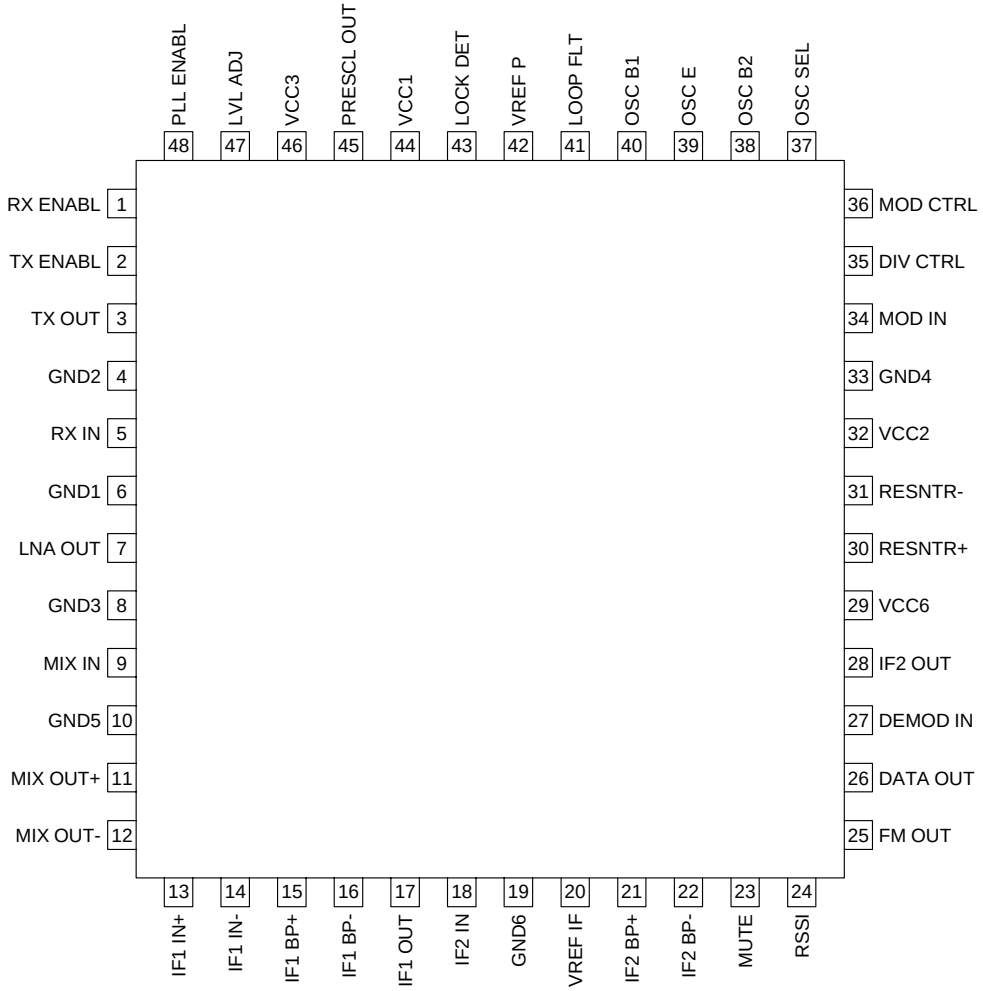
CRYSTAL SELECTION

Several issues arise in the selection of the crystals. Timing specifications such as start-up and switching are related to the crystal specifications, as well as external circuitry. The tolerance of the crystals are also an issue in optimum radio performance. In general, tighter tolerance crystals lead to better performance and are more critical to higher data rates. Frequency offsets between the TX crystal, RX crystal and discriminator generate duty cycle variations in the receive demodulator.

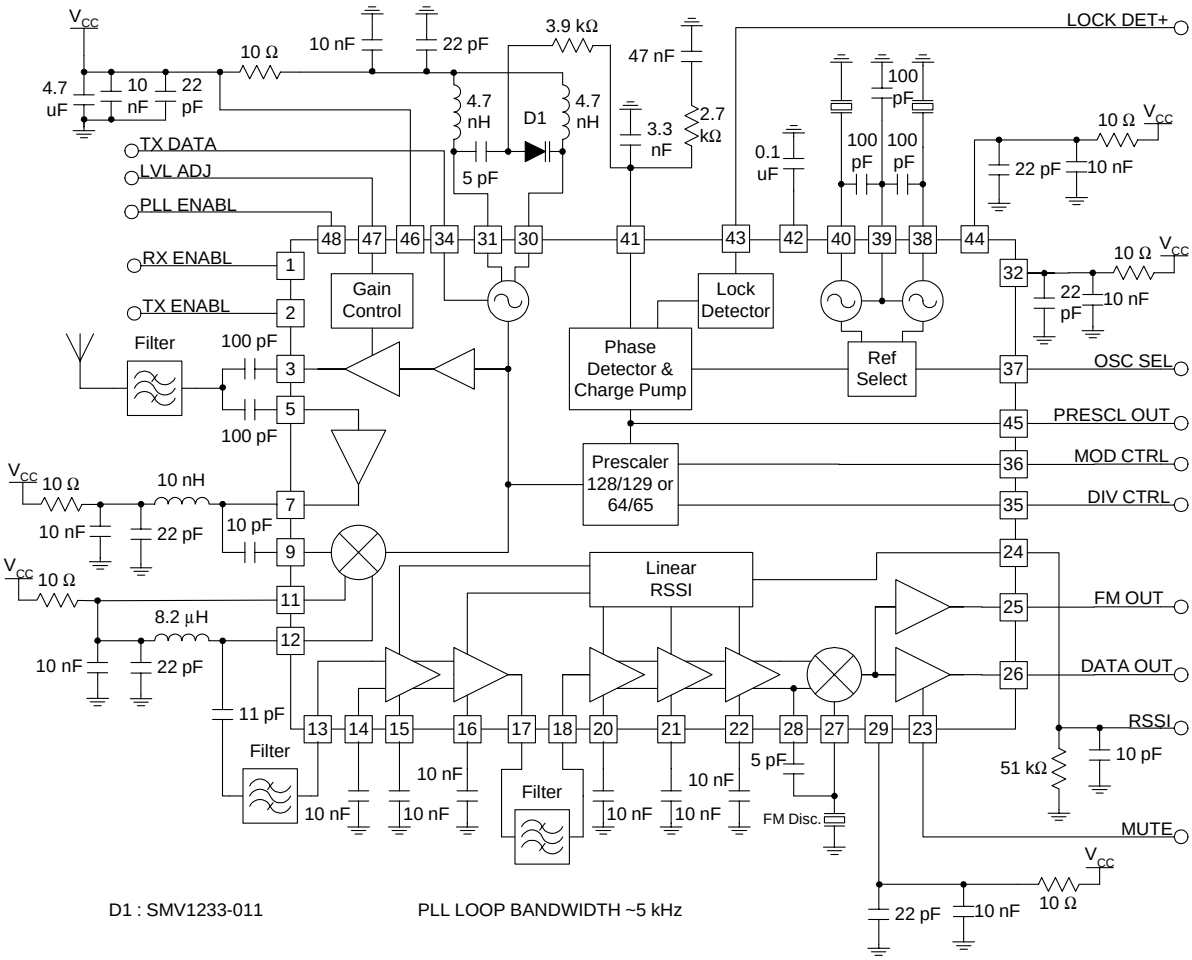
The crystals used on the RF2905 evaluation boards are specified as a parallel resonant, 30pF crystal with a maximum ESR of 80Ω. The initial tolerance is ±20ppm and temperature stability is ±30ppm for -10°C to 70°C. The transistor oscillator will work with a variety of different crystals and the final crystal specifications should be evaluated for each application.

Faster start-up or switching times are achievable by specifying crystals with low motion inductance and low motional resistance. Additionally, the feedback caps of the oscillator can be changed to increase the voltage on the crystal. Generally, crystals in the leaded HC-49U packages will provide better start-up times than the smaller surface-mount types used on the evaluation board.

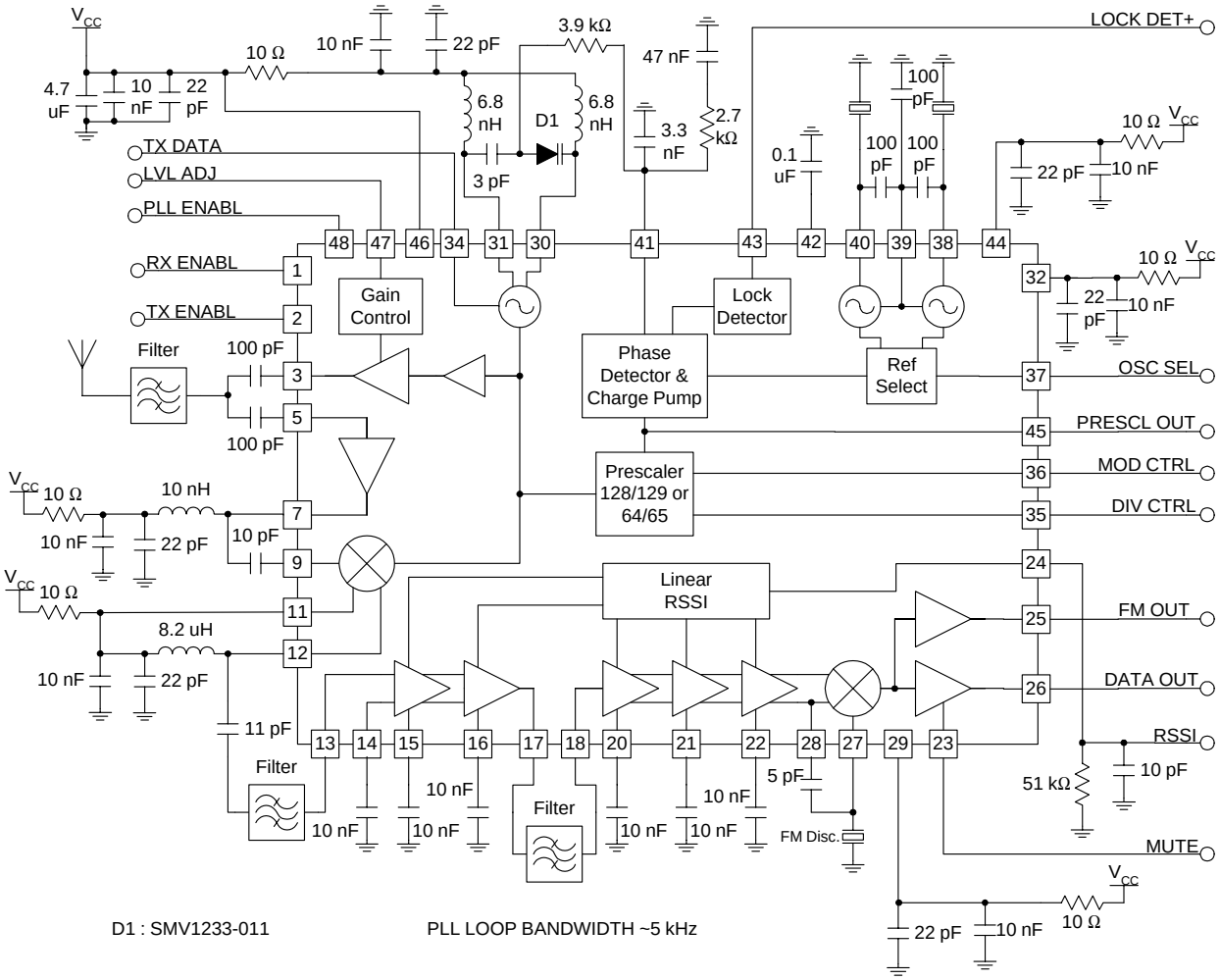
Pin Out


PLL ENABL 48
LVL ADJ 47
VCC3 46
PRESCL OUT 45
VCC1 44
LOCK DET 43
VREF P 42
LOOP FLT 41
OSC B1 40
OSC E 39
OSC B2 38
OSC SEL 37
RX ENABL 1
TX ENABL 2
TX OUT 3
GND2 4
RX IN 5
GND1 6
LNA OUT 7
GND3 8
MIX IN 9
GND5 10
MIX OUT+ 11
MIX OUT- 12
36 MOD CTRL
35 DIV CTRL
34 MOD IN
33 GND4
32 VCC2
31 RESNTR-
30 RESNTR+
29 VCC6
28 IF2 OUT
27 DEMOD IN
26 DATA OUT
25 FM OUT
13 IF1 IN+
14 IF1 IN-
15 IF1 BP+
16 IF1 BP-
17 IF1 OUT
18 IF2 IN
19 GND6
20 VREF IF
21 IF2 BP+
22 IF2 BP-
23 MUTE
24 RSSI

Application Schematic
915MHz



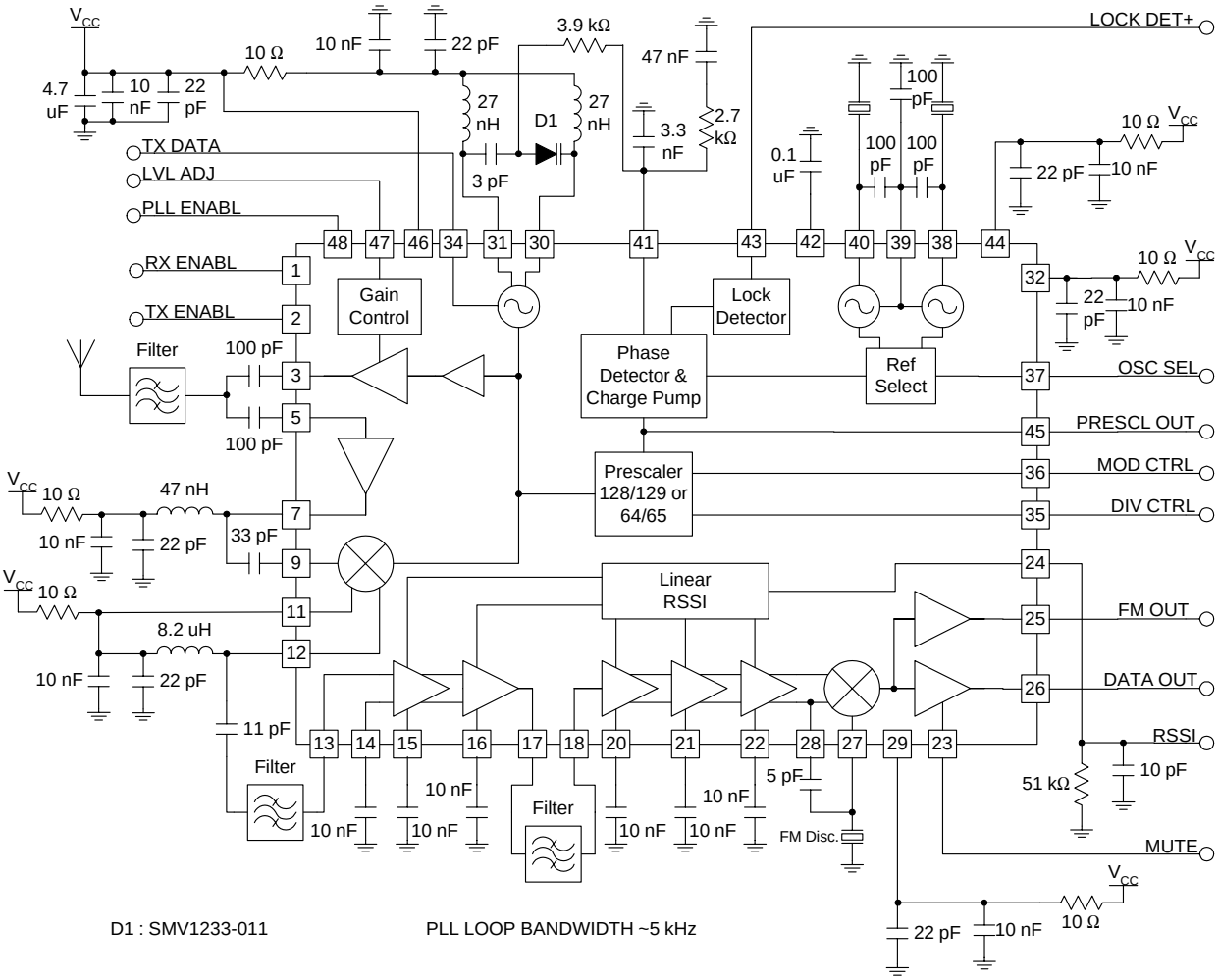
Application Schematic
868MHz



D1 : SMV1233-011

PLL LOOP BANDWIDTH ~5 kHz

Application Schematic
433MHz

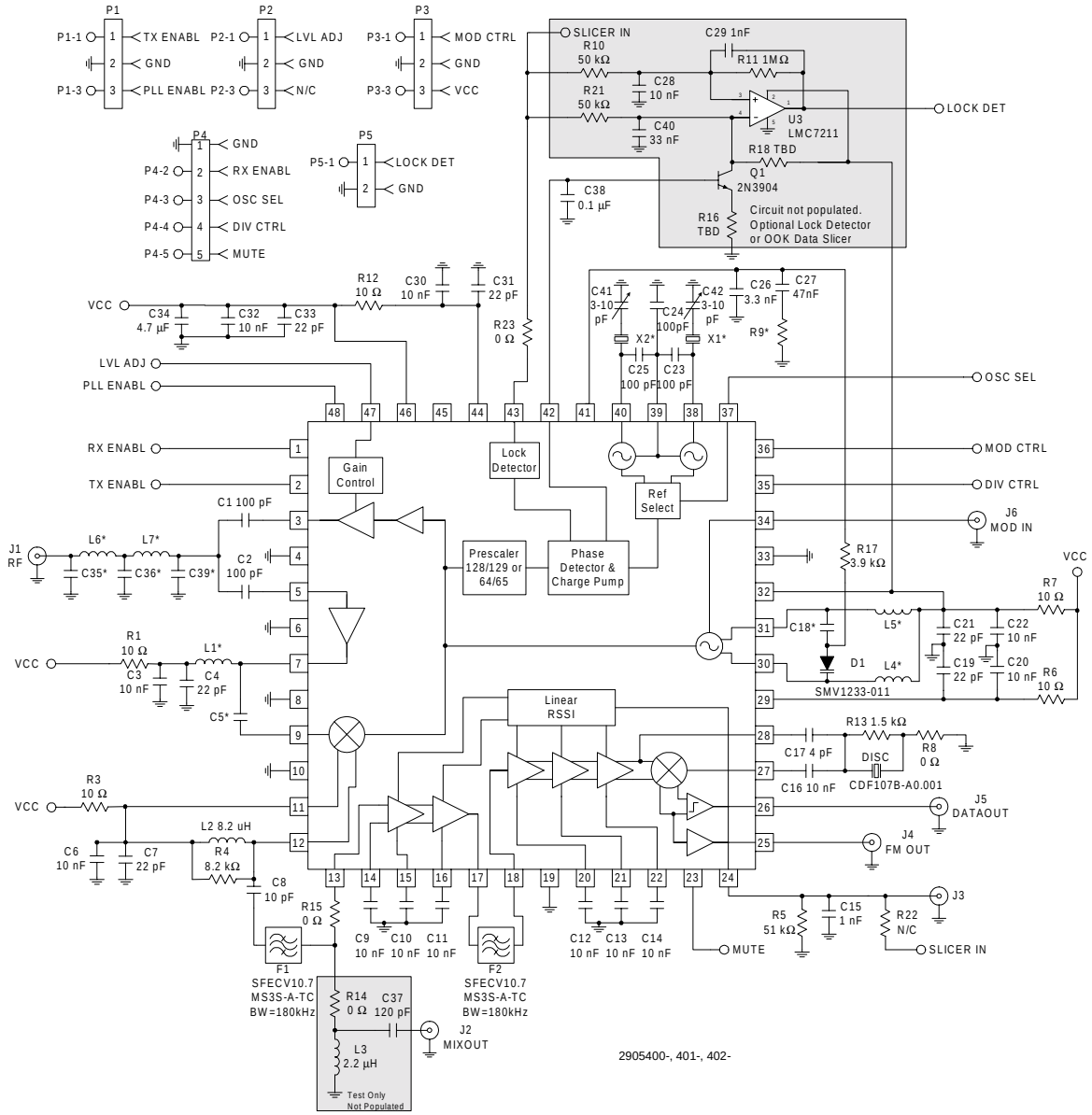


D1 : SMV1233-011

PLL LOOP BANDWIDTH ~5 kHz

Evaluation Board Schematic

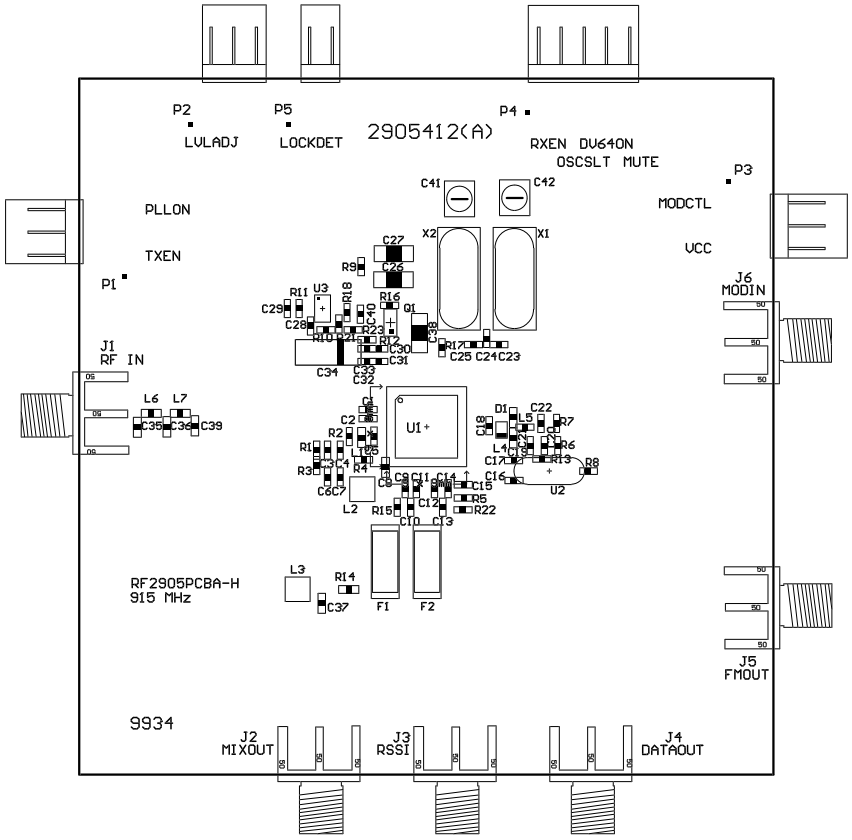
(Download Bill of Materials from www.rfmd.com.)

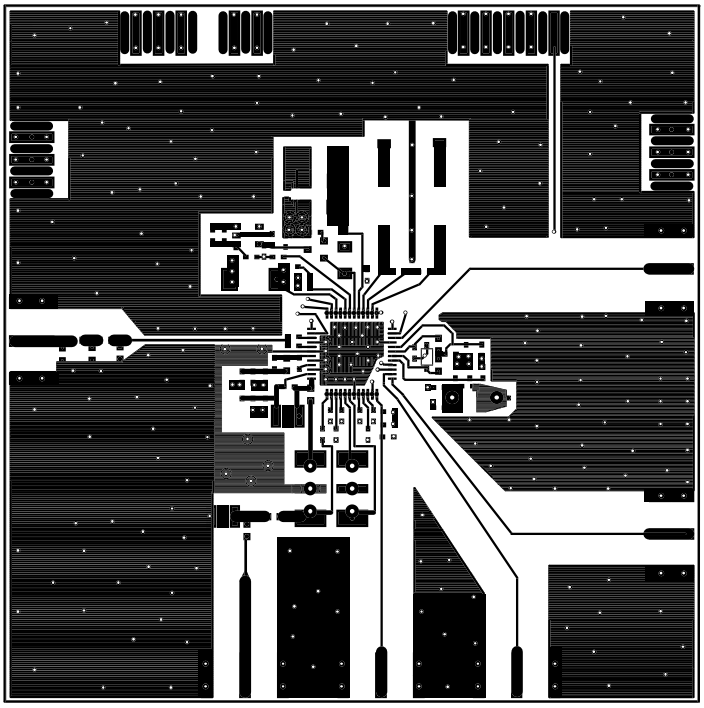


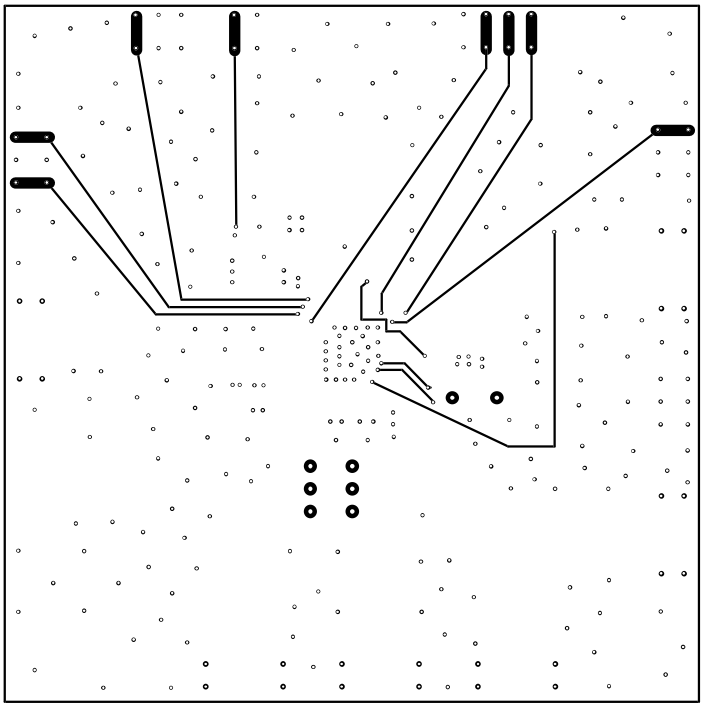
Board	C35 (pF)	L6 (nH)	L7 (nH)	C39 (pF)	L1 (nH)	C5 (pF)	C18 (pF)	L4,L5(nH)	R9 (kΩ)	X1 (MHz)	X2 (MHz)
L (433MHz)	8	22	22	8	47	35	3	27	2.4	6.78	6.612
M (868MHz)	4	8.2	Jumper	N/C	10	10	5	4.7	2.7	13.577344	13.410156
H (915MHz)	4	8.2	Jumper	N/C	10	10	5	4.7	2.7	7.15909	7.07549

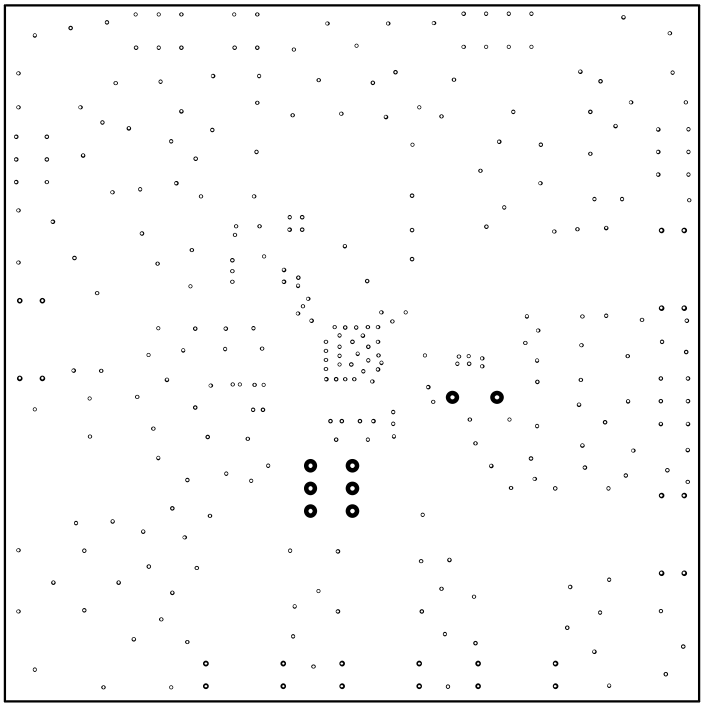
Evaluation Board Layout
Board Size 3.05” x 3.05”

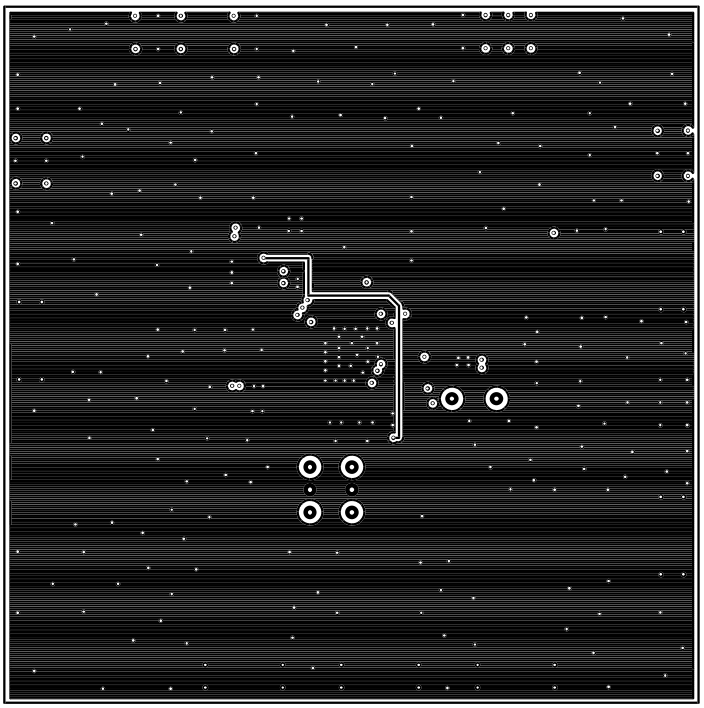
Board Thickness 0.031”, Board Material FR-4, Multi-Layer
(Same board layout is used for the -L, -M, and -H versions.)

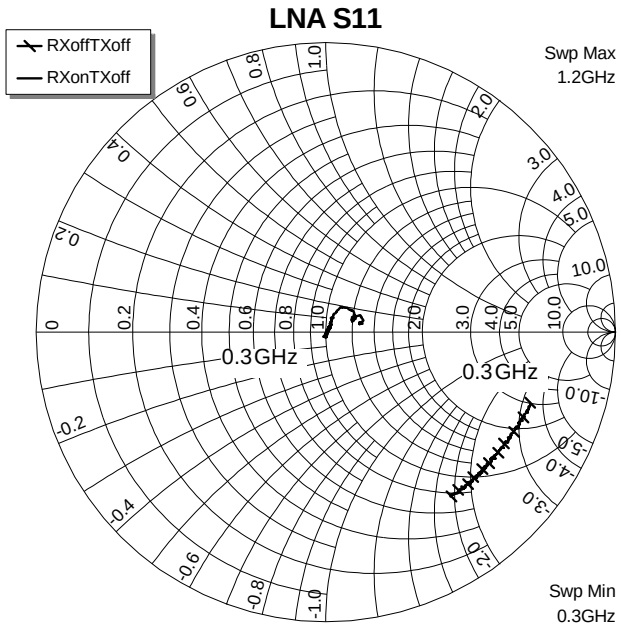


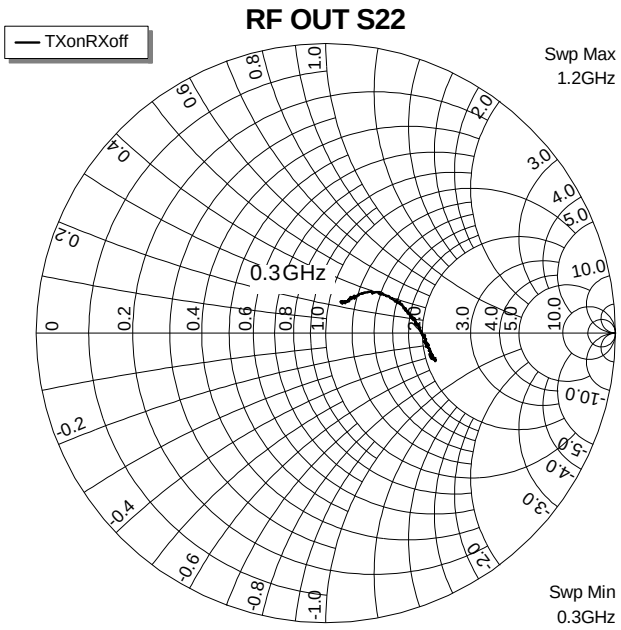




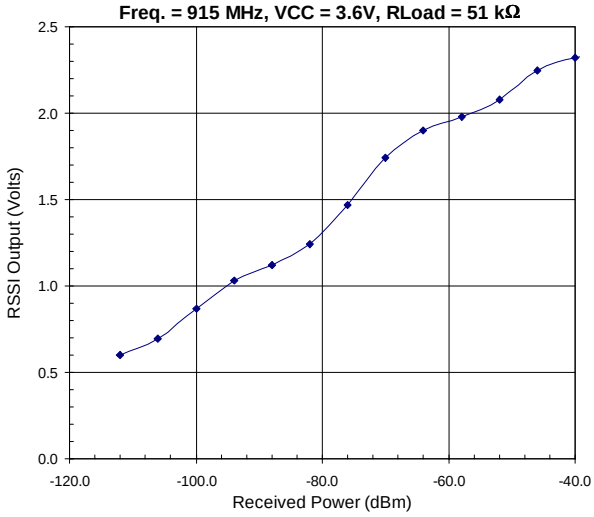




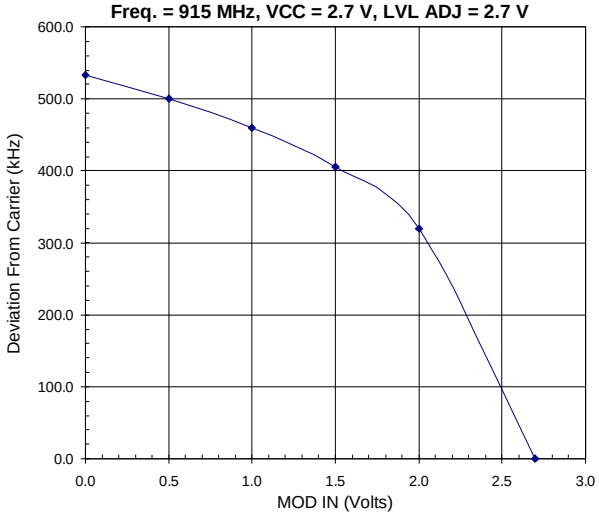

LNA S11
RXoffTXoff
RXonTXoff
Swp Max
1.2GHz
0.3GHz
0.3GHz
Swp Min
0.3GHz


RF OUT S22
TXonRXoff
Swp Max
1.2GHz
0.3GHz
Swp Min
0.3GHz

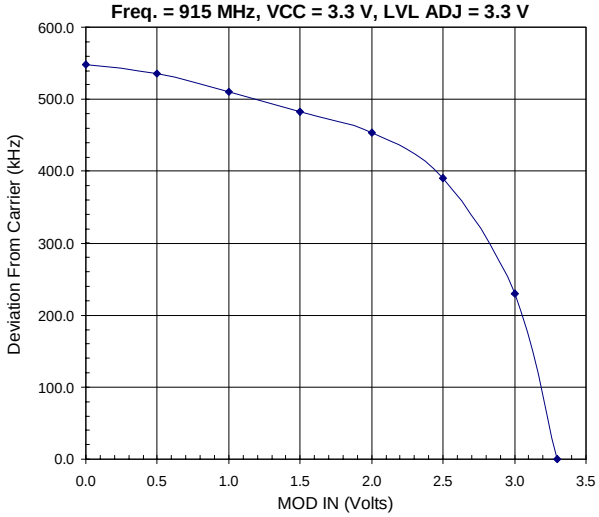
RSSI
Freq. = 915 MHz, VCC = 3.6V, RLoad = 51 kΩ



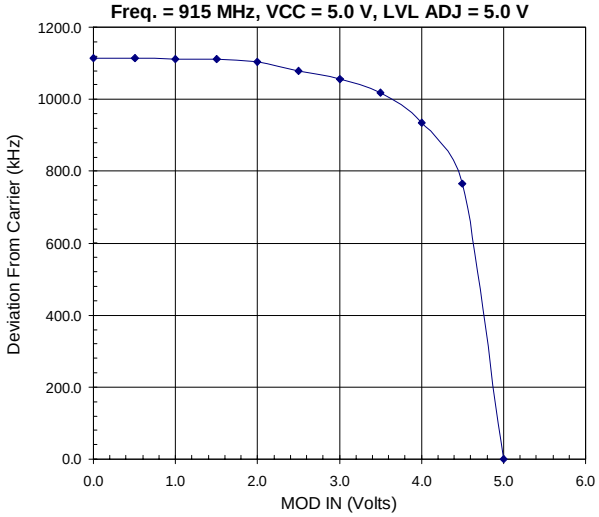
Modulation Deviation
Freq. = 915 MHz, VCC = 2.7 V, LVL ADJ = 2.7 V

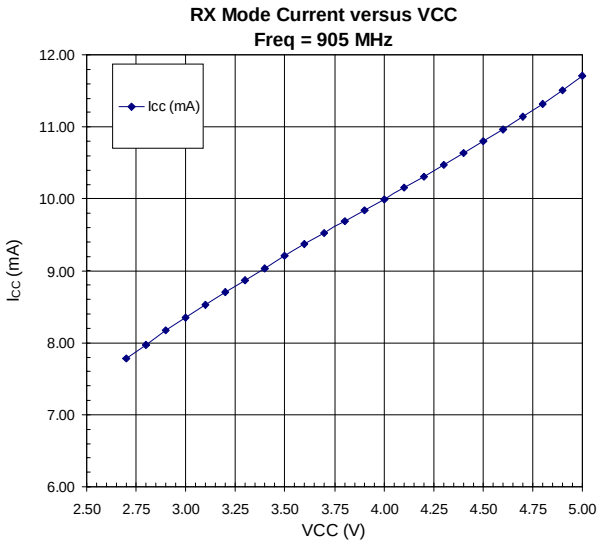


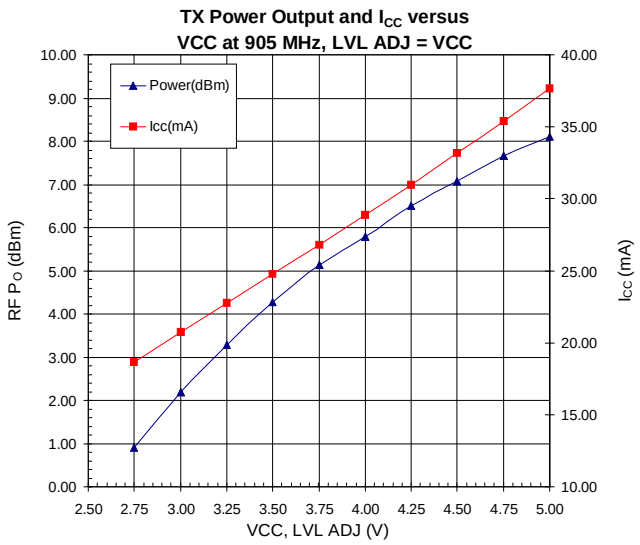
Modulation Deviation
Freq. = 915 MHz, VCC = 3.3 V, LVL ADJ = 3.3 V

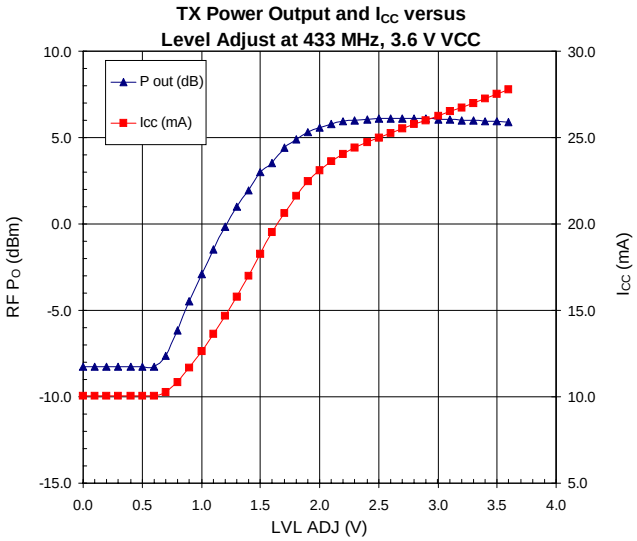


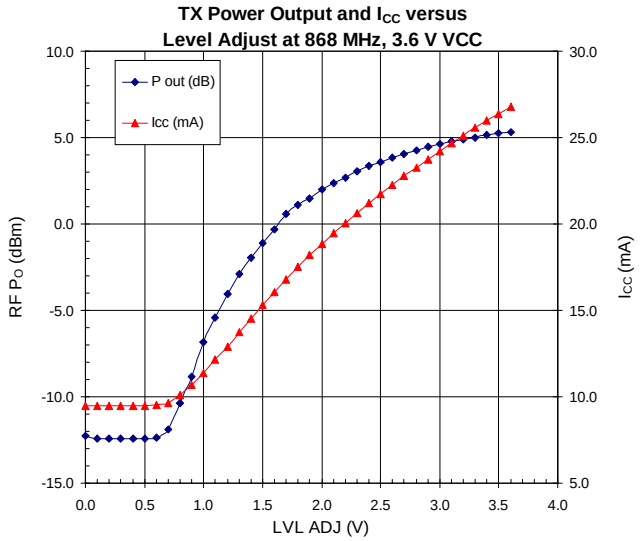
Modulation Deviation
Freq. = 915 MHz, VCC = 5.0 V, LVL ADJ = 5.0 V

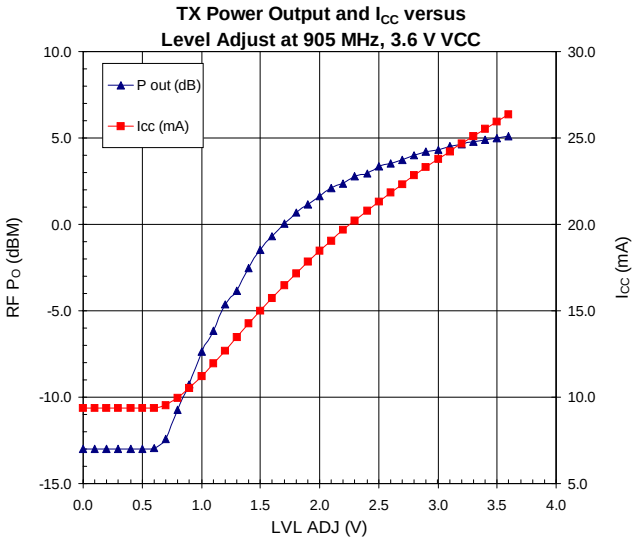



RX Mode Current versus VCC
Freq = 905 MHz
Icc (mA)
ICC (mA)
VCC (V)


TX Power Output and ICC versus
VCC at 905 MHz, LVL ADJ = VCC
Power(dBm)
Icc(mA)
RF PO (dBm)
ICC (mA)
VCC, LVL ADJ (V)


TX Power Output and ICC versus
Level Adjust at 433 MHz, 3.6 V VCC
P out (dB)
Icc (mA)
RF PO (dBm)
ICC (mA)
LVL ADJ (V)


TX Power Output and ICC versus
Level Adjust at 868 MHz, 3.6 V VCC
P out (dB)
Icc (mA)
RF PO (dBm)
ICC (mA)
LVL ADJ (V)


TX Power Output and ICC versus
Level Adjust at 905 MHz, 3.6 V VCC
P out (dB)
Icc (mA)
RF PO (dBM)
ICC (mA)
LVL ADJ (V)