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RF5125

3V TO 5V, 2.4GHz TO 2.5GHz LINEAR POWER AMPLIFIER

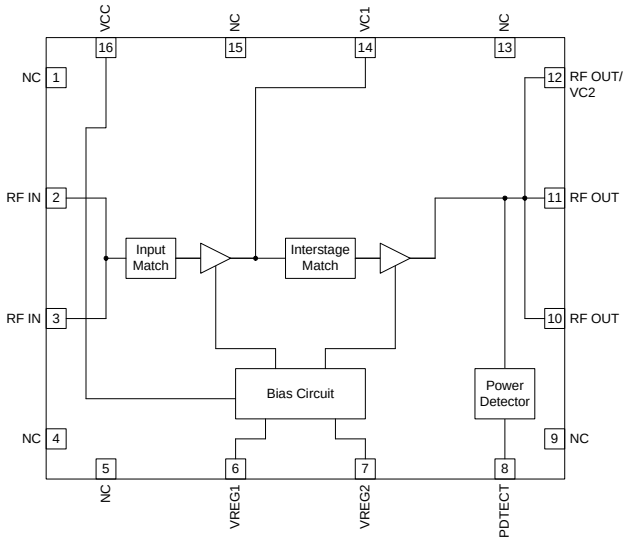
RoHS Compliant & Pb-Free Product
Package Style: QFN, 16-Pin, 3 x 3

Features

- Single Power Supply 3.0V to 5.0V
- +21dBm, <4.0% EVM, 185mA@V_{CC}=3.3V
- 28dB Typical Small Signal Gain
- 50Ω Input and Interstage Matching
- 2400MHz to 2500MHz Frequency Range
- +23dBm, <4% EVM, 250mA@V_{CC}=5.0V

Applications

- IEEE802.11b/g/n WLAN Applications
- 2.5GHz ISM Band Applications
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- Spread-Spectrum and MMDS Systems



Functional Block Diagram

Product Description

The RF5125 is a linear, medium-power, high-efficiency, two-stage amplifier IC designed specifically for battery-powered WLAN applications such as PC cards, mini PCI, and compact flash applications. The device is manufactured on an advanced InGaP Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz OFDM and other spread-spectrum transmitters. The device is provided in a 3mmx3mm, 16-pin, QFN with a backside ground. The RF5125 is designed to maintain linearity over a wide range of supply voltage and power output.

Ordering Information

RF5125	3V to 5V, 2.4GHz to 2.5GHz Linear Power Amplifier
RF5125PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{REG})	-0.5 to 3.5	V
DC Supply Current	600	mA
Input RF Power	+5	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC Level 2	

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall - 54Mbps OFDM Signal					T=+25°C, V_{CC}=3.3V, V_{REG}=2.8V, Freq=2450MHz, circuit per evaluation board schematic.
Frequency Range		2400 to 2500		MHz	
Maximum Linear Output Power					With 802.11g modulation (54Mbit/s) meeting 802.11g spectral mask.
V_{CC}=3.3V	20.0	21.0	22.0	dBm	
V_{CC}=5.0V	22.0	23.0	24.0	dBm	
EVM	2.0	3.0	4.0	%	P_{OUT}=+21dBm, 54M OFDM, V_{CC}=3.3V_{DC}
	2.0	3.5	4.0	%	P_{OUT}=+23dBm, 54M OFDM, V_{CC}=5.0V_{DC}
Gain	26	29	33	dB	P_{OUT}=+21dBm, 54M OFDM, V_{CC}=3.3V_{DC}
Input Impedance	49	50	51	Ω	Internally Matched Input and Interstage
Output VSWR			10:1		No spurs above -43dBm
Power Detector (P_detect)					
P_{OUT}=8dBm	0.2	0.22	0.25	V_{DC}	V_{CC}=3.3V
P_{OUT}=21dBm	0.85	1.05	1.2	V_{DC}	V_{CC}=3.3V
P_{OUT}=23dBm		1.3		V	V_{CC}=5.0V
Power Supply					
Operating Voltage	3.0	3.3	3.6	V_{DC}	5V operation requires output match revision
V_{REG} (Bias) Voltage (V_{REG1}, V_{REG2})	2.7	2.8	3.0	V_{DC}	
Current Consumption	170	185	220	mA	RF P_{OUT}=+21dBm, V_{CC}=3.3V, 54Mbps OFDM
		250			RF P_{OUT}=+23dBm, V_{CC}=5.0V, 54Mbps OFDM
Quiescent Current		95		mA	RF=OFF
Leakage Current	10	25	150	nA	V_{CC}=+3.3V_{DC}; RF In=OFF; V_{REG} OFF
V_{REG} (Bias) Current (Total)	1	2	5	mA	V_{CC}=3.3V
	1	2	6	mA	V_{CC}=5.0V

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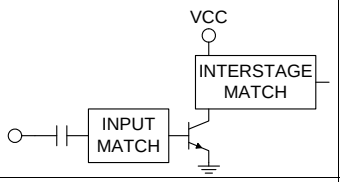
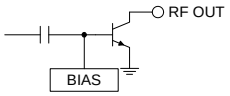
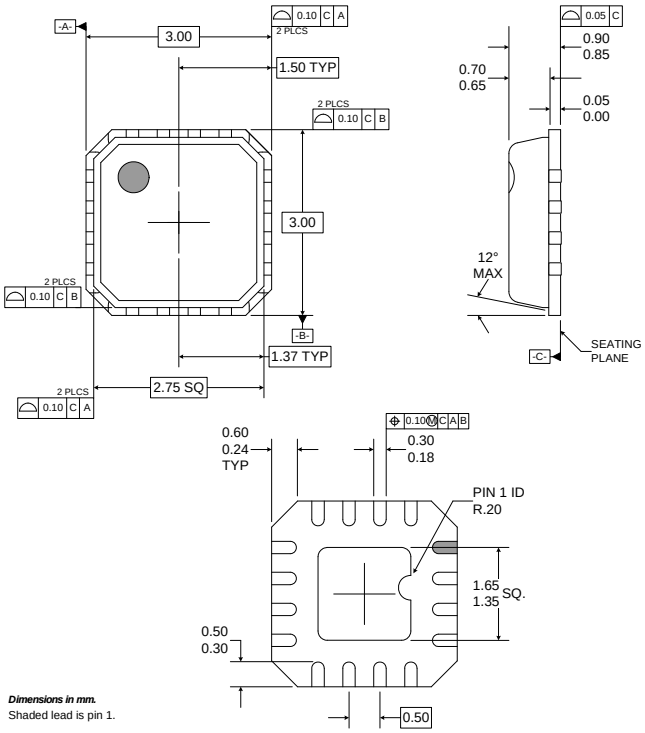
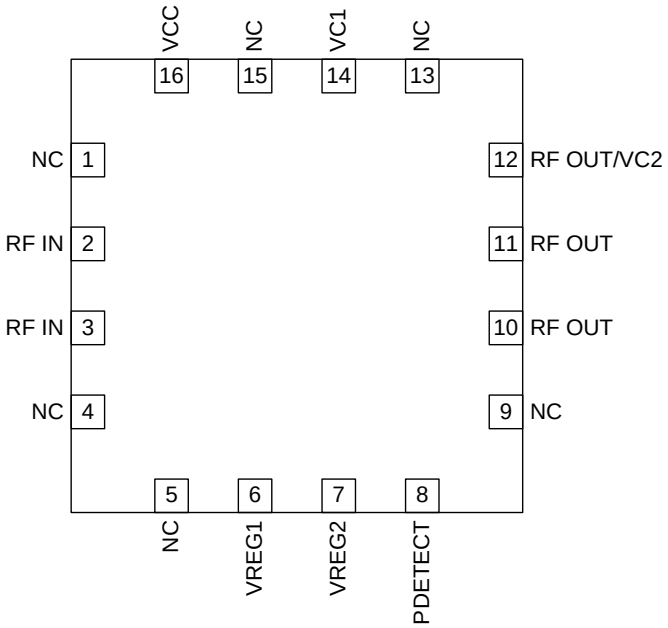
Pin	Function	Description	Interface Schematic
1	NC	Not connected. May be connected to ground (GND).	
2	RF IN	RF input. See evaluation board schematic for details.	
3	RF IN	RF input. See evaluation board schematic for details.	See pin 2.
4	NC	Not connected. May be connected to ground (GND).	
5	NC	Do not connect. **Note:** VCC voltage may be applied to this pin without damage to, or affecting the performance of, the RF5125.	
6	VREG1	Bias current control voltage for the first stage.	
7	VREG2	Bias current control voltage for the second stage. The VREG2 pin may be connected to VREG1 through an external resistor bridge.	
8	PDETECT (or N/C*)	Provides an output voltage proportional to the output RF level. *In applications where the PDETECT function is not desired, this pin may be left unconnected.	
9	NC	No-connect.	
10	RF OUT	RF output.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT/ VC2	Power supply for second stage amplifier. Connect as shown on evaluation board schematic.	
13	NC	Not connected. May be connected to ground (GND).	
14	VC1	Power supply for first stage amplifier. Connect as shown on evaluation board schematic.	
15	NC	Not connected. May be connected to ground (GND).	
16	VCC	Supply voltage for the bias reference and control circuits. May be connected with VC1 and VC2 (single-supply voltage).	
Pkg Base	GND	The center metal base of the QFN package provides DC and RF ground as well as heat sink for the amplifier.	

Package Drawing



Pin Out



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Theory of Operation and Application Information

The RF5125 is a two-stage (2-stage) power amplifier (PA) with a minimum gain of 26dB (29dB typical) in the 2.4GHz to 2.5GHz Industrial, Scientific, and Medical (ISM) band. The RF5125 has a 50Ω internal input and interstage match. Only the RF5125 output stage requires matching. The RF5125 is designed primarily for IEEE802.11g/n wireless local area network (WLAN) applications where the available supply voltage and current are limited. This amplifier will operate to and below the lowest expected voltage made available by a typical PC Card (PCMCIA or CardBus) slot in a laptop personal computer (PC). The RF5125 maintains required linearity at decreased supply voltages.

The RF5125 operates from a single supply voltage of $3.0V_{DC}$ to $5.0V_{DC}$ to deliver specified performance. Power control is provided through two (2) bias control input pins (V_{REG1} and V_{REG2}). For the best performance and lower current, there is a 68Ω resistor placed as R2. In most applications these two (2) bias control input pins are connected together (before R1 and R2) and employed as a single control input.

There is no required matching on the RF5125 input or interstage circuits. Only the RF5125 output stage requires matching allowing the RF5125 to be implemented in applications requiring the fewest end product bill of materials (BOM) parts count and lowest BOM cost. In most cases the capacitor used as part of the RF5125 output matching circuit is also employed to accomplish DC-blocking. The RF5125PCBA evaluation board (available from RF Micro Devices, Inc. (RFMD)) is optimized for $3.3V_{DC}$ supply input.

For best results, the RF5125PCBA evaluation board circuit layout should be copied as closely as possible. In particular, the RF5125PCBA evaluation board ground layout, ground vias, and output matching components and location should be copied without deviation. Other PCB layout configurations may provide acceptable RF5125 performance; however, the end product design process will be faster and manufacturing first time yield (FTY) better if the RF5125PCBA evaluation board design is followed. RFMD provides RF5125PCBA design and Gerber files upon request.

Though not difficult to implement to achieve state-of the-art performance, the RF5125 is employed at frequencies greater than 2GHz, where care in circuit layout and component selection is advisable. Of primary concern with RF5125 PCB layout is the selection and placement of output matching components (RF5125PCBA bill of materials (BOM) is available upon request). High-Q (quality factor) capacitors and inductors are not required in every RF5125 based design; however, it is highly recommended that the RF5125PCBA evaluation board BOM be followed exactly for all initial end product designs. Upon initial baseline of RF5125 based PCB performance, less costly (Lower-Q) output matching circuit components may be substituted and evaluated against the initial design performance. RFMD experience indicates that end product FTY improvements more than offset the cost difference between “High-Q” and “Low-Q” components.

The output matching capacitor is C10 (or C11) which is connected between the RF5125 and the connector J2 (RFOUT) as shown on the *RF5125PCBA Evaluation Board Schematic*. This capacitor is selected in value and positioned with reference to the 50Ω transmission line. This matching capacitor is a single 2.2pF shunt capacitor whose placement depends on the supply voltage applied. With the nominal $3.0V_{DC}$ to $3.6V_{DC}$ supply voltage, the distance of the transmission line should be 115mils (this is marked as the placement for C10). For a supply voltage of 5V, the length of the transmission line should be 101mils (which is marked as the placement for C11). Notice, only one of the shunt output capacitors is placed at one time (C10 or C11). The transmission line length and thickness should be duplicated as closely as possible in any customer PCB layout. Due to PCB material variation (e.g., FR4) and PCB manufacturing variations, the customer may benefit from small adjustments made to the length of the transmission line when the RF5125PCBA evaluation board is duplicated to produce an end product PCB design. The initial PCB layout should include exposed ground area near C10 or C11 to allow ease of RF5125 output circuit optimization; Smith Chart-based design tools may be used to assist in determining the desired capacitor value and transmission line physical characteristics. Note that the use of a single capacitor output circuit match results in a more sensitive match and slightly reduced RF5125 bandwidth. In this configuration, the RF5125 will exhibit sufficient output spectrum bandwidth to meet IEEE802.11b/g requirements when matched properly.

The RF5125 had been primarily characterized with a V_{REG} voltage of 2.8V_{DC}. However, the RF5125 will operate from a wide range of bias control voltages and within a wide range of frequencies (typically 1800MHz to 2800MHz). If a bias control voltage other than 2.8V_{DC} is preferred or if a different frequency range (other than 2.4GHz to 2.5GHz) is desired, please contact RFMD Sales or Applications Engineering for assistance.

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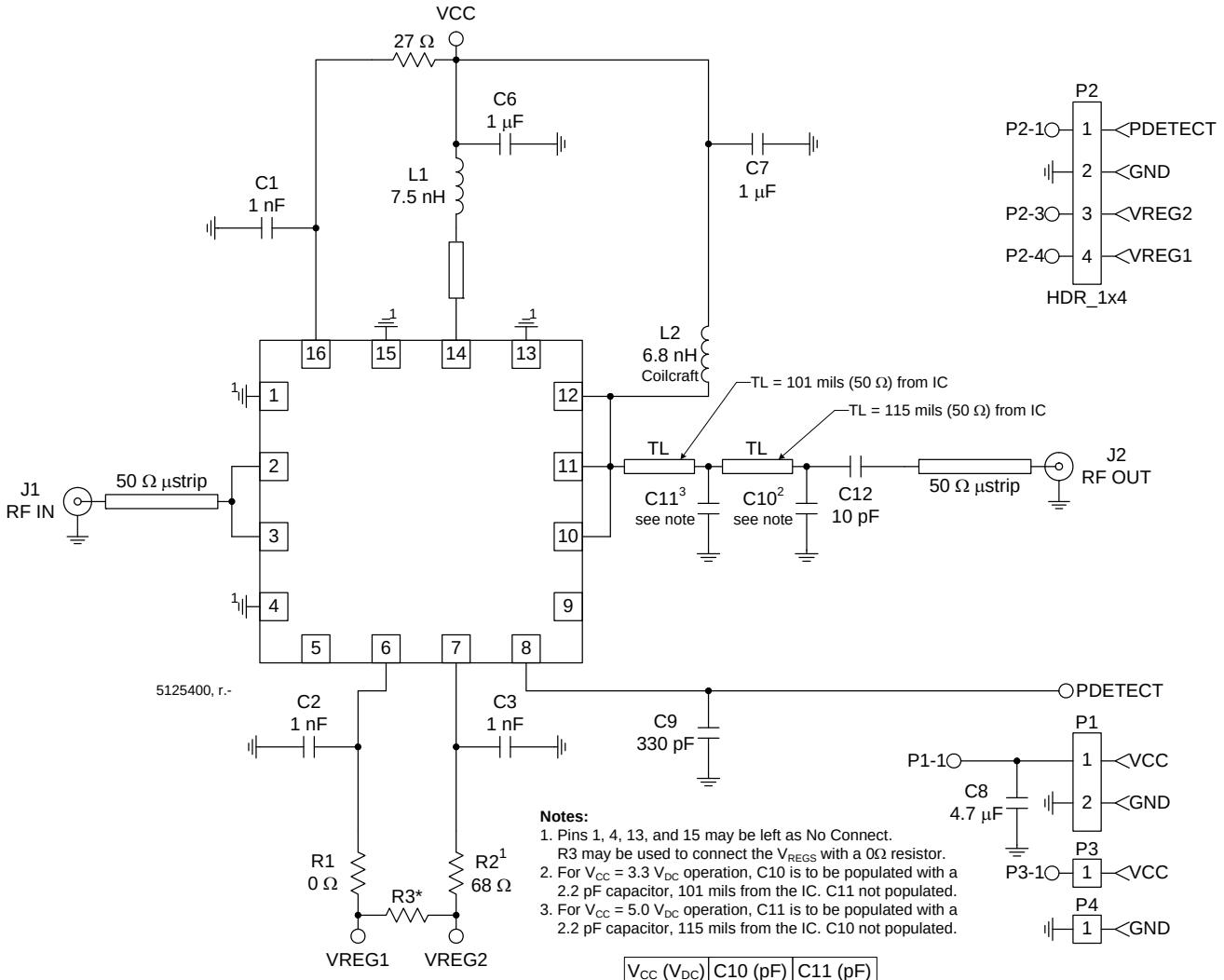
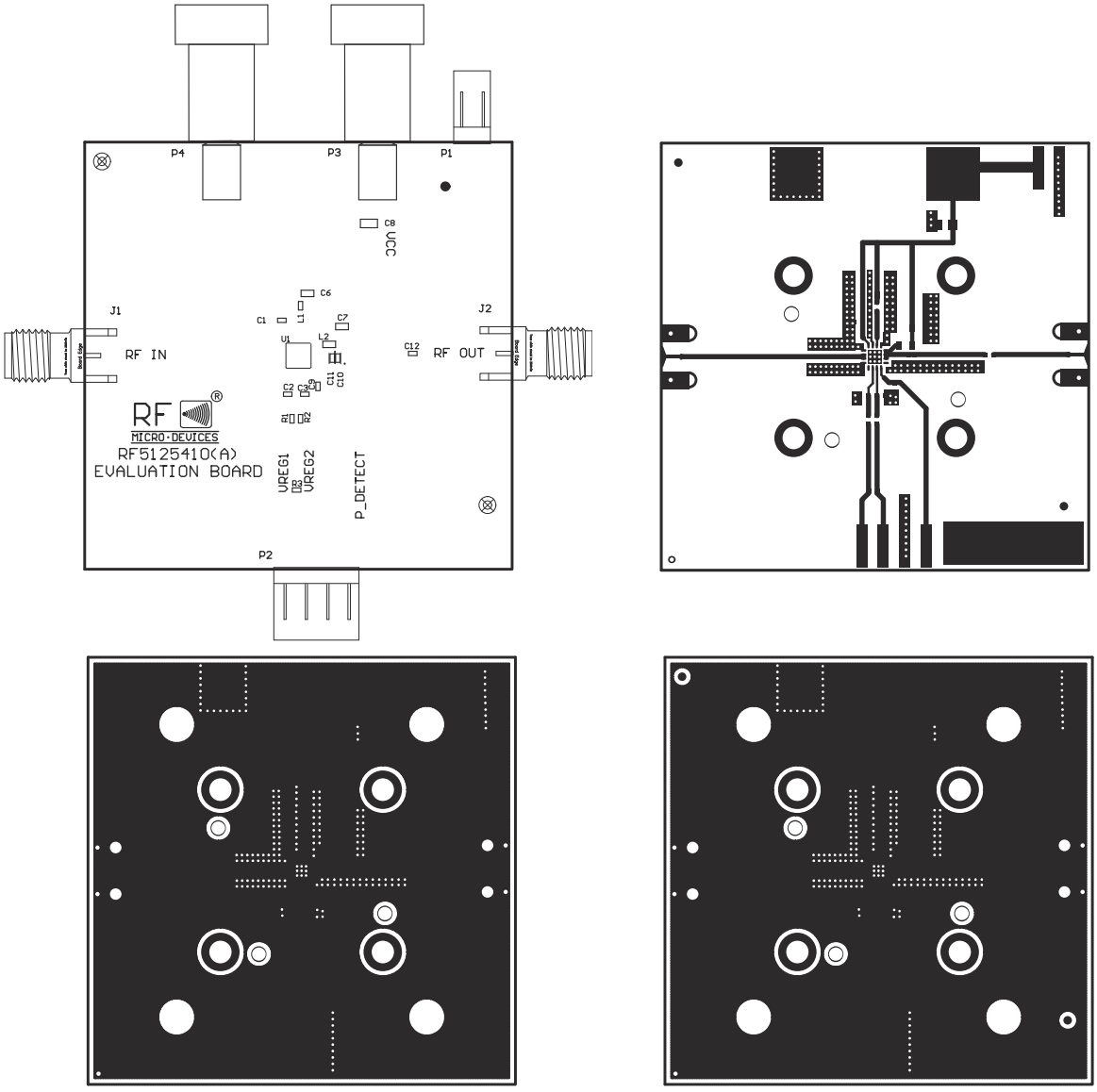
Evaluation Board Schematic



Notes:
1. Pins 1, 4, 13, and 15 may be left as No Connect. R3 may be used to connect the V_{REGS} with a 0Ω resistor.
2. For V_{CC} = 3.3 V_{DC} operation, C10 is to be populated with a 2.2 pF capacitor, 101 mils from the IC. C11 not populated.
3. For V_{CC} = 5.0 V_{DC} operation, C11 is to be populated with a 2.2 pF capacitor, 115 mils from the IC. C10 not populated.

V_{CC} (V_{DC})	C10 (pF)	C11 (pF)
3.3	2.2	DNP
5.0	DNP	2.2

Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.031”, Board Material FR-4, Multi-Layer



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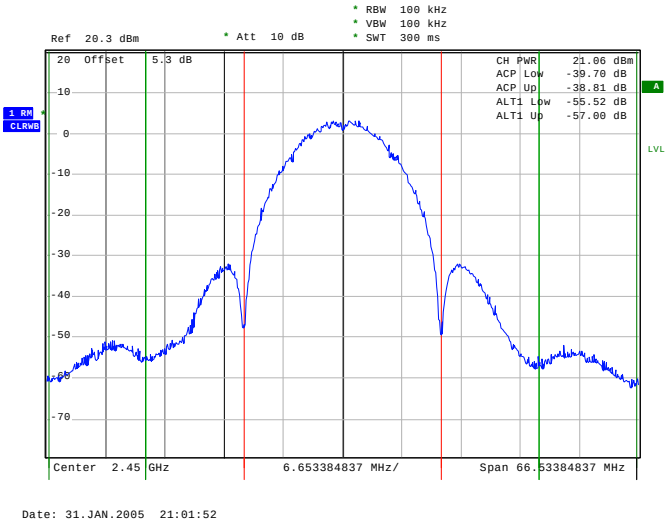
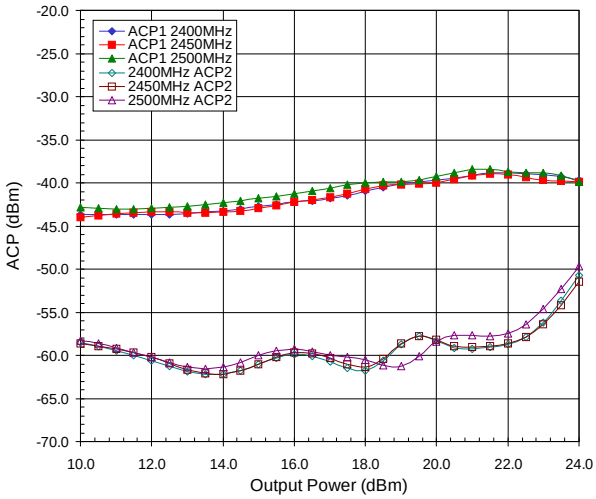
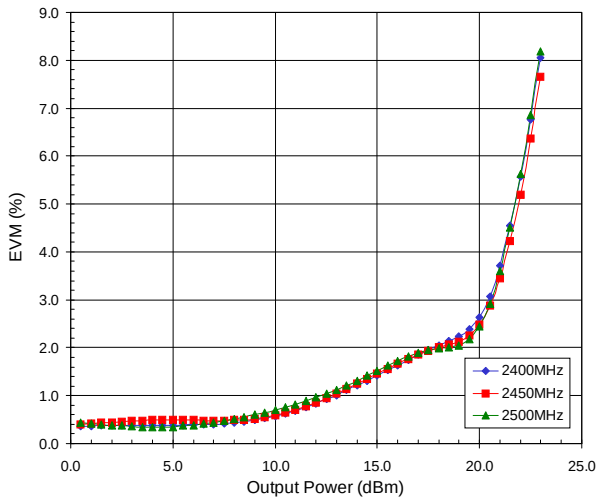
RF Power Spectrum @ +21 dBm 11 Mbps CCK Modulation
(V_{CC} = +3.3 V_{DC}; V_{REG} = +2.8 V_{DC}; Frequency = 2.45 GHz)



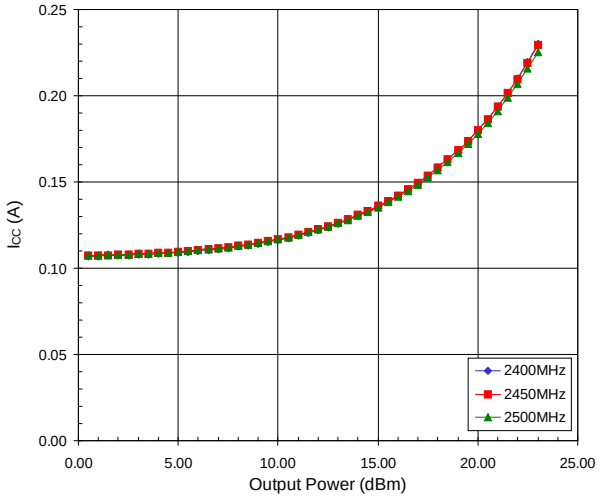
ACP versus P_{OUT}



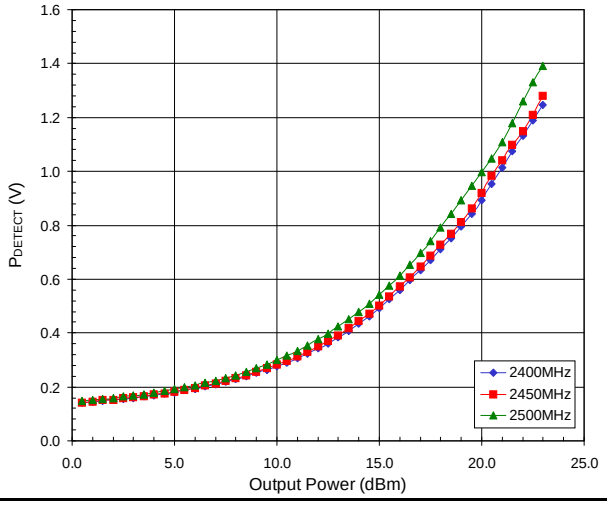
EVM versus P_{OUT}



Operating Current versus P_{OUT}



P_{DETECT} versus P_{OUT}



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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

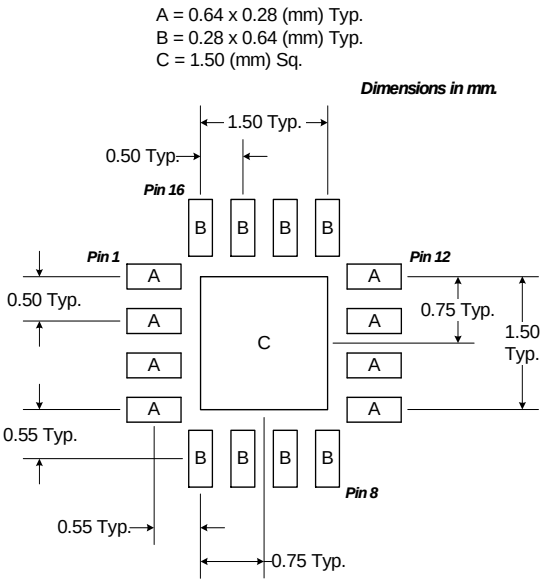

Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

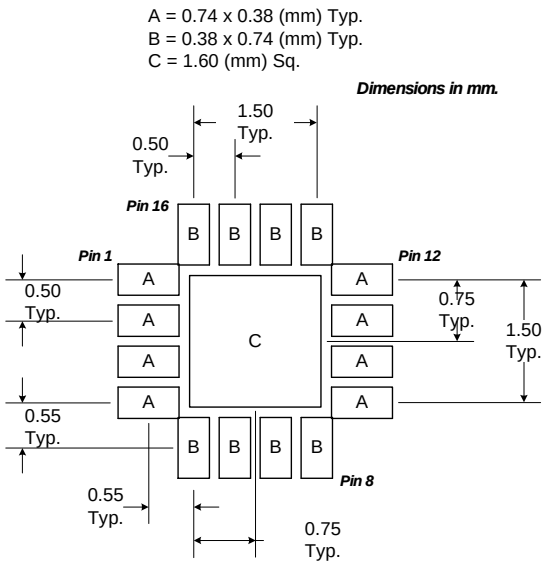

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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