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# **RF5188** 3V 1950 MHZ W-CDMA LINEAR POWER AMPLIFIER MODULE

RoHS Compliant & Pb-Free Product Package Style: QFN, 16-Pin, 3 x 3

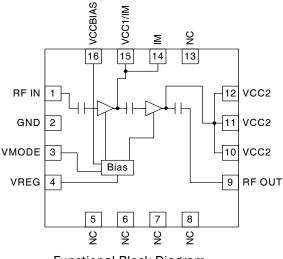


### **Features**

- Input/Output Internally Matched@50Ω
- 27.5dBm Linear Output Power
- 42% Peak Linear Efficiency
- 28dB Linear Gain
- -42dBc ACLR @ ±5MHz
- HSDPA Capable

### **Applications**

- 3V W-CDMA Band 1 Handsets
- Multi-Mode W-CDMA 3G Handsets
- 3V TD-SCDMA Handsets
- Spread-Spectrum Systems



Functional Block Diagram

### **Product Description**

The RF5188 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V W-CDMA handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1920MHz to 1980MHz band (Band 1). The RF5188 has a digital control line for low power applications to lower quiescent current. The RF5188 is assembled in at 16-pin, 3mmx3mm, QFN package.

### **Ordering Information**

RF5188 RF5188PCBA-41X

3V 1950MHz W-CDMA Linear Power Amplifier Module Fully Assembled Evaluation Board

### **Optimum Technology Matching® Applied**

🗹 GaAs HBT	□ SiGe BiCMOS	GaAs pHEMT	🗌 GaN HEMT
GaAs MESFET	Si BiCMOS	Si CMOS	
InGaP HBT	SiGe HBT	🗌 Si BJT	

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# **RF5188**



### **Absolute Maximum Ratings**

-		
Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ( $P_{OUT} \leq 31 dBm$ )	+5.2	V
Control Voltage (V <sub>REG</sub> )	+3.9	V
Input RF Power	+10	dBm
Mode Voltage (V <sub>MODE</sub> )	+3.9	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity Level (IPC/JEDEC J-STD-20)	MSL 2 @ 260	°C



Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical perfor-mance or functional operation of the device under Absolute Maximum Rating condi-tions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Devenedar	Specification		11.4.14	Condition		
Parameter	Min.	Тур.	Max.	Unit	Condition	
High Gain Mode (V <sub>MODE</sub> Low)					$\begin{array}{l} T=25^{\circ}C \text{ Ambient, } V_{CCBIAS}=3.4V, \\ V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, \text{ and} \\ P_{OUT}=27.5dBm \text{ for all parameters (unless otherwise specified). Modulation is 3GPP 3.2 03-00 DPCCH+1DPDCH.} \end{array}$	
Operating Frequency Range	1920		1980	MHz		
Linear Gain	26	28.5	32	dB		
Harmonics			-10	dBm	f=2fo, 3fo	
Maximum Linear Output	27.5			dBm		
Linear Efficiency	38	42	47	%		
Maximum I <sub>CC</sub>	352	394	435	mA		
ACLR1@±5MHz		-42	-37	dBc		
ACLR2 @ ±10MHz		-53	-48	dBc		
Input VSWR		1.7:1				
Output VSWR Stability Ruggedness			6:1		No oscillation>-70dBc	
			10:1		No damage	
Noise Power		-150		dBm/Hz	-50≤P <sub>OUT</sub> ≤+27.5dBm, RX=925MHz to 960MHz (EGSM)	
		-133		dBm/Hz	-50≤P <sub>OUT</sub> ≤+27.5dBm, RX=1805MHz to 1880MHz (DCS)	
		-140		dBm/Hz	-50≤P <sub>OUT</sub> ≤+27.5dBm, RX=2110MHz to 2170MHz (W-CDMA), TX / RX Offset=130MHz	
		-143		dBm/Hz	-50≤P <sub>OUT</sub> ≤+27.5dBm, RX=2110MHz to 2170MHz (W-CDMA), TX / RX Offset=190MHz	
		-147		dBm/Hz	-50≤P <sub>0UT</sub> ≤+27.5dBm, RX=2400MHz to 2480MHz (Bluetooth)	
		-107		dBm/Hz	-50≤P <sub>OUT</sub> ≤+27.5dBm, TX=1932.3MHz to 1980MHz, RX=1893.5MHz to 1919.6MHz (PHS)	
IM Products						
IM 5MHz			-31	dBc	IF offset f <sub>0</sub> +5MHz with CW signal=-40dBc	
IM 10MHz			-41	dBc	IF offset $f_0$ +10MHz with CW signal=-40dBc	

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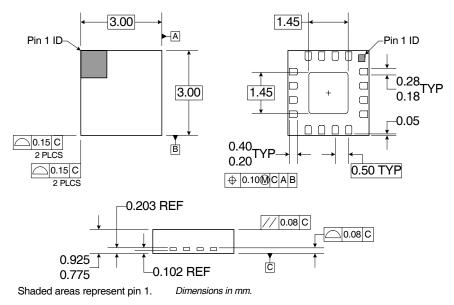
Min.         Typ.         Max.         Max.           Low Gain Mode (V <sub>MODE</sub> High) $V_{CP}$ <	Devenueter	Specification			11	Oened!#iene	
Low Gain Mode (V <sub>MODE</sub> High)         wasse         wasse         wasse         wasse         wasse         wasse         wasse         wasse         wasse         Poor = 1.68 m for Moor         Poor = 1.6	Parameter	Min.	Тур.	Max.	Unit	Condition	
Linear Gain         22         26         31         dB           Maximum Linear Output         16         dBm         dBm           Linear Efficiency         18.3         21.0         25.3         %           ACIR $@$ ±5MHz         41         -37         dBc           ACIR $@$ ±5MHz         -54         48         dBc           ACIR $@$ ±5MHz         105         125         145         mA           Input VSWR         105         125         145         mA           Input VSWR Stability Ruggedness         6:1         No oscillation >-65dBc           IM Products         -         10:1         No damage           IM SDMHz         -         -31         dBc         IF offset $f_0 + 5MHz$ with CW signal=-40dBc           Power Supply         -         -31         dBc         IF offset $f_0 + 5MHz$ with CW signal=-40dBc           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         Low power with DC to DC converter           V <sub>CC</sub> Bias         1.5         -         4.2         V         Low power with DC to DC converter           V <sub>CC Dias</sub> 1.5         -         4.2         V         Low power with DC to DC converter	Low Gain Mode (V <sub>MODE</sub> High)					$V_{CC}$ =1.5V, $V_{REG}$ =2.8V, $V_{MODE}$ =2.8V, and $P_{OUT}$ =16dBm for all parameters (unless otherwise specified). Modulation is 3GPP 3.2 03-00	
Maximum linear Output         16         16         dBm           Linear Efficiency         18.3         21.0         25.3         %           ACLR $\oplus$ 100MHz         -41         -37         dBc         ACLR $\oplus$ 100MHz         -54         48         dBc           Maximum loc         105         125         145         mA         Input VSWR         -         105         125         145         mA           Input VSWR         2:1         -	Operating Frequency Range	1920		1980	MHz		
Linear Efficiency         18.3         21.0         25.3         %         ACLR $@$ ±50Mz           ACLR $@$ ±50Mz         -41         -37         dBc           ACLR $@$ ±10MHz         -54         48         dBc           Maximum $l_{CC}$ 105         125         145         mA           Input SWR         105         125         145         mA           Output VSWR Stability Ruggedness         105         125         145         No oscillation>-65dBc           Mutput SWR         -         10:1         No damage         No damage           IM Products         -         10:1         No damage         Image           IM 10MHz         -         -         10:1         No damage           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         V           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         Low power with DC to DC Converter           V <sub>CC</sub> Bias         1.5         -         -         V         Low power with DC to DC Converter           V <sub>GC Bias</sub> Infle Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBMS</sub> )         -         60         83         mA         V <sub>MODE</sub> =Iow and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =3.8V, V <sub>CC</sub> =1.5V	Linear Gain	22	26	31	dB		
ACLR @ $\pm 5MHz$ Image         Image         Image         Image           ACLR @ $\pm 10MHz$ 105         125         145         mA         Image           Input VSWR         105         125         145         mA         Image           Input VSWR         105         125         145         mA         Image           Output VSWR Stability Ruggedness         105         2:1         Image         Image         Image           IM Products         Image         10:1         No oscillation>-85dBc         No damage           IM Products         Image         Image         Image         Image         Image           IM 10MHz         Image         Image         Image         Image         Image           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         Image           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         Image           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         Image           Supply Collage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V         Image           Voc Bias         1.5	Maximum Linear Output	16			dBm		
ACLR @ ±10MHz         Image	Linear Efficiency	18.3	21.0	25.3	%		
Maximum $I_{CC}$ 105         125         145         mA         Input VSWR           Input VSWR Stability Ruggedness         1         2:1         Input VSWR Stability Ruggedness         No oscillation>-65 dBc           Output VSWR Stability Ruggedness         1         10:1         No damage           IM Products         1         1         No damage           IM Products         1         1         No damage           IM 10MHz         1         0         No damage           Power Supply         1         3         dBc         IF offset $f_0 + 10$ MLz with CW signal = .40 dBc           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V           Supply Constance         1.5         4.2         V         Low power with DC to DC Converter           V <sub>CC</sub> Bias         1.5         4.2         V         Low gain Idle Current           (Ig_C1/I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         70         93         mAA         V <sub>MODE</sub> =low and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =3.4V           V <sub>MOEC</sub> Curent         1         3	ACLR @ ±5 MHz		-41	-37	dBc		
Input VSWRImageImageImageImageOutput VSWR Stability RuggednessImage $6:1$ No oscillation>-65dBcOutput VSWR Stability RuggednessImageNo damageIM ProductsImageImageNo damageIM ProductsImageImageImageIM 10MHzImageImageImageIM 10MHzImageImageImageSupply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )3.23.44.2VSupply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )3.23.44.2VU <sub>CC</sub> Bias1.54.2VImageU <sub>CC</sub> Bias1.54.2VImageU <sub>CC</sub> Vicc2/ (CcsIAS)1.53.0MAV <sub>MODE</sub> =Iow and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =3.4VU <sub>CC</sub> Vicc2/ (CcsIAS)Image1.33.0MAV <sub>MODE</sub> Urrent1.33.0MAImageU <sub>CC</sub> Vicc2/ (CcsIAS)Image2.5ImageImageDC Turn On/Off Time1.26 <td>ACLR @ ±10MHz</td> <td></td> <td>-54</td> <td>-48</td> <td>dBc</td> <td></td>	ACLR @ ±10MHz		-54	-48	dBc		
Output VSWR Stability RuggednessImageImageImageNo obscillation >-65 dBcIM ProductsImageImageIM PoductsImageImageIM SMHzImageImageIM 10MHzImageImageIM 10MHzImage <t< td=""><td>Maximum I<sub>CC</sub></td><td>105</td><td>125</td><td>145</td><td>mA</td><td></td></t<>	Maximum I <sub>CC</sub>	105	125	145	mA		
RuggednessIndIndIndIndNo damageIMIM10:1No damageIM ProductsIMIMIMIMIMIMIM 5MHzIMIMIMIB offset $f_0$ +5MHz with CW signal=-40 dBcIM 10MHzIMIMIMIF offset $f_0$ +10MHz with CW signal=-40 dBcPower SupplyIMIMIMIFSupply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )3.23.44.2VSupply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )3.23.44.2VIm Gain Idle Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBAS</sub> )Im7093mAV <sub>MCDE</sub> =low and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =3.4VImV <sub>MODE</sub> =low and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =1.5VV <sub>RCG</sub> Gurrent (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBAS</sub> )Im3mAV <sub>MODE</sub> =high and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =1.5VImImV <sub>MODE</sub> Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBAS</sub> )Im3mAV <sub>MODE</sub> =high and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =1.5VImImV <sub>MCDE</sub> Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBAS</sub> )ImImImV <sub>MCDE</sub> Current (I <sub>CC1</sub> /I <sub>CCC</sub> /I <sub>CCBAS</sub> ) <td>Input VSWR</td> <td></td> <td>2:1</td> <td></td> <td></td> <td></td>	Input VSWR		2:1				
IM Products         Image: marked state				6:1		No oscillation >-65 dBc	
IM 5 MHz         Image: marked state st				10:1		No damage	
IM 10 MHz         -41         dBc         IF offset $f_0 + 10 MHz$ with CW signal = 40 dBc           Power Supply         3.2         3.4         4.2         V           Supply Voltage (V <sub>CC1</sub> and V <sub>CC2</sub> )         3.2         3.4         4.2         V           Come         0.6         V         Low power with DC to DC Converter           V <sub>CC</sub> Bias         1.5         4.2         V         Low power with DC to DC Converter           High Gain Idle Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         1.5         4.2         V         Low power with DC to DC Converter           Low Gain Idle Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         1.5         4.2         V         Low Gain MA           V <sub>MGDE</sub> Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         60         83         mA         V <sub>MODE</sub> =low and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =3.4V           V <sub>MGDE</sub> Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         1         3         mA         V <sub>MODE</sub> =low and V <sub>REG</sub> =2.8V, V <sub>CC</sub> =1.5V           V <sub>REG</sub> Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         1         3         mA         Supple         Supple           V <sub>MODE</sub> Current (I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )         1         3         mA         Supple         Supple           V <sub>REG</sub> Current         1         2         6         uS         Suple         Supple         Suple	IM Products						
Power Supply         Image: Constraint of the sector o	IM 5MHz			-31	dBc	IF offset $f_0$ +5MHz with CW signal=-40dBc	
Supply Voltage ( $V_{CC1}$ and $V_{CC2}$ )         3.2         3.4         4.2         V         Low power with DC to DC Converter $V_{CC}$ Bias         1.5         4.2         V         Low power with DC to DC Converter           High Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CBIAS}$ )         1.5         4.2         V            Low Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CBIAS}$ )         70         93         mA $V_{MODE}$ =low and $V_{REG}$ =2.8V, $V_{CC}$ =3.4V           Low Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CCBIAS}$ )         60         83         mA $V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5V           VREG Current         1         3         mA         V_{MODE}=high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5V           VREG Current         1         3         mA         V_{MODE}=high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5V           VREG Current         1         3         mA         V_{MODE}         Image: Comparison of the comparison	IM 10MHz			-41	dBc	IF offset f <sub>0</sub> +10MHz with CW signal=-40dBc	
ImportanceImage (Cold and Cold)Image (Cold and Cold)Image (Cold and Cold)Voc Bias0.6VLow power with DC to DC ConverterVoc Bias1.54.2VHigh Gain Idle Current ( $l_{CC1}/l_{C2}/l_{CGBIAS}$ )7093mA $V_{MODE}$ =low and $V_{REG}$ =2.8V, $V_{CC}$ =3.4VLow Gain Idle Current ( $l_{CC1}/l_{C2}/l_{CGBIAS}$ )6083mA $V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5VVREG Current13mAVMODEVMODE Current250uA1Prime1.26uSDC Turn On/Off Time225uSTotal Current (Power Down)0.20.5vAVREG Low Voltage (Power Down)00.5VVREG High Voltage (Recommended)2.752.82.95VREG High Voltage (Operational)2.73.0VVMODE Voltage00.5VHigh Gain Mode	Power Supply						
V <sub>CC</sub> Bias1.54.2VHigh Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CCBIAS}$ )7093mA $V_{MODE}$ =low and $V_{REG}$ =2.8V, $V_{CC}$ =3.4VLow Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CCBIAS}$ )6083mA $V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5VLow Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CCBIAS}$ )13mA $V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5VVREG Current13mAV_{MODE}VMODE Current120uAPR Turn On/Off Time126uSDC Turn On/Off Time225uS1Total Current (Power Down)0.20.5uA1V <sub>REG</sub> Low Voltage (Power Down)00.5V1V <sub>REG</sub> High Voltage (Operational)2.72.82.95VV <sub>MODE</sub> Voltage00.5VHigh Gain Mode	Supply Voltage ( $V_{CC1}$ and $V_{CC2}$ )	3.2	3.4	4.2	V		
High Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CCBIAS}$ )To93mA $V_{MODE}$ =low and $V_{REG}$ =2.8V, $V_{CC}$ =3.4VLow Gain Idle Current ( $I_{CC1}/I_{CC2}/I_{CCBIAS}$ )6083mA $V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5V $V_{REG}$ Current13mA $V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5V $V_{MODE}$ Current13mA $V_{MODE}$ $V_{MODE}$ Current13mA $V_{MODE}$ $V_{MODE}$ Current126uSDC Turn On/Off Time126uSDC Turn On/Off Time00.5uAV_{REG} Low Voltage (Power Down)00.5V $V_{REG}$ High Voltage (Recom- mended)2.752.82.95V $V_{REG}$ High Voltage (Operational)2.73.0V $V_{MODE}$ Voltage00.5VHigh Gain Mode		0.6			V	Low power with DC to DC Converter	
$(I_{CC1}/I_{CC2}/I_{CCBIAS})$ Image: formed and the second s	V <sub>CC</sub> Bias	1.5		4.2	V		
(I <sub>CC1</sub> /I <sub>CC2</sub> /I <sub>CCBIAS</sub> )IIIIIIV <sub>REG</sub> CurrentI13mAIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	-		70	93	mA	$V_{MODE}$ = low and $V_{REG}$ = 2.8 V, $V_{CC}$ = 3.4 V	
$V_{MODE}$ Current         Image: Current         250         uA         uA           RF Turn On/Off Time         1.2         6         uS            DC Turn On/Off Time         2         25         uS            Total Current (Power Down)         0         0.5         uA            V <sub>REG</sub> Low Voltage (Power Down)         0         0.5         V            V <sub>REG</sub> High Voltage (Recommended)         2.75         2.88         2.95         V            V <sub>REG</sub> High Voltage (Operational)         2.7         3.0         V             V <sub>MODE</sub> Voltage         0         0.5         V         High Gain Mode			60	83	mA	$V_{MODE}$ =high and $V_{REG}$ =2.8V, $V_{CC}$ =1.5V	
RF Turn On/Off Time1.26 $uS$ DC Turn On/Off Time225 $uS$ DC Turn On/Off Time00.20.5 $uA$ Total Current (Power Down)00.5 $uA$ $V_{REG}$ Low Voltage (Power Down)00.5 $V$ $V_{REG}$ High Voltage (Recommended)2.752.82.95 $V$ $V_{REG}$ High Voltage (Operational)2.73.0 $V$ $V_{MODE}$ Voltage00.5 $V$ High Gain Mode	V <sub>REG</sub> Current		1	3	mA		
DC Turn On/Off Time $2$ $25$ $uS$ Total Current (Power Down) $0.2$ $0.5$ $uA$ $V_{REG}$ Low Voltage (Power Down) $0$ $0.5$ $V$ $V_{REG}$ High Voltage (Recommended) $2.75$ $2.8$ $2.95$ $V$ $V_{REG}$ High Voltage (Operational) $2.7$ $3.0$ $V$ $V_{NODE}$ Voltage $0$ $0.5$ $V$	V <sub>MODE</sub> Current		250		uA		
Total Current (Power Down)00.5uAVREG Low Voltage (Power Down)00.5VVREG High Voltage (Recommended)2.752.882.95VVREG High Voltage (Operational)2.73.0VVMODE Voltage00.5VHigh Gain Mode	RF Turn On/Off Time		1.2	6	uS		
VREG Low Voltage (Power Down)00.5VVREG High Voltage (Recommended)2.752.82.95VVREG High Voltage (Operational)2.73.0VVNODE Voltage00.5VHigh Gain Mode	DC Turn On/Off Time		2	25	uS		
VREG High Voltage (Recommended)2.752.82.95VVREG High Voltage (Operational)2.73.0VVMODE Voltage00.5VHigh Gain Mode	Total Current (Power Down)		0.2	0.5	uA		
mended)         Image: Constraint of the system         Image: Constand of the system	V <sub>REG</sub> Low Voltage (Power Down)	0		0.5	V		
V <sub>MODE</sub> Voltage         O         O.5         V         High Gain Mode		2.75	2.8	2.95	V		
	V <sub>REG</sub> High Voltage (Operational)	2.7		3.0	V		
	V <sub>MODE</sub> Voltage	0		0.5	V	High Gain Mode	
	V <sub>MODE</sub> Voltage	2.0		3.0	V	Low Gain Mode	

# RF5188

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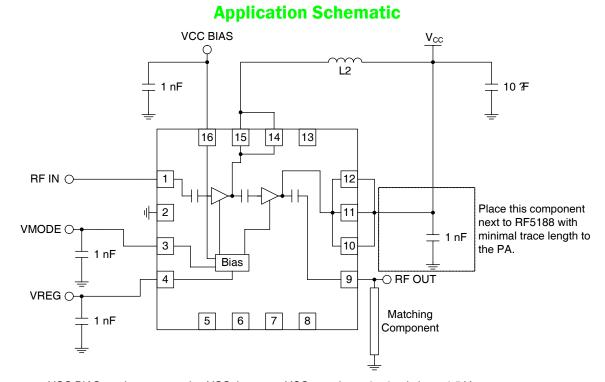
Pin	Function	Description	Interface Schematic
1	RF IN	RF input internally matched to $50\Omega$ . This input is internally AC-coupled.	
2	GND	Ground connection.	
3	VMODE	For nominal operation (High Power mode), V <sub>MODE</sub> is set LOW. When set HIGH, devices are biased lower to improve efficiency at lower output levels.	
4	VREG	Regulated voltage supply for amplifier bias circuit. In power down mode, both $V_{\text{REG}}$ and $V_{\text{MODE}}$ need to be LOW (<0.5V).	
5	NC	No connection. Do not connect this pin to any external circuit.	
6	NC	No connection. Do not connect this pin to any external circuit.	
7	NC	No connection. Do not connect this pin to any external circuit.	
8	NC	No connection. Do not connect this pin to any external circuit.	
9	RF OUT	RF output. Internally AC-coupled.	
10	VCC2	Output stage collector supply. Please see the schematic for required exter- nal components.	
11	VCC2	Same as pin 10.	
12	VCC2	Same as pin 10.	
13	NC	No connection. Do not connect this pin to any external circuit.	
14	IM	Interstage matching. Connect to pin 15.	
15	VCC1/IM	First stage collector supply and interstage matching. A $4.7\mu\text{F}$ decoupling capacitor may be required. Connect to pin 14.	
16	VCCBIAS	Power supply input for the DC bias circuitry.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

# **Package Drawing**









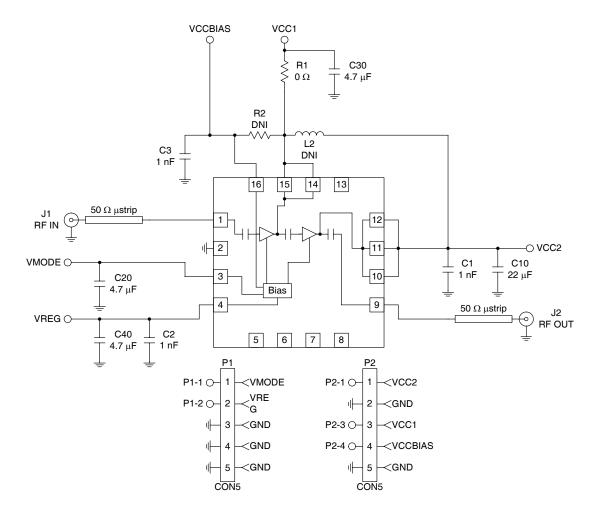
VCC BIAS can be connected to VCC; however, VCC must be maintained above 1.5 V. L2 = 8.2 nH and may be needed to provide isolation between VCC1 and VCC2 depending on layout.

Circuit Optimization for various Output Power Requirements						
Output Power	(dBm)	Matching Component	Sample Part Number	Typical Efficiency (%)		
28		12nH	LQG15HN12NJ02D (Murata)	41		
27.5		N/A		42		
26.5		0.5 pF	GRM1555C1HR50BZ01E (Murata)	42		
26		1.0pF	GRM1555C1H1R0BZ01E (Murata)	42		
25		1.5pF	GRM1555C1H1R5BZ01E (Murata)	41		

### **Circuit Optimization for Various Output Power Requirements**



## **Evaluation Board Schematic**





## **PCB Design Requirements**

#### **PCB Surface Finish**

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

#### **PCB Land Pattern Recommendation**

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

### **PCB Metal Land Pattern**



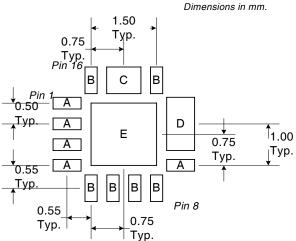


Figure 1. PCB Metal Land Pattern (Top View)





### **PCB Solder Mask Pattern**

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

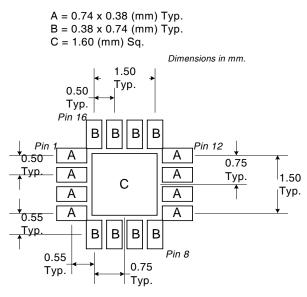


Figure 2. PCB Solder Mask Pattern (Top View)

#### Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.