RFMD

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RF6001

FRACTIONAL-N RF SYNTHESIZER WITH MODULATOR AND DIGITAL IF FILTER

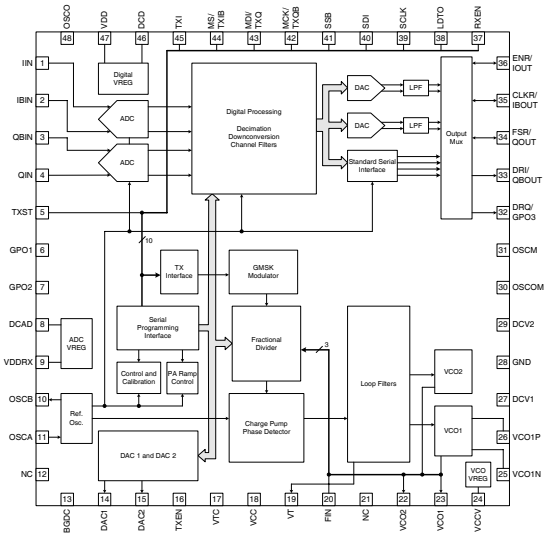
Part of the POLARIS™ TOTAL RADIO™ Solution
RoHS Compliant & Pb-Free Product
Package Style: QFN, 48-Pin, 7 x 7

Features

- Fractional-N Synthesizer with Digital GMSK Modulator
- Signal Processing Circuitry for use with RF2722 VLIF Receiver
- Versatile Baseband Interface
- Integrated RF Transmit VCO's

Applications

- GSM/DCS Handsets
- GSM/DCS/PCS Handsets
- Quad-Band GSM Handsets
- Multi-Band $EDGE_{RX}$ Handsets
- Multi-Band GPRS Handsets



Functional Block Diagram

Product Description

The RF6001 is a combination synthesizer and signal processing IC, which along with the RF2722 Very-Low-IF Receive IC, constitutes RFMD's low-cost GSM transceiver solution. The high-performance fractional-N synthesizer offers numerous features including a fully digital GMSK modulator with provisions for an analog I/Q interface and extremely low current consumption. The signal processor section provides a digital receive filter path designed to complement the RF2722. The IF inputs are digitized, filtered and downconverted to baseband I and Q signals. The flexible baseband interface can be configured for either analog or digital operation. Chip functionality is controlled through a three-wire serial data interface (SDI) bus. The RF2722 is part of the POLARIS™ TOTAL RADIO™ solution.

Ordering Information

RF6001	Fractional-N RF Synthesizer with Modulator and Digital IF Filter

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Storage Temperature	-40 to +150	°C
Input Voltage, IIN, IBIN, QIN, QBIN	2.7	V
Input Voltage, all others	3.6	V
Supply Voltage, V_{CC}	-0.5 to 5.0	V
Supply Voltage, V_{DD}, V_{RXVDD}, V_{CCV}	-0.5 to 3.6	V

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Range					All specifications met over listed operating range, unless otherwise specified.
Supply Voltage (V_{RXVDD}, V_{DD}, V_{CCV}, V_{CC})	2.7	2.75	3.0	V	
Temperature (T_{OP})	-40	+25	+85	°C	
Frequency Range					
Receive					
Cellular 850	869		894	MHz	Low Band Receive
EGSM900	925		960	MHz	Low Band Receive
DCS1800	1805		1880	MHz	High Band Receive
PCS1900	1930		1990	MHz	High Band Receive
Transmit					
Cellular 850	824		849	MHz	Low Band Transmit
EGSM900	880		915	MHz	Low Band Transmit
DCS1800	1710		1785	MHz	High Band Transmit
PCS1900	1850		1910	MHz	High Band Transmit
Power Supply					
Supply Current RX I_{RXD}			30	mA	Digital interface
Supply Current RX I_{RXA}			34	mA	Analog interface
Supply Current TX I_{TXHGD}			80	mA	High band GMSK, digital
Supply Current TX I_{TXLGD}			65	mA	Low band GMSK, digital
Supply Current TX I_{TXHGA}			80	mA	High band GMSK, analog
Supply Current TX I_{TXLGA}			65	mA	Low band GMSK, analog
Supply Current Idle I_{MODE1}			5	mA	Reference and buffers on
Supply Current Idle I_{MODE2}			9	mA	Reference, buffer and AFC DAC
Supply Current Standby I_{SB}		130	170	uA	Digital supply on, clocks off
Maximum Current by Pin					
V_{DDRX} (pin 9)		14.5	TBD	mA	Worst case mode of operation
V_{CC} (pin 18)		10.5	TBD	mA	Worst case mode of operation
V_{CCV} (pin 24)		42.0	TBD	mA	Worst case mode of operation
V_{DD} (pin 47)		11.2	TBD	mA	Worst case mode of operation

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Performance Specifications					
SDI Write to RXEN or TXST	200			ns	Delay from SDI write to RXEN or TXST
RX_EN to Valid Data Start			200	µs	DCR mode
			160	µs	VLIF mode
TX_ST to Valid Data Start			140	µs	
Modulation Accuracy					
TX RMS Phase Error		1.1	3.0	°	
TX Peak Phase Error		5.0	7.0	°	
TX 400kHz GMSK Spectrum			-60	dBc	30kHz RBW rel to mod peak
VCO1					External inductor Q≥30.
Frequency Range (F_{VCO1})	824		915	MHz	
Phase Noise at 20MHz (L_F)			-164	dBc/Hz	
Power Out	3			dBm	
Frequency Pushing		4		MHz/V	V_{CCV}±0.15V
Frequency Pulling			1	MHz	2:1 VSWR all phases
Output VSWR			2.5:1		
VCO2					
Frequency Range (F_{VCO2})	1710		1910	MHz	
Phase Noise at 20MHz (L_F)			-155	dBc/Hz	
Power Out	3			dBm	
Frequency Pushing		4		MHz/V	V_{CCV}±0.15V
Frequency Pulling			1	MHz	2:1 VSWR all phases
Output VSWR			2.5:1		

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PLL Specification					
Frequency Range	0		2100	MHz	Internal
	0		550	MHz	FIN pin
Input Level (FIN pin)	50			mV_{RMS}	
Input Impedance (FIN pin)		2kΩ//2pF			On PC board
Phase Detector Frequency (F_R)			26	MHz	
PLL Bandwidth		90		kHz	TX mode
		50		kHz	RX mode
Phase Noise at 50kHz		-80		dBc/Hz	RX mode
		-102		dBc/Hz	TX mode, VCO1
		-95		dBc/Hz	TX mode, VCO2
Output RF Spectrum due to Modulation					
200kHz		-86.3	-83.3	dBc/Hz	
250kHz		-89.3	-86.3	dBc/Hz	
400kHz		-116.3	-113.3	dBc/Hz	Low band
400kHz		-113.8	-110.8	dBc/Hz	High band
600kHz to <1800kHz		-116.3	-113.3	dBc/Hz	
1800kHz to <3000kHz		-126.5	-123.5	dBc/Hz	
3000kHz to <6000kHz		-126.5	-123.5	dBc/Hz	
≥6000kHz		-134.5	-131.5	dBc/Hz	
Total Integrated Noise			1	°rms	
RX PLL Spurious Outputs			-65	dBc	600kHz to 1.6MHz
ETSI Spec Limits			-75	dBc	1.6MHz to 3MHz
			-85	dBc	>3MHz low band
			-82	dBc	>3MHz high band
			-108	dBc	Out of band
PLL Warm-up Time			140	µs	TX mode
			150	µs	RX mode
Reference Oscillator Input VCTCXO (OSCA Pin)					
Frequency Range (F_R)	0		26	MHz	
Input Level (V_{INR})	250			mV_{RMS}	
Input Impedance (Z_{INR})		5kΩ//2pF			On PC board
Phase Noise			-150	dBc/Hz	At 100kHz offset and above (external TCXO)
Reference Oscillator Input Crystal (If Used)					
Beckmann Curve Discontinuities			0.2	ppm	
Crystal Startup Time			1	ms	
Crystal Load Capacitance		10.5		pF	
Crystal Case Capacitance		2.5	4.0	pF	
Pullability		30		ppm/pF	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Oscillator Output Buffer					
Output Voltage (V_{OUT})	800			mV_{P-P}	Load: 10kΩ//10pF
Output Frequency	13		26	MHz	Selected by OSCOM pin
Phase Noise			-115	dBc/Hz	SSB @ 50kHz
			-120	kHz	SSB @ 100kHz
			-125	dBc/Hz	SSB @ 400kHz
Harmonic Level			-10	dBc	3rd harmonic
			-60	dBc	35th harmonic
Load Resistance	10			kΩ	Shunt
Load Capacitance	5		30	pF	Shunt
DAC1 and DAC2 Specifications					
Resolution ($RES_{D/A}$)	12.5	14.0		bits	Effective number of bits
Sample Rate (F_S)		26		MHz	
Lowpass Filter Bandwidth ($BW_{D/A}$)	120	128	136	kHz	
Lowpass Filter Order ($N_{D/AF}$)		6			Butterworth
Turn On Time			15	μs	Within 10mV
Output Noise Floor			500	nV/rtHz	At 100kHz offset
Offset Error (V_{OFF})		20	40	mV	
Gain Error (G_{ERROR})		TBD		%	
Output Range ($FS_{D/A}$)	0.1		VCC-0.1	V	
Output Resistive Load ($R_{D/A}$)	30			kΩ	
Output Capacitive Load ($C_{D/A}$)			500	pF	
DAC2 (AFC) Tri-State Output Impedance		160		kΩ	DAC2EN=0
RX ADC Specifications					Pins: IIN, IBIN, QIN, QBIN
Bandwidth ($BW_{A/D}$)	200			kHz	
Resolution ($RES_{A/D}$)	12	13		bits	Effective number of bits
Input Voltage ($V_{CMA/D}$)		1.25		V	Common mode voltage
Input Level ($FS_{A/D}$)			1	V_{P-P}	Measured differentially
Input Impedance ($Z_{INA/D}$)		30		kΩ	Single-ended
Sample Rate (F1)		13		MHz	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Composite Digital Filtering and Downconversion					
Output Word Length	12		16	bits	
Output Word Rate	13/48		13/12	MHz	
100kHz VLIF Mode					
Passband Ripple			1	dB	All bandwidths
Group Delay					Composite with RF2716
	43.0	43.2	43.5	us	BW=80kHz and 85kHz
	30.1	30.3	30.6	us	BW=90kHz and greater
Group Delay Variance		2		ns	RF6001 only
Group Delay Variance at Bandwidth Edge					Worst case composite with RF2716
	237	273	367	ns	BW=80kHz
	250	289	409	ns	BW=85kHz
	264	307	464	ns	BW=90kHz
	281	330	538	ns	BW=95kHz
	301	358	634	ns	BW=100kHz
	360	443	911	ns	BW=110kHz
	453	582	1321	ns	BW=120kHz
	693	944	2108	ns	BW=135kHz
3dB Corner Frequency					Composite with RF2716
		80.0		MHz	BW=80kHz
		85.4		MHz	BW=85kHz
		87.2		MHz	BW=90kHz
		94.0		MHz	BW=95kHz
		97.2		MHz	BW=100kHz
		107.8		MHz	BW=110kHz
		118.3		MHz	BW=120kHz
		133.3		MHz	BW=135kHz
Attenuation at -600kHz	-100			dB	All bandwidths
Attenuation at -400kHz	-60			dB	All bandwidths
Attenuation at -200kHz	-35			dB	BW=80kHz and 85kHz
	-40			dB	BW=90kHz and 95kHz
	-50			dB	BW=100kHz and greater
Attenuation at +200kHz	-40			dB	BW=80kHz and 85kHz
	-55			dB	BW=90kHz and greater
Attenuation at +400kHz	-100			dB	All bandwidths
Attenuation at +600kHz	-100			dB	All bandwidths

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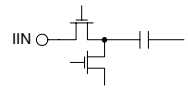
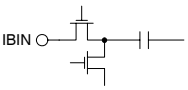
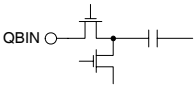
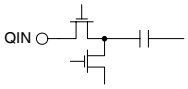
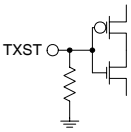
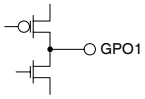
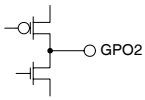
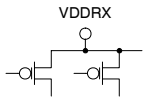
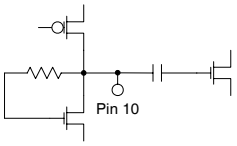
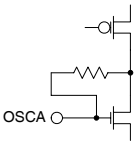
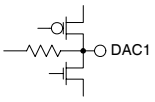
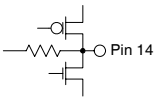
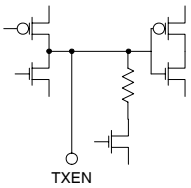
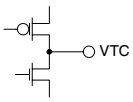
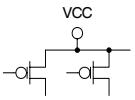
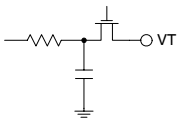
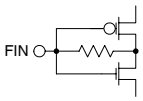
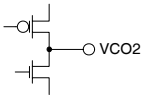
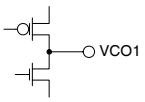
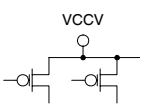
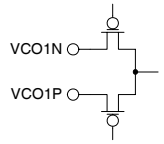
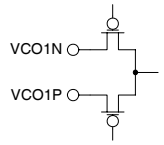
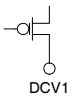
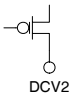
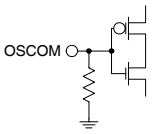
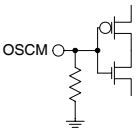
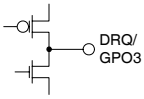
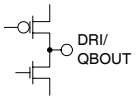
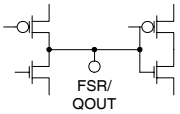
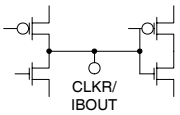
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Composite Digital Filtering and Downconversion, cont'd.					
DCR Mode					
Passband Ripple			0.5	dB	All bandwidths except 85kHz
			1.0	dB	BW=85kHz
Group Delay					Composite with RF2716
	43.0	43.2	43.5	us	BW=80kHz and 85kHz
	30.1	30.3	3.06	us	BW=90kHz and greater
Group Delay Variance		2		ns	RF6001 only
Group Delay Variance at Bandwidth Edge					Composite with RF2716
	228	256	341	ns	BW=80kHz
	241	271	369	ns	BW=85kHz
	253	286	406	ns	BW=90kHz
	267	303	456	ns	BW=95kHz
	282	324	521	ns	BW=100kHz
	325	383	720	ns	BW=110kHz
	392	481	1035	ns	BW=120kHz
	572	752	1750	ns	BW=135kHz
3dB Corner Frequency					Composite with RF2716
		80.8		MHz	BW=80kHz
		85.4		MHz	BW=85kHz
		89.8		MHz	BW=90kHz
		96.5		MHz	BW=95kHz
		100.1		MHz	BW=100kHz
		110.2		MHz	BW=110kHz
		119.8		MHz	BW=120kHz
		136.1		MHz	BW=135kHz
Attenuation at -600kHz	-100			dB	All bandwidths
Attenuation at -400kHz	-60			dB	All bandwidths
Attenuation at ±200kHz	-35			dB	BW=80kHz and 85kHz
	-45			dB	BW=90kHz and 95kHz
	-50			dB	BW=100kHz and greater
Attenuation at +400kHz	-100			dB	All bandwidths
Attenuation at +600kHz	-100			dB	All bandwidths

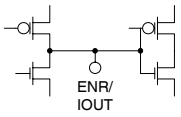
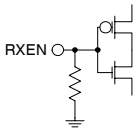
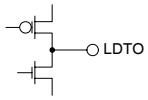
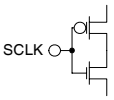
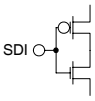
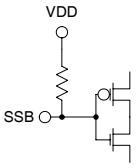
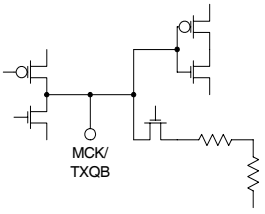
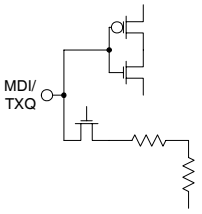
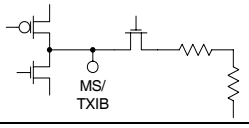
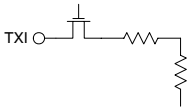
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX D/A Converters					pins: IOUT, IBOUT, QOUT, QBOUT
Resolution ($RES_{D/A}$)	12			bits	Effective number of bits
Sample Rate (Fs)		13		MHz	
Lowpass Filter Bandwidth ($BW_{D/A}$)	140	150	160	kHz	
Lowpass Filter Order ($N_{D/AF}$)		6			hybrid Butterworth/Bessel
IQ Differential Offset		10		mV	
IQ Gain Mismatch		0.1	0.5	dB	
Common Mode Voltage		$V_{DDRX}/2$		V	
Output Voltage Range ($FS_{D/A}$)	0		2.0	V_{P-P}	differential, 0dB gain
Output Resistive Load ($R_{D/A}$)	30			kΩ	each signal
Output Capacitive Load ($C_{D/A}$)			50	pF	each signal
GMSK I/Q Interface					Pins: TXI, TXIB, TXQ, TXQB
I/Q Input Voltage ($V_{CMI/Q}$)	1.00	1.25	1.50	V	Common mode
I/Q Input Level ($V_{PI/Q}$)	0.5	1.0	1.20	V_{PK}	Differential
Input Impedance ($Z_{INI/Q}$)	30			kΩ	
Digital Input Specifications					Apply to pins: SSB, SDI, SCLK, RXEN, TXST, TXEN, MCK, MDI, MS, OSCM, OSCOM, CLKR
Input High Voltage (V_{IH})	$0.7V_{DD}$			V	
Input Low Voltage (V_{IL})			$0.3V_{DD}$	V	
Input High Current (I_{IH})			50	µA	
Input Low Current (I_{IL})			50	µA	
Input Setup Time* (T_{SU})	10			ns	
Input Hold Time* (T_{HLD})	10			ns	
Input Rise/Fall Time (T_{RFI})			15	ns	
Input Clock to Select Time (T_{CS})	10			ns	
Input Clock Pulse Width High (T_{CWH})	15			ns	
Input Clock Pulse Width Low (T_{CWL})	15			ns	
Input Capacitance (C_{IN})			650	fF	
Digital Output Drivers					Apply to pins: LDTO, ENR, CLKR, FSR, DRI, MCK, MS
Output High Voltage (V_{OH})	$0.8V_{DD}$			V	With 1mA load
Output Low Voltage (V_{OL})			$0.2V_{DD}$	V	With 1mA load
Output Rise/Fall Time (T_{RFO})			5	ns	With 20pF maximum load capacitance
GPO Output Drivers					Apply to pins: GP01, GP02 and DRQ/GP03.
Output High Voltage (V_{OH})	V_{DD}-0.05			V	With 1mA load
	V_{DD}-0.45			V	With 10mA load
Output Low Voltage (V_{OL})			0.02	V	With 1mA load
			0.2	V	With 10mA load

* Setup and Hold Times are measured from the time where the waveforms cross $V_{DD}/2$.

Pin	Function	Description	Interface Schematic
1	IIN	Non-inverting input of the I channel A/D converter, to be connected to I out of the RF2722. Analog input.	
2	IBIN	Inverting input of the I channel A/D converter, to be connected to IB out of the RF2722. Analog input.	
3	QBIN	Inverting input of the Q channel A/D converter, to be connected to QB out of the RF2722. Analog input.	
4	QIN	Non-inverting input of the Q channel A/D converter, to be connected to Q out of the RF2722. Analog input.	
5	TXST	Transmit start. A rising edge on this signal initiates the transmit sequence (PA ramp up). A falling edge on this signal begins the transmit shut down sequence (PA ramp down). Digital input with weak pulldown.	
6	GPO1	General purpose output 1. This pin can be used to control a T/R switch. General purpose digital output (GPO).	
7	GPO2	General purpose output 2. This pin can be used to control a T/R switch. General purpose digital output (GPO).	
8	DCAD	Digital Receiver, ADC, and DAC voltage regulator output. A decoupling capacitor is required to ground. DC output voltage of 2.5V when the receive circuits are enabled.	
9	VDDRX	Receive power supply. Supply filtering components may be required in some applications (e.g. series resistor and shunt capacitor). Note that series resistance to this pin will drop the supply voltage. The specified supply voltage range needs to be present on this pin during operation.	
10	OSCB	Reference oscillator B input. When used with the internal reference oscillator this pin is connected to an external 26MHz crystal. If an external TCXO is used, this pin should be floating. This pin possesses a DC voltage and may require a DC-blocking cap in some applications. DC voltage equal to VDD when the oscillator is off (OSCM pin low); DC voltage of approximately 1V when used with a crystal; DC voltage of approximately 2.4V when used with a TCXO. Analog input.	
11	OSCA	Reference oscillator A input. When used with the internal reference oscillator this pin is connected to an external 26MHz crystal. If an external TCXO is used, this pin should be connected to the TCXO output through a decoupling capacitor. This pin possesses a DC voltage of approximately 1.25V and may require a DC-blocking capacitor in some applications. DC voltage equal to VDD when the oscillator is off (OSCM pin low). Analog input.	
12	NC	No connect.	

Pin	Function	Description	Interface Schematic
13	BGDC	Bandgap voltage regulator output. A decoupling capacitor is required to ground. DC output voltage of 1.25V.	
14	DAC1	DAC1 output. This pin is dedicated for the PA ramp control system when PAEN bit is set to logic 1. Buffered analog output.	
15	DAC2	DAC2 output. General purpose DAC that can be used for AFC control of the reference oscillator. Buffered analog output.	
16	TXEN	Transmit enable. Bi-directional digital pin. This pin can be used as an input or as an output of the PA ramp system. This signal is also used to enable the PA; for example, it should be connected to TX enable pin of the RF3146 PA. The direction of the pin is determined by the TXENIO bit. Digital input with weak pulldown or digital output.	
17	VTC	VCO coarse tuning control. This pin is connected to VTC pin on the RF2722 front end IC. Digital output.	
18	VCC	PLL power supply. Supply filtering components may be required in some applications (e.g., series resistor and shunt capacitor). Note that series resistance to this pin will drop the supply voltage. The specified supply voltage range needs to be present on this pin during operation.	
19	VT	PLL loop filter output. This pin should be connected to VT pin on the RF2722. Provides the correct tuning voltage to set the RX VCO to the programmed frequency. Low impedance analog output.	
20	FIN	PLL prescaler input. This pin should be connected to VCO OUT pin on the RF2722. Input impedance is specified in the PLL section of the electrical specifications. When probing this pin, the probe must have an effective DC resistance of 180kΩ minimum and <10pF capacitance.	
21	NC	No connect.	
22	VCO2	VCO2 output. DCS/PCS VCO output to the PA. This pin possesses a DC voltage and may require a DC blocking cap in some applications. Output impedance is specified in the VCO2 section of the electrical specifications.	
23	VCO1	VCO1 output. US cellular/EGSM output to the PA. This pin possesses a DC voltage and may require a DC blocking cap in some applications. Output impedance is specified in the VCO1 section of the electrical specifications.	
24	VCCV	VCO power supply. Supply filtering components may be required in some applications (e.g. series resistor and shunt capacitor). Note that series resistance to this pin will drop the supply voltage. The specified supply voltage range needs to be present on this pin during operation.	

Pin	Function	Description	Interface Schematic
25	VCO1N	VCO1 tank inductance, negative side. Used to complete resonant circuit for VCO1. Refer to the applications section of the datasheet for details.	
26	VCO1P	VCO1 tank inductance, positive side. Used to complete resonant circuit for VCO1. Refer to the applications section of the datasheet for details.	
27	DCV1	VCO1 regulator output. A decoupling capacitor is required to ground. DC output voltage of approximately 1.4V when VCO1 is enabled.	
28	GND	This pin should be tied to ground.	
29	DCV2	VCO2 regulator output. A decoupling capacitor is required to ground. DC output voltage of approximately 1.4V when VCO2 is enabled.	
30	OSCOM	Oscillator buffered output mode control. This pin controls the frequency of the OSCO (pin 48) output. A logic 0 on this pin results in 13MHz output and a logic 1 results in a 26MHz output. Digital input with weak pulldown.	
31	OSCM	Oscillator mode control. This pin controls the internal reference oscillator mode as described in the Reference Oscillator section. Digital input with weak pulldown.	
32	DRQ/GPO3	Digital serial RX data interface output for Q data. This pin provides the Q data while in digital RX interface mode and RXMODE(2:0) is set to 001 or 110. When S_MODE is low or RXMODE(2:0) is not equal to 001 or 110, this pin can be multiplexed and used as a third general purpose output(GPO3). This GPO can be used to control a T/R switch. Digital output.	
33	DRI/QBOUT	Digital serial RX data interface output or QB analog output. This pin is multiplexed between analog and digital RX output modes. The S_MODE bit sets the interface mode. Digital output or buffered analog output.	
34	FSR/QOUT	Digital serial RX data interface frame sync or Q analog output. This pin is multiplexed between analog and digital RX interface modes. The S_MODE bit sets the interface mode. The RXFSB bit determines the direction of the pin in digital mode. Digital input, digital output, or buffered analog output.	
35	CLKR/ IBOUT	Digital serial RX data interface clock or IB analog output. This pin is multiplexed between analog and digital RX output interface modes. The S_MODE bit sets the interface mode. The RXCKB bit determines the direction of the pin in digital mode. Digital input, digital output, or buffered analog output.	

Pin	Function	Description	Interface Schematic
36	ENR/IOUT	Digital serial RX data interface enable input or I analog output. This pin is multiplexed between analog and digital RX interface modes. The S_MODE bit sets the interface mode. Digital input or buffered analog output.	
37	RXEN	Receive path enable. Receive circuitry is active when a logic 1 is applied to this pin. Digital input with weak pulldown.	
38	LDTO	Lock detect/test digital output. This pin is multiplexed between various internal signals on the IC as defined by the TMUX and TEN bits. Digital output.	
39	SCLK	Serial data interface clock input. Digital input.	
40	SDI	Serial data interface data input. Digital input.	
41	SSB	Serial data interface select input. The serial interface accepts clock and data when SSB is at a logic 0 (active low). Digital input with weak pullup.	
42	MCK/TXQB	Modulation clock input/output or TXQB transmit analog input. This pin is multiplexed between analog and digital TX interface modes. The TXAD bit sets the interface mode. The TXD_MODE bit determines the direction of the pin in digital mode. Digital input, digital output, or analog input.	
43	MDI/TXQ	Modulation data input or TXQ transmit analog input. This pin is multiplexed between analog and digital TX interface modes. The TXAD bit sets the interface mode. Digital input or analog input.	
44	MS/TXIB	Modulation sync input/output or TXIB transmit analog input. This pin is multiplexed between analog and digital TX interface modes. The TXAD bit sets the interface mode. Digital input/output or analog input.	
45	TXI	TXI transmit analog input.	

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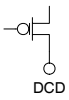
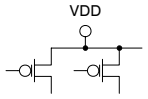
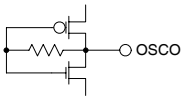
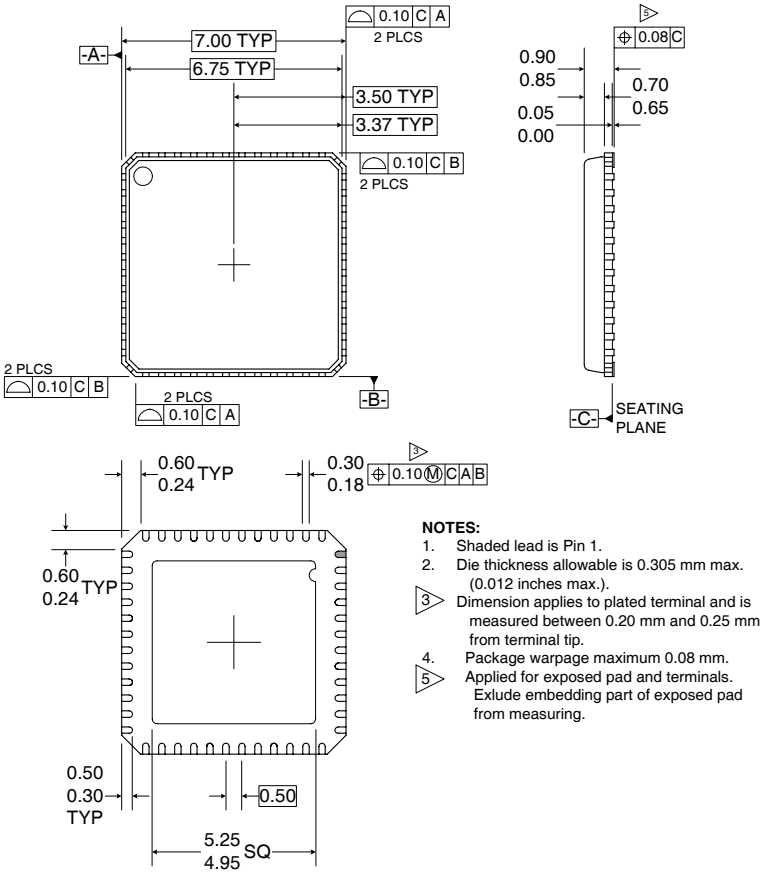
Pin	Function	Description	Interface Schematic
46	DCD	Digital voltage regulator output. A decoupling capacitor is required to ground. DC output voltage of 2.5V.	
47	VDD	Digital power supply. Supply filtering components may be required in some applications (e.g. series resistor and shunt capacitor). Note that series resistance to this pin will drop the supply voltage. The specified supply voltage range needs to be present on this pin during operation.	
48	OSCO	Buffered reference oscillator output. This pin can be used to provide the system clock for the radio. Analog output. DC output voltage of approximately 1.6V when OSCO is enabled.	

Packaging

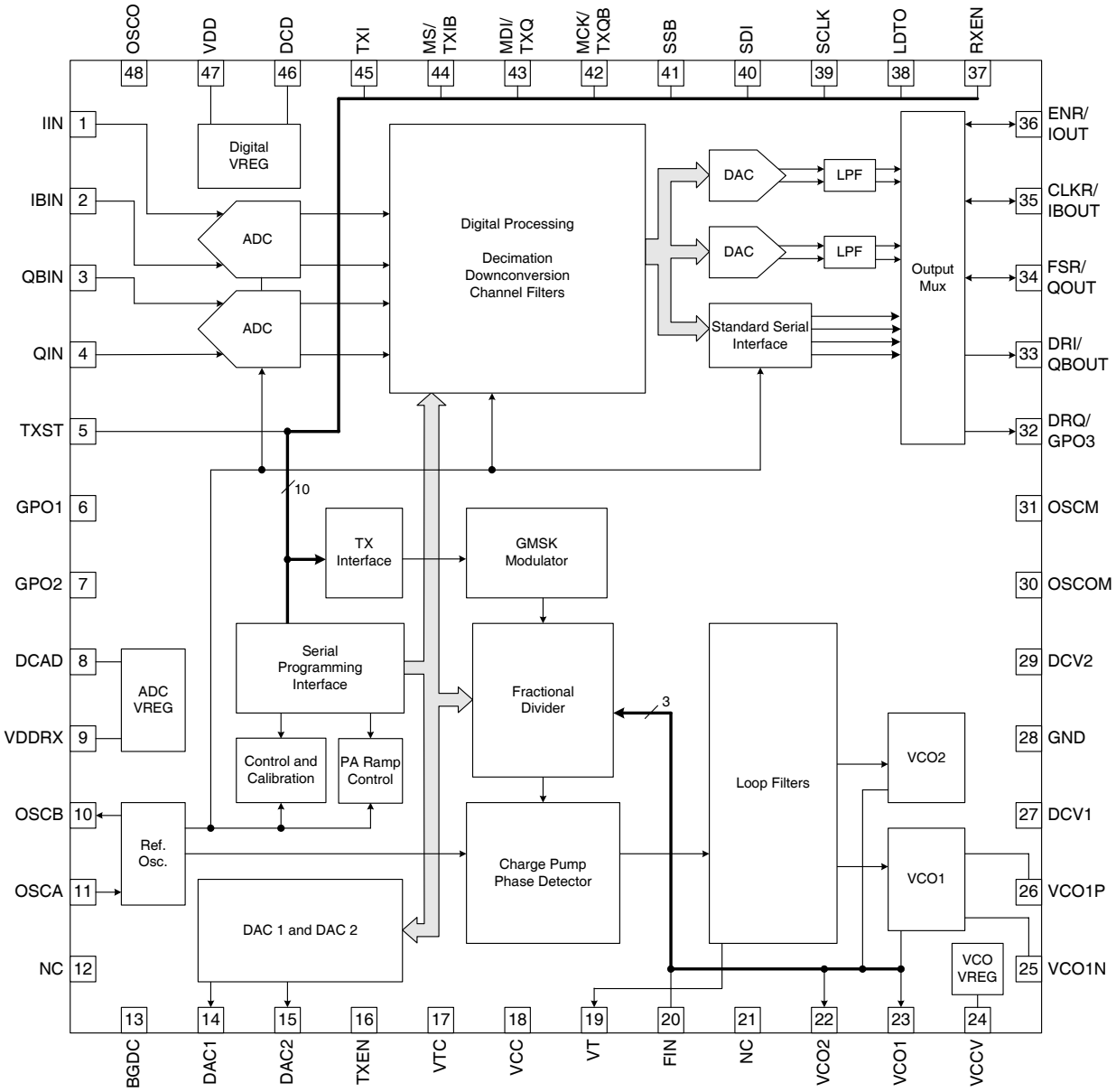
The device is packaged in a 48-pin leadless package with an outside dimension of 7mmx7mm and an exposed bottom-side ground flag.

Package Drawing



NOTES:
1. Shaded lead is Pin 1.
2. Die thickness allowable is 0.305 mm max. (0.012 inches max.).
3. Dimension applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
4. Package warpage maximum 0.08 mm.
5. Applied for exposed pad and terminals. Exlude embedding part of exposed pad from measuring.

Detailed Functional Block Diagram



Application Information

Functional Description

The RF6001 is a highly integrated receive and transmit processor intended for GSM/GPRS/EDGE$_{RX}$ applications. It contains the following functionality: A high performance fractional-N PLL, baseband digital filtering with A/D's and D/A's for GSM VLIF reception, two power transmit VCO's, GMSK modulator, PA ramp control DAC, and oscillator AFC control (reference oscillator circuitry). The fractional-N synthesizer section is multiplexed between transmit and receive functions, creating two sets of PLL parameters. PLL10-PLL12 registers are intended to be used with the receive VCO on the RF2722 VLIF receiver IC and PLL20-PLL21 registers are used with the two internal power VCO's on the RF6001. Each PLL configuration has a fully integrated loop filter. The internal power VCOs are designed for use in all GSM transmit bands; VCO1 has a frequency range of 824MHz to 915MHz and VCO2 has a frequency range of 1710MHz to 1910MHz. Each VCO has a +3dBm minimum output power. Down conversion from VLIF to baseband and all necessary baseband filtering for GSM/GPRS/EDGE reception is implemented digitally, with programmable bandwidths ranging from 80kHz to 135kHz. The receive and transmit baseband interfaces can be configured to work with standard analog differential I/Q signals or fully digital signals depending on SDI programming. The GMSK modulator necessary for GSM signaling is also provided and feeds into the transmit Fractional-N synthesizer for direct modulation of the VCO's. There are also two D/As (DAC1/DAC2) provided; DAC1 is configured to provide programmable ramp control for the PA, and DAC2 for general-purpose DC tuning voltage applications. An automatic PA ramp control function is provided, which has programmable ramp shaping and timing.

Features of the part include:

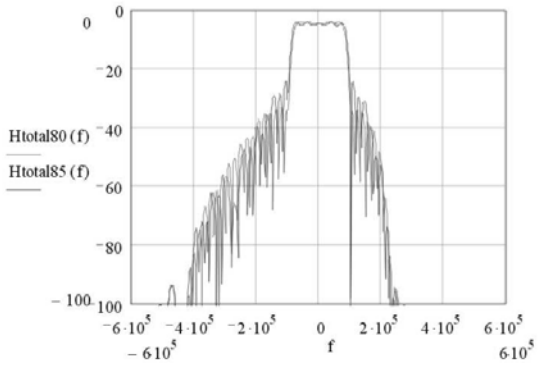
- A DC to 2.5GHz fractional-N PLL having:
  - Fine frequency resolution (typically 1.55Hz)
  - Charge pump with programmable current capability and operation to 5V
  - Integrated Loop Filters
  - Low Prescaler drive level requirement
- Two integrated RF transmit power VCO's with min +3dBm output power capability to drive PA's
- PA control system with GPRS support
- Power control DAC for PA ramp generation and programmable DAC for DC tuning voltage operation
- Programmable digital or analog TX interface to fractional-N GMSK modulation system
- I and Q channel digital filtering with 12-bit A/D's and D/A's for VLIF reception
- I and Q digital SSI interface with option for analog interface

This Device contains technology licensed under certain patents.

Receive Information

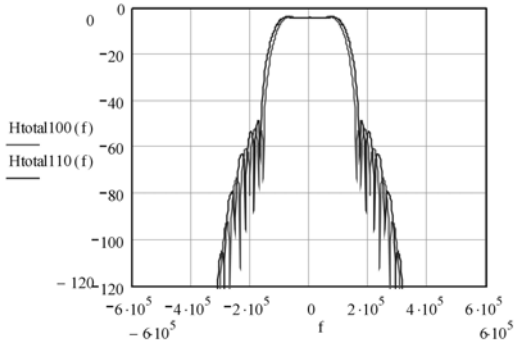
Composite Filter Responses

The stopband frequency response is shown below for the 80kHz and 85kHz channel bandwidths of the cascade of the RF2716/2722 and RF6001 in 100kHz VLIF mode. Note the notch at 100kHz. In this mode only the 80kHz and 85kHz bandwidths have this notch. Higher bandwidths may be used in this mode but a tone at 100kHz will be present due to any residual DC components converted by the VLIF offset.

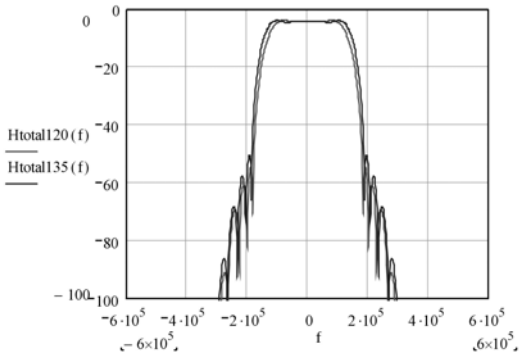


For the bandwidths of 90kHz and greater, the DCR mode is suggested. Residual DC errors will be present in the output in this mode.

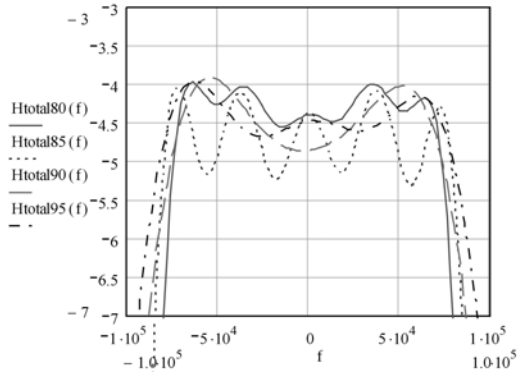
The stopband frequency response is shown below for the 100kHz and 110kHz channel bandwidths of the cascade of the RF2716/2722 and the RF6001 in DCR mode.



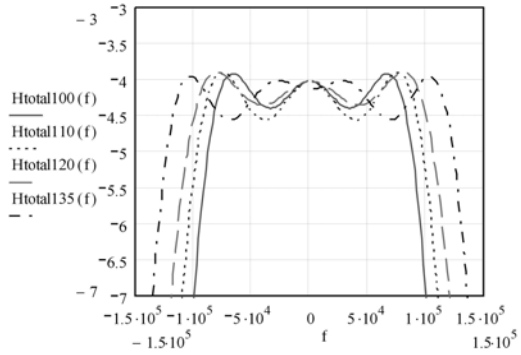
The stopband frequency response is shown below for the 120kHz and 135kHz channel bandwidths of the cascade of the RF2716/2722 and the RF6001 in DCR mode.



The passband frequency is shown below for the 80kHz, 85kHz, 90kHz, and 95kHz channel bandwidths of the cascade of the RF2716/2722 and the RF6001 in 100kHz VLIF mode.



The passband frequency is shown below for channel bandwidths of 100kHz, 110kHz, 120kHz, and 135kHz channel bandwidths of the cascade of the RF2716/2722 and the RF6001 in DCR mode.

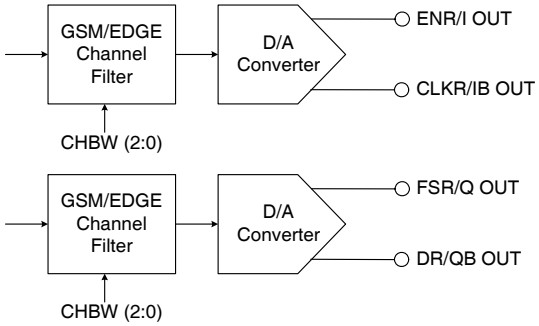


Baseband Output Interface

The output of the digital filtering system can be selected to be a digital SSI interface or to be an analog I and Q interface. The SPI bit S_MODE selects the digital mode if programmed high and selects the analog mode if programmed low.

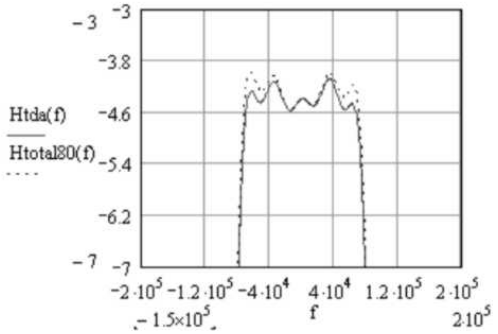
Analog Mode (S_MODE=0)

The block diagram presented below shows the interface in this mode of operation.

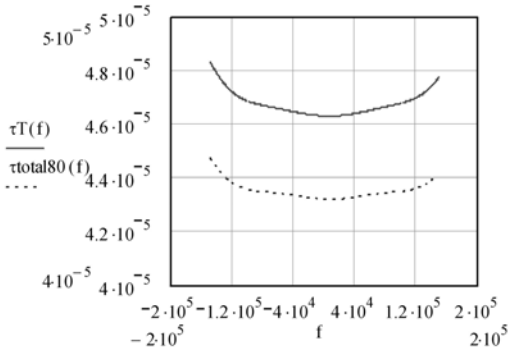


The analog outputs are intended to interface directly with existing baseband ICs which already contain 12 bit A/D converters.

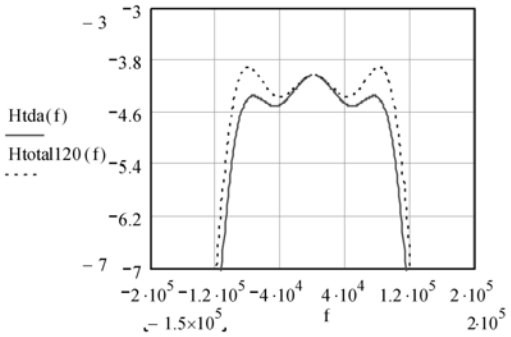
Due to the filters added to the D/A converter outputs, the group delay and channel bandwidths will be slightly modified. The plot below shows the amplitude response of the 80kHz channel bandwidth in 100kHz VLIF mode for the cascade of the RF2716/2722 and RF6001 with and without the D/A converter filter.

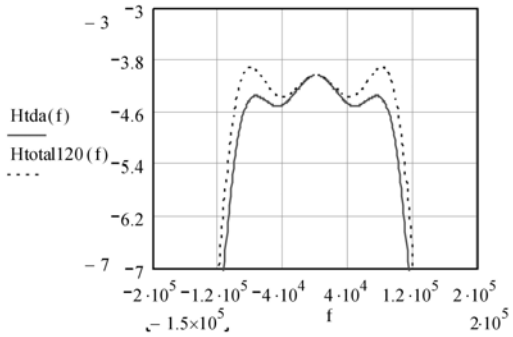


The plot below shows the group delay response of the cascade of the RF2716/2722 and the RF6001 with and without the D/A converter filter.



As a second example, the same two plots are repeated for a channel bandwidth of 120kHz in DCR mode.





RX Digital Mode (S_MODE=1)

If S_MODE is set true, the receiver baseband interface is configured to digital mode. In this mode:

ENR acts as the SSI bus enable pin.

CLKR acts as the clock output for the serial data transfer.

FSR acts as the frame sync output for the serial data transfer.

DRI and DRQ are the serial data outputs.

The following sections describe the various operational modes available.

Selection of RX Clocks and Sync as Inputs or Outputs
FSR can be configured as an input (RXFSB=1) or as an output (RXFSB=0).

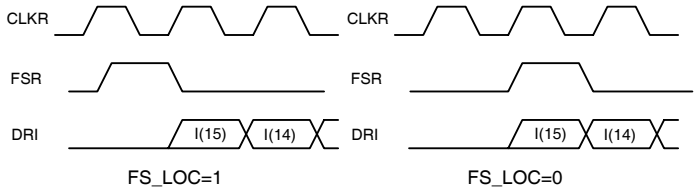
CLKR can be configured as an input (RXCKB=1) or as an output (RXCKB=0).

If CLKR is an input, then:

1. There must be at least two CLKR periods before valid data is output.
2. FSR can be an input or an output.
3. If FSR is also an input, then there must be at least two CLKR periods before FSR is externally set.

If CLKR is an output then FSR must be an output as well.

Selection of RX Sync Location Relative to Data
The position of FSR relative to the I channel MSB can be set with the SDI bit FS_LOC. If FS_LOC is set false then the FSR pulse occurs with the MSB of the I channel data as shown in all of the diagrams in the Digital RX SSI Mode section below. If FS_LOC is set true then the FSR pulse will occur on the clock immediately before the MSB of the I channel data.



Selection of RX SSI Enable Method
The digital RX SSI can be enabled by two methods. The first method is a physical pin labeled ENR. If ENR is set high then the RX SSI will activate two CLKR pulses after ENR rises. The sampling point of the digital filters is set by the position of RX_EN relative to the midamble and will not change with the position of ENR. The sample time of the SSI output word WILL move with the edge of ENR.

If ENR is set low then the RX SSI will deactivate after the current data transfer completes. This mode is active if the SDI bit EN_SEL is programmed low.

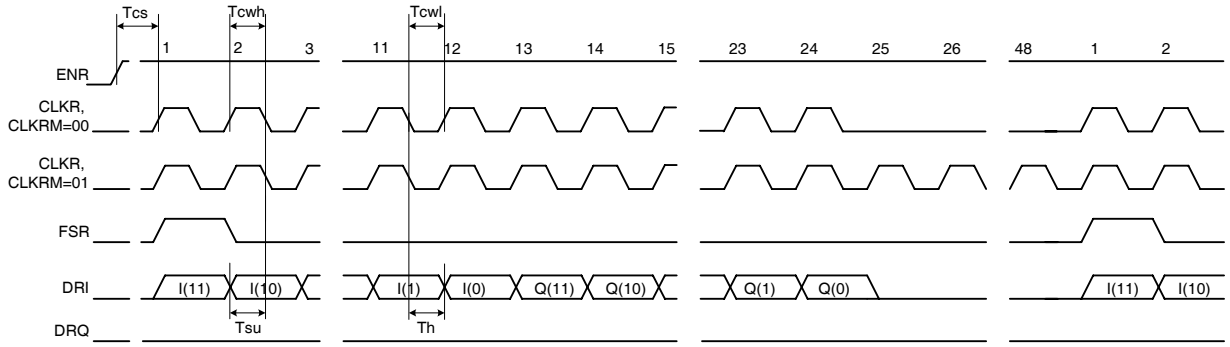
If EN_SEL is programmed high then the RX SSI activates with RX_EN high and deactivates with RX_EN low. All timing edges are relative to RX_EN.

Summary of Digital RX SSI Modes
The various digital receive modes are explained in detail below.

RXMODE=000, DBL=0
In this mode the SSI provides one sample of I and one sample of Q for each GSM symbol period. The output data pattern on DRI is 12 bits of I data followed by 12 bits of Q data followed by 24 blank bits. In this case FSR is (13/48)MHz=270.8333kbps and CLKR is 13MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

The following diagram summarizes this mode of operation.

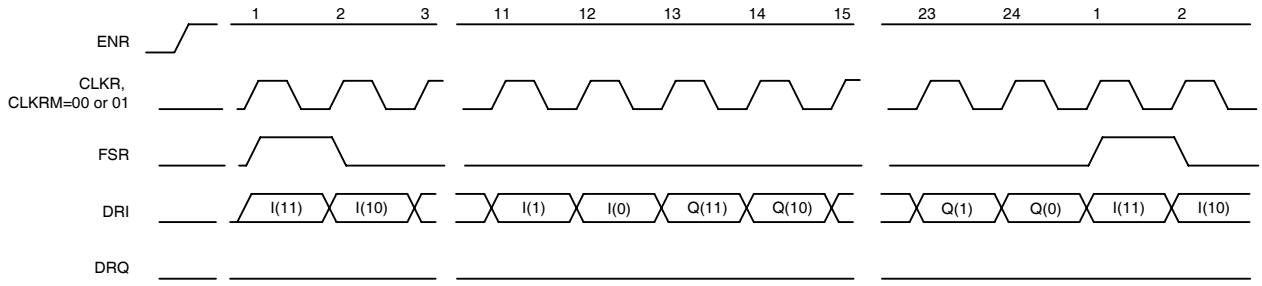


RXMODE=000, DBL=1

In this mode the SSI provides two samples of I and two samples of Q for each GSM symbol period. The output data pattern on DRI is 12 bits of I data followed by 12 bits of Q data. In this case, FSR is (13/24)MHz=541.667kbps and always marks the beginning of the I data transfer. CLKR is 13MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power (with RXMODE=000 and DBL=1, CLKR will always be enabled as there is no blank data); with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

The following diagram summarizes this mode of operation.



RXMODE=001, DBL=0

In this mode the SSI provides one sample of I and one sample of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 32 blank bits, and the output data pattern on DRQ is 16 bits of Q data followed by 32 blank bits. In this case FSR is (13/48)MHz=270.8333kbps and CLKR is 13MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

The following diagram summarizes this mode of operation.

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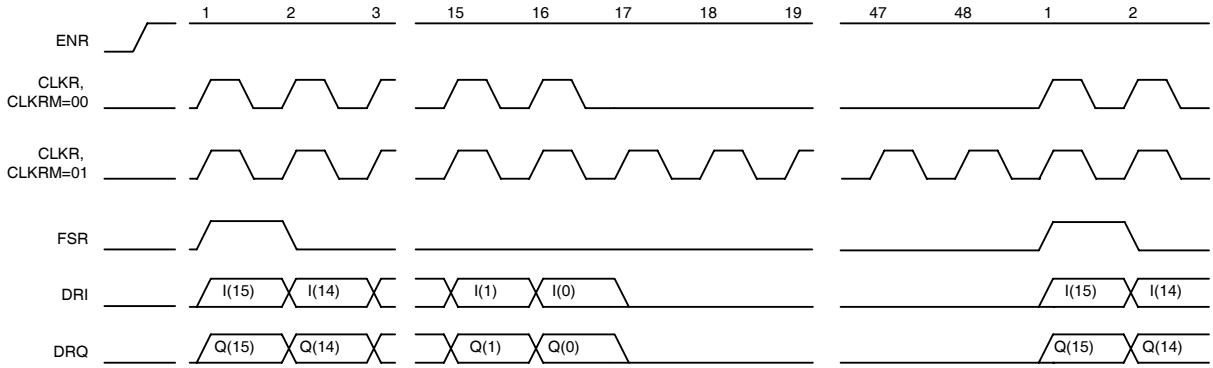
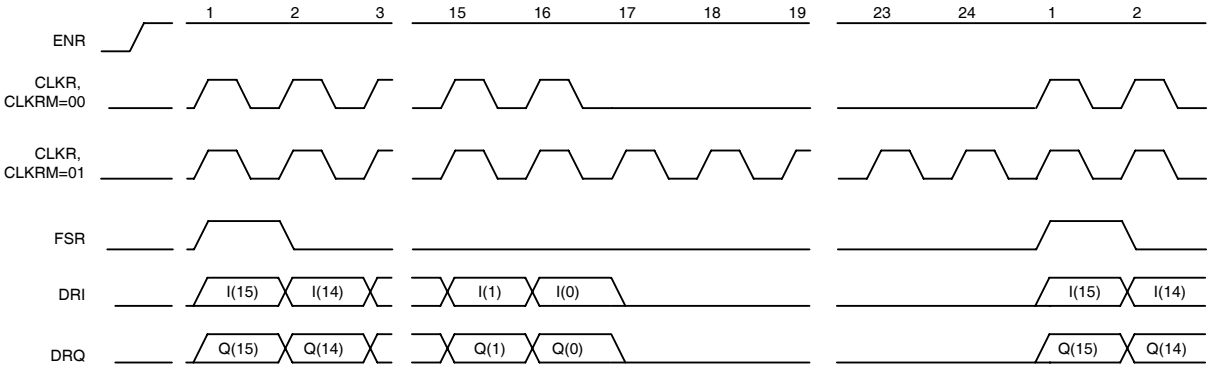


RXMODE=001, DBL=1

In this mode the SSI provides two samples of I and two samples of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 8 blank bits, and the output data pattern on DRQ is 16 bits of Q data followed by 8 blank bits. In this case, FSR is (13/24)MHz=541.667kbps and always marks the beginning of the I and Q data transfer. CLKR is 13MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

The following diagram summarizes this mode of operation.



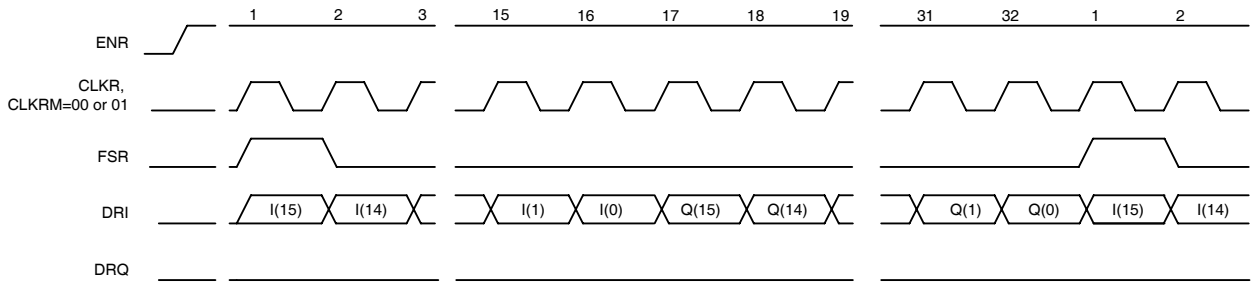
RXMODE=010

In this mode the SSI provides one sample of I and one sample of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 16 bits of Q data. In this case, FSR is (8.667/32)MHz=270.833kbps and always marks the beginning of the I data transfer. CLKR is 8.667MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power (with RXMODE=010, CLKR will always be enabled as there is no blank data); with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

DBL has no effect in this mode.

The following diagram summarizes this mode of operation.



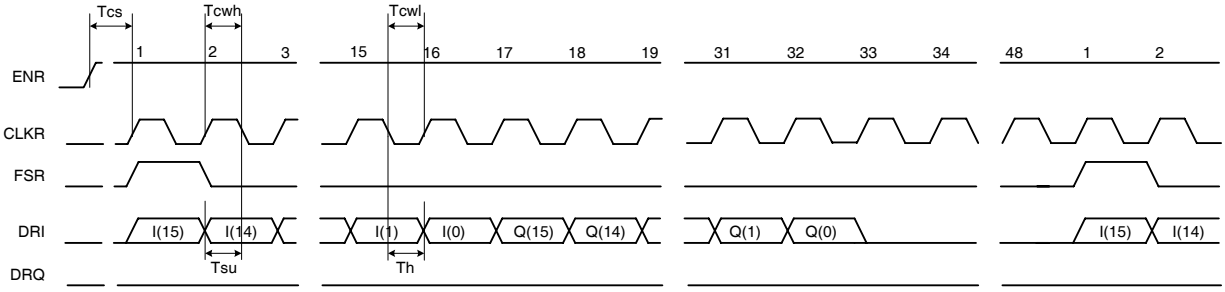
RXMODE=011

In this mode the SSI provides one sample of I and one sample of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 16 bits of Q data followed by 16 blank bits. In this case, FSR is (13/48)MHz=270.833kbps and CLKR is 13MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

DBL has no effect in this mode.

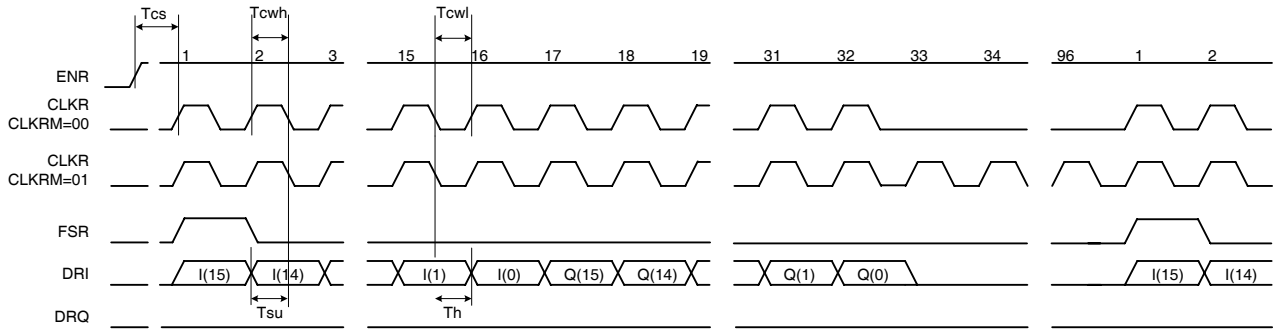
The following diagram summarizes this mode of operation.



RXMODE=100, DBL=0

In this mode the SSI provides one sample of I and one sample of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 16 bits of Q data followed by 64 blank bits. In this case FSR is (13/48)MHz=270.8333kbps and CLKR is 26MHz. The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

The following diagram summarizes this mode of operation.



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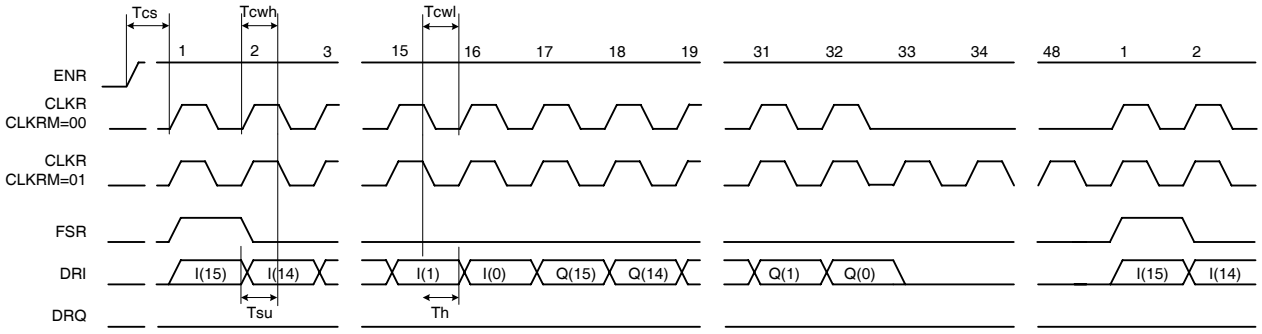
RXMODE=100, DBL=1

In this mode the SSI provides two samples of I and two samples of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 16 bits of Q data followed by 16 blank bits. In this case FSR is (13/24)MHz=541.667kbps and CLKR is 26MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

The following diagram summarizes this mode of operation.



RXMODE=101

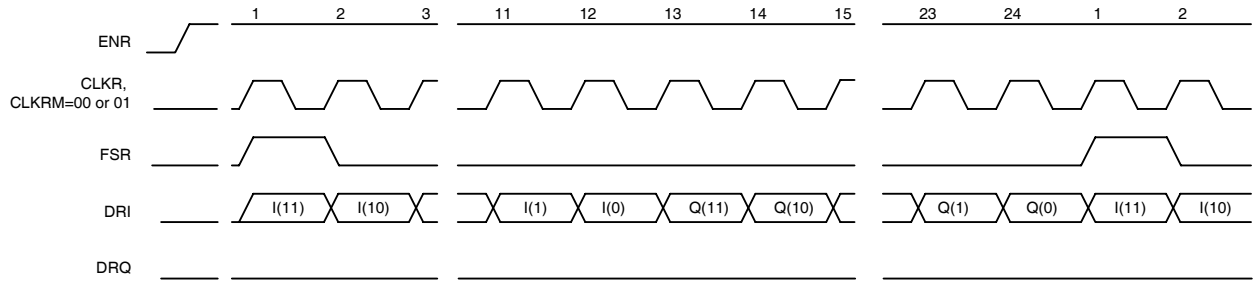
(Valid only for CHBW greater than or equal to 90kHz in 100kHz VLIF or DCR mode.)

In this mode the SSI provides four samples of I and four samples of Q for each GSM symbol period. The output data pattern on DRI is 12 bits of I data followed by 12 bits of Q data. In this case FSR is (13/12)MHz=1083.333kbps and CLKR is 26MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power (with RXMODE=101, CLKR will always be enabled as there is no blank data); with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

DBL will have no effect in this mode.

The following diagram summarizes this mode of operation.



RXMODE=110

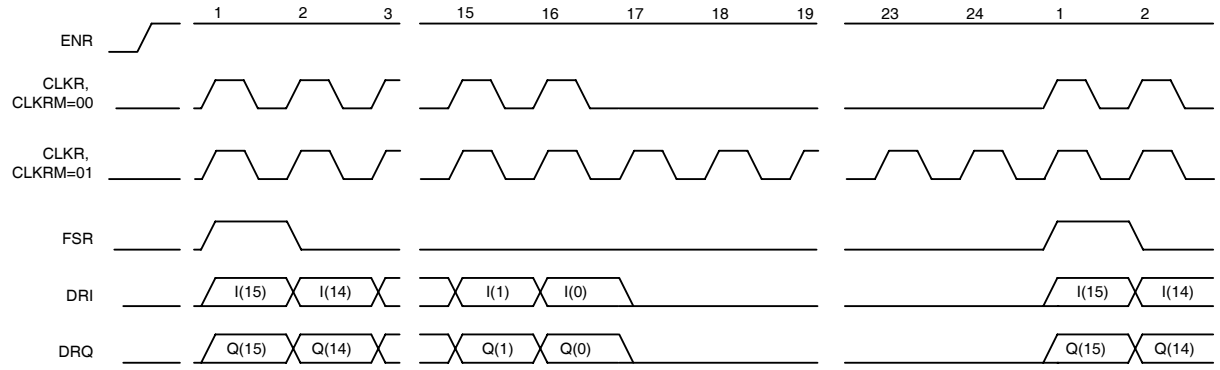
(Valid only for CHBW greater than or equal to 90kHz in 100kHz VLIF or DCR mode.)

In this mode the SSI provides four samples of I and four samples of Q for each GSM symbol period. The output data pattern on DRI is 16 bits of I data followed by 8 blank bits, and the output data pattern on DRQ is 16 bits of Q data followed by 8 blank bits. In this case, FSR is (13/12)MHz=1083.333kbps and always marks the beginning of the I and Q data transfer. CLKR is 26MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power; with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

DBL will have no effect in this mode.

The following diagram summarizes this mode of operation.



RXMODE=111 (valid only for CHBW greater than or equal to 90kHz in 100kHz VLIF or DCR mode)

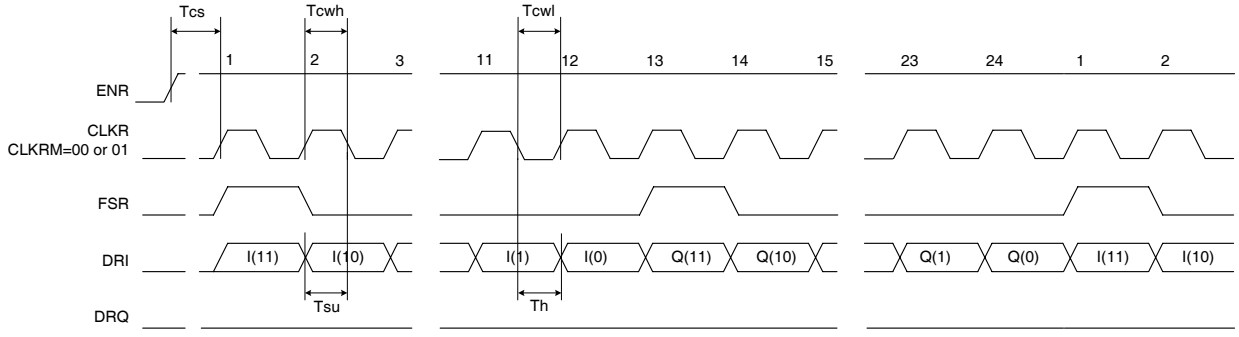
In this mode the SSI provides four samples of I and four samples of Q for each GSM symbol period. The output data pattern on DRI is 12 bits of I data followed by 12 bits of Q data. In this case, FSR is (13/6)MHz=2166.67kbps and CLKR is 26MHz.

The various CLKR modes are defined as follows: with CLKRM=00 and RXCKB=0, CLKR will shut down after the Q data transfer completes until the next I data transfer to save power (with RXMODE=111, CLKR will always be enabled as there is no blank data); with CLKRM=01 and RXCKB=0, CLKR is always enabled if ENR is true; with CLKRM=1x, CLKR is always disabled.

DBL will have no effect in this mode.

The first data field of 12 bits after ENR rises will always be the I word.

The following diagram summarizes this mode of operation.



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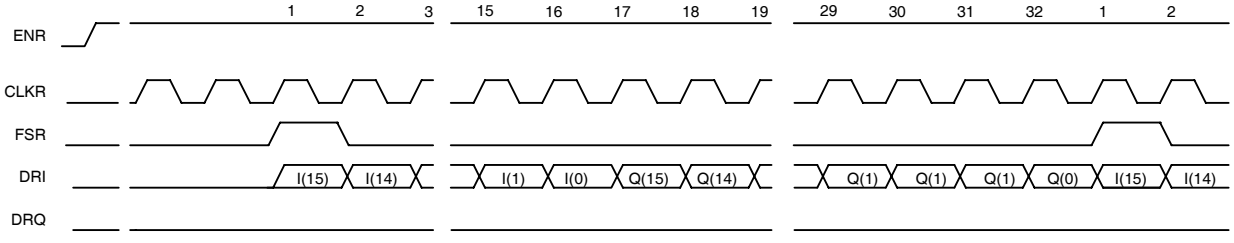
All of the above diagrams assumed that RXCKB=RXFSB=0. The diagram below presents an example with RXCKB=1 and RXFSB=0. This is an external (baseband) clock with the FSR sync generated by the RF6001.

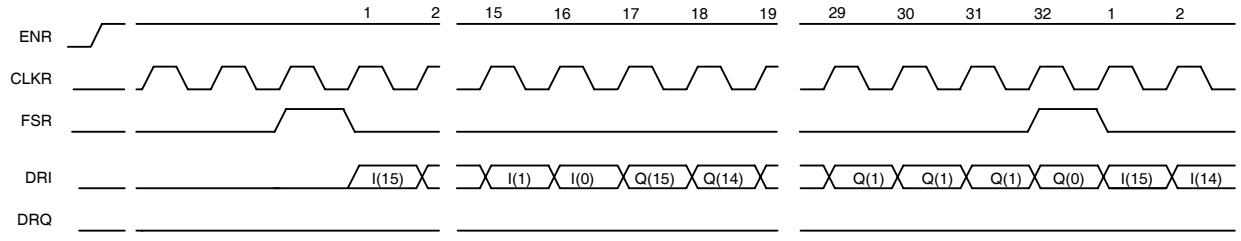
Note that the FSR pulse is located at the MSB of the I word, and that there will be two CLKR pulses output before FSR rises.

The same diagram will hold true with RXFSB=1 except in this case the sync is an input coming from the baseband part and the baseband must provide at least two CLKR pulses before asserting FSR.



RX_MODE=010
RXCKB=1, FS_LOC=0

If FS_LOC=1 then the sync pulse is advanced by one clock cycle as shown below.



RX_MODE=010
RXCKB=1, FS_LOC=1

DC Offset Correction

Fast Fine DC Adapt (FFDA)

The digital filters in the RF6001 perform a "fast fine DC adapt" (FFDA) which normally continues for about 50usec beyond the end of the CDCA (coarse DC adapt on RF2716/2722), and results in a DC error of less than 80uV at the baseband interface.

The FFDA is triggered by the RX_EN pin on the RF6001, which is normally exerted at the same time as the RX_EN of the RF2716/2722. This means that the FFDA runs during the CDCA as well, but has little effect during that time. The total time that the FFDA operates is set by RF6001 SDI fields DCAD and DCAD_2. During FFDA, the clock rate to the DC correction system is 13MHz.

The automatic operation of the FFDA can be disabled by programming SDI bits ADEN=0 and ADEN_2=0. Please note that, unlike with the CDCA in the RF2716/2722, there is no way to activate the FFDA in the RF6001 other than to assert a rising edge on RX_EN.

Slow Fine DC Adapt (SFDA)
Normally, once the FFDA timer has expired, the RF6001 fine DC correction system then holds the last value calculated until the RX_EN transitions to low at the end of the receive burst. However, the system can be configured setting the SDI bits AD2EN and AD2EN_2 to continue operating after the FFDA is completed in a lower bandwidth mode called the Slow Fine DC Adapt (SFDA). In this mode, the internal adaptation update rate would normally be lowered by a factor of 48 to reduce the group delay distortion. This SFDA rate is selected by the SDI fields ADCLK and ADCLK_2, and is adjustable from the default of 13/48MHz up to 13MHz.

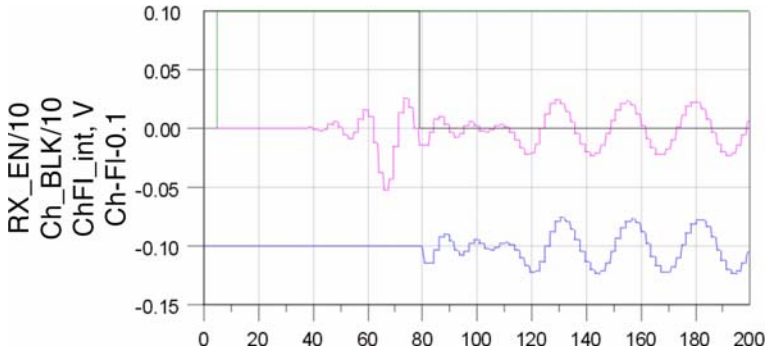
Once the fine DC adapt process is completed, the DC correction offsets internal to the RF6001 will be held until RX_EN is no longer asserted, power is removed from the IC, or another slow adapt operation is scheduled.

Realistically, it is unlikely that the SFDA mode will be used with GSM systems. This is because the SFDA would convert a DC error into a slowly moving AC error. Also, the GSM system will refresh the DC adapt on every frame, and thus a slow long term correction is not necessary.

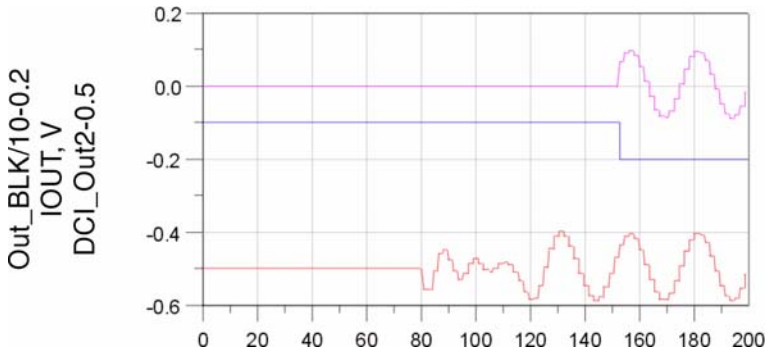
Digital Gain Control
SDI bits DAGC (3:0) can be used as a digital gain control with a range from -18dB to +60dB. This may be used to keep the RF6001 I/Q output voltages at a constant level for those baseband IC's that require this functionality.

Blanking
The receiver has two programmable blanking circuits. The first of these is controlled by the SDI field BLK_DLY and blanks the output of the channel filter so that the second DC offset correction block does not see the initial transients of the receiver. This reduces the amount of time needed to complete the second stage of the DC offset correction.

The upper line in the diagram below shows the channel filter output. The lower line shows the output of the BLK_DLY block as input to the second DC offset correction block.



The second blanking circuit is controlled by the SDI field AGC_DLY and blanks the I and Q outputs. This avoids large startup transients being sent to the baseband processing. The diagram below shows the action of the AGC_DLY field on the output signals.



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As initial guidance for the settings of the DC offset and blanking system, the following two setups are presented. Both are acceptable for GPRS operation. The 160usec option represents a minimum startup time. The 210usec startup option will minimize any DC errors due to initial thermal drift.

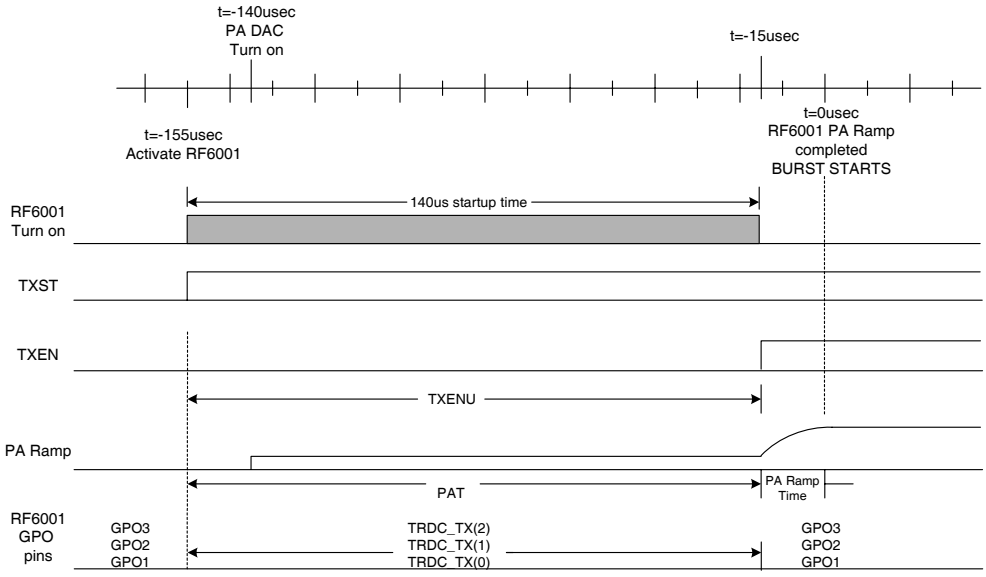
160usec Startup		
DCTIME1=20us	DCTIME2=140us	DCAD=23h=129.2us
BLK_DLY=1fh=114.5us	AGC_DLY=2ch=162.5us	DCAD_2=25h=136.6us
210usec Startup		
DCTIME1=20us	DCTIME2=180us	DCAD=30h=177us
BLK_DLY=2ch=162.5us	AGC_DLY=39h=210.5us	DCAD_2=32h=184.6us

Transmit Information

Transmit Turn-On Sequence

The following diagram documents the transmit turn-on sequence when using the RF6001 with the RF3146 power amplifier. The sequence is initiated by taking TXST signal high. The RF6001 requires 140μs worst case for all calibrations and PLL lock to take place. Once this is complete, the PA will be turned on by taking TXEN high (TXENU=140μs). The PA ramp should start about 2μs later for optimal switching spectrum performance of the RF3146 (PAT=142μs).

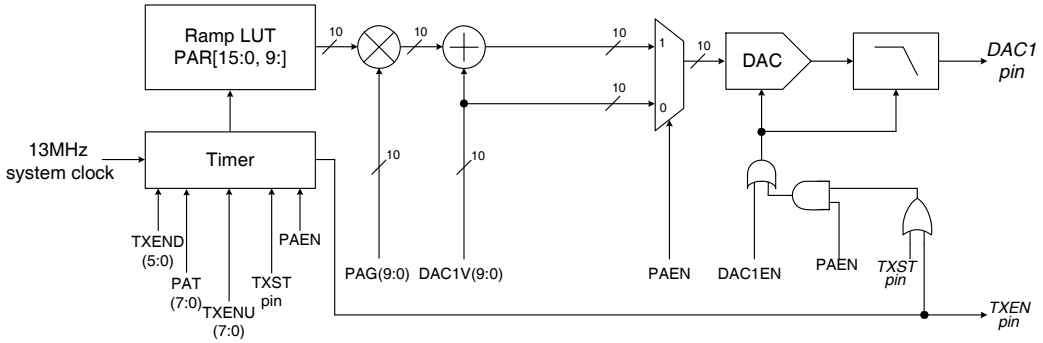
There is a programming feature within the RF6001 to provide real-time control of the front-end transmit/receive (T/R) switch. The T/R switch must be turned off during the prior bust to ensure the ETSI time-mask is not violated. This feature is invoked by setting TRD bit high. The GPO1, GPO2 and GPO3 outputs of the RF6001 will be set to values programmed into TRDC_TX(2:0) bits when TXST is taken high. These values should turn off the T/R switch for the given transmit state. After time TXENU, the GPO outputs of the RF6001 will revert back to the originally programmed states defined in SDI bits GPO1, GPO2 and GPO3.



PA Ramp Control

The RF6001 contains a PA ramp control system that operates through the DAC1 pin. The PA ramp control system is turned on by programming PAEN bit to one (1). The user programs the minimum DAC1 level into the DAC1V register, the desired PA ramp waveform sample values into the PAR registers, and a gain word into the PAG register.

A conceptual block diagram of the PA Ramp control system is illustrated below.



The timing diagram below illustrates a GSM transmit burst. In this case the GPRS_TX1 bit is programmed to zero (0). The transmit VCO and PLL should be turned on and given sufficient time to lock prior to starting modulation and the PA ramp. The modulation and ramp sequence is initiated by taking the TXST pin high. This starts the TX modulator (after a delay set by MD_DLY1), using data or modulation present on the GMSK modulation interface or stored in the First In First Out (FIFO), and turns on DAC1/VRAMP DAC, set to the value in the DAC1V register (the minimum value). (If modulation is not desired, the modulation interface should be set to digital mode, and the TX input pins should be held inactive.) The TXEN pin is an output used to enable the PA. This pin will go high after the rising edge of the TXST input pin with a delay programmed by the SDI field TXENU.

The PA ramp waveform starts after time PAT relative to the rising edge of TXST. The 16 steps in the PAR registers (PARAMP3-PARAMP11) are swept at a rate of (12/13)µs with an interpolation by 2 to result in a rate of (6/13)µs per step. DAC1 remains at the maximum value of the PA ramp waveform until TXST is taken low, at which point the PAR waveform is used to ramp the DAC1 signal back down to the DAC1V value. The DAC and modulation shut off and the TXEN pin goes low after the ramp down is completed and following a delay programmed by the SDI field TXEND. The DAC1 signal is defined by the following equation:

$$PA_{RAMP} = \left[\frac{PAG \cdot PAR}{1024} + \frac{DAC1V}{65536}\right] \cdot 2.5V$$

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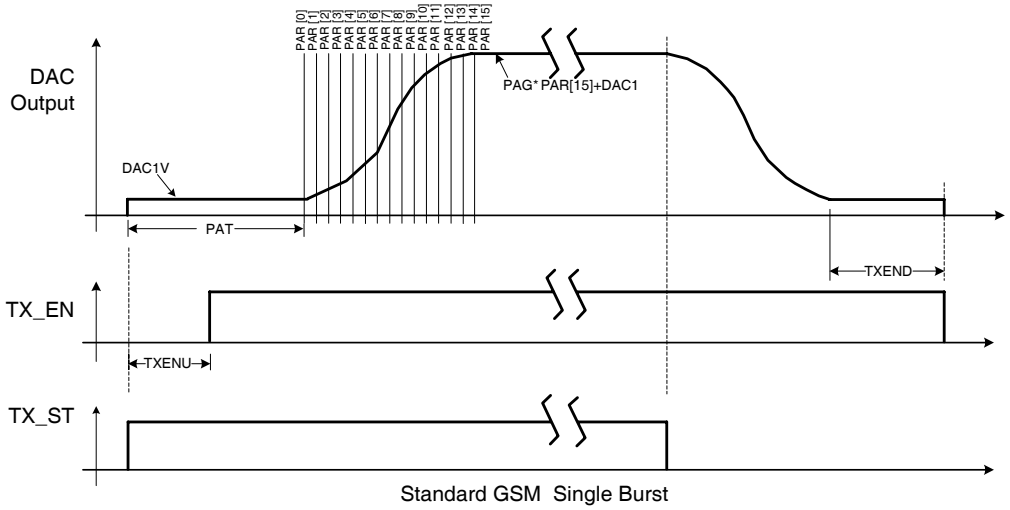
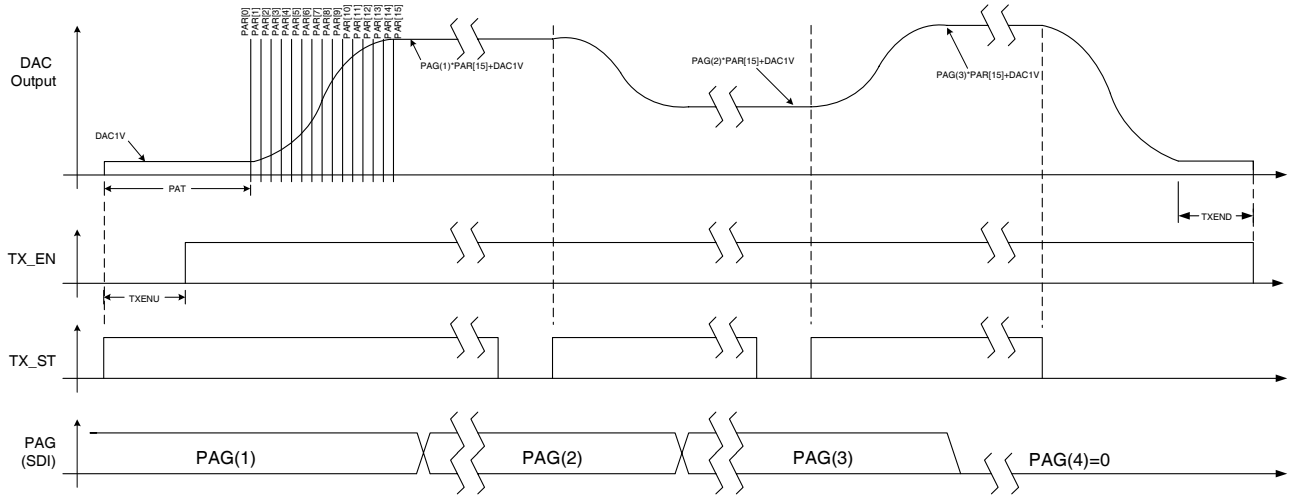


Standard GSM Single Burst
(GPRS_TX1=0, GPRS_TX2=0)

The next diagram illustrates operation of the PA ramp control system for a GPRS transmit sequence. In this case, the GPRS_TX1 bit should be programmed to one (1), and GPRS_TX2 is set to zero (0). As in the GSM burst case, the sequence is initiated by taking the TXST pin high. The DAC1 pin will ramp to the output level set by the PAR and PAG settings. The new power level for the next GPRS slot should then be programmed into the PAG register. When TXST is taken low and then high again, the system will ramp to the new value in the PAG register, again using the waveform programmed into the PAR registers. (The change is initiated on the rising edge of TXST.) This can continue indefinitely until a PAG value of zero is programmed. The system will then ramp down to the minimum (DAC1V) value on the falling edge of TXST. The TXEN pin will then return low after a delay set by TXEND after the ramp down has completed.

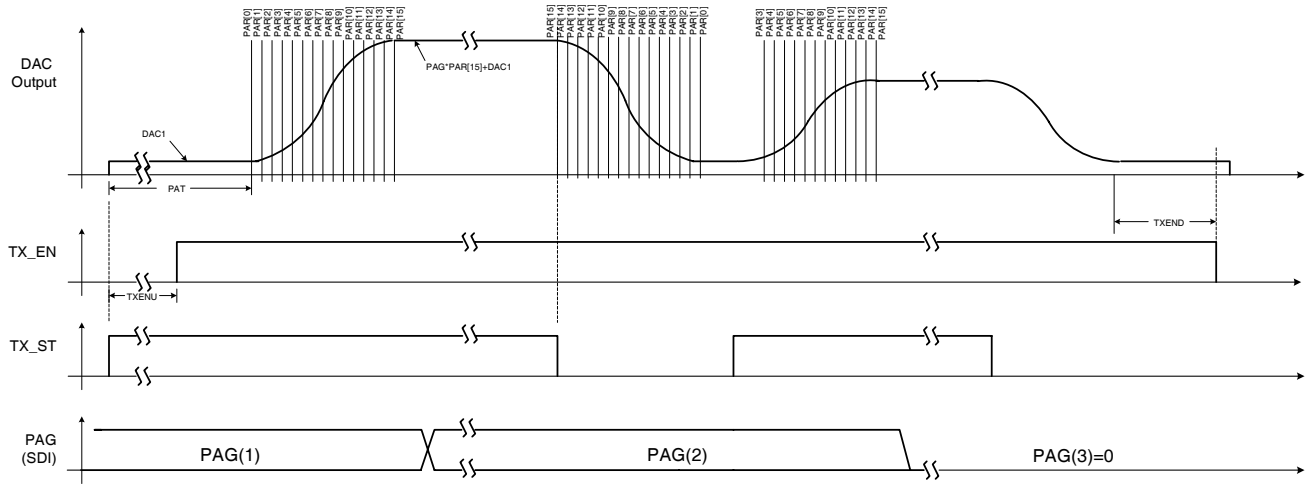


GPRS Mode 1
(GPRS_TX1=1, GPRS_TX2=0)

A second GPRS mode exists in the RF6001. Setting GPRS_TX1 to zero (0), and GPRS_TX2 to one (1) activates this mode. In this mode, the DAC is programmed to ramp down on the falling edge of TX_ST, and then ramp back up on the next rising edge of TX_ST. The next power level will change state on the rising edge of TX_ST. This forces any phase discontinuities to occur at minimum output power and this avoids any spectral purity issues. This is similar in operation to non-GPRS mode except that new parameters are loaded during the previous burst, and that the TX_EN pin will not return low after a ramp down unless the next power level programmed is zero.

To get one-eighth symbol time resolution (instead of full symbol resolution), MD_DLY2 may be used. MD_DLY2 is triggered when TX_ST goes high between bursts. In FIFO mode, once TX_ST is deasserted and the current bit cycle clock completes, the MD_DLY2 timer starts counting in one-eighth symbol resolution. During this time, the value stored in G_DEF will be sent to the modulator. When the MD_DLY2 counter times out, the FIFO begins shifting out data again. Serial mode functions in the same manner except the serial bit clock stops during MD_DLY2 and starts once the timer expires.

The diagram below shows this mode of operation.



GPRS Mode 2
(GPRS_TX1=0, GPRS_TX2=1, R1316B=1)

Since the minimum guard time (center of last tail bit to center of first tail bit) can be as short as 32qst, the ramp time of 16qst down and 16qst up would be marginally too long to fit the guard time. The SDI bit R1316B may be programmed high to shorten the ramp to be 13qst long instead of 16qst long. In this case, the ramp starts with PAR3 and ends with PAR15. The pre programmed ramp accessed with RMPSEL=1 is particularly convenient for use with this compressed ramp mode.

The SDI bit R0816B, may be programmed high to shorten the ramp to 8qst instead of 16qst. In this case, the ramp starts with PAR1 and will use every other entry in the ramp table ending with PAR15.

Two different ramp shapes can be selected by appropriately setting the RMPSEL bit. The default values of the PAR registers for each RMPSEL setting are shown below. These defaults were chosen so that when used with the RF3146 power amplifier, the GSM time-mask and transient spectrum due to switching conform to ETSI specifications. The defaults associated with RMPSEL=0 should be used for EGSM band, and the defaults associated with RMPSEL=1 should be used for DCS/PCS bands. User defined ramp shapes can be loaded into registers PAR0-PAR15, they must be scaled to start at 000h (0) and end at 3FFh (1023) to work properly with the PA ramp system.

	RMPSEL=0	RMPSEL=1

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PAR0	000h	000h
PAR1	000h	000h
PAR2	029h	000h
PAR3	076h	000h
PAR4	0CDh	051h
PAR5	128h	0C2h
PAR6	183h	13Fh
PAR7	1DFh	1BEh
PAR8	23Ch	237h
PAR9	299h	2A8h
PAR10	2F4h	30Bh
PAR11	349h	360h
PAR12	393h	3A4h
PAR13	3CDh	3D6h
PAR14	3F2h	3F4h
PAR15	3FFh	3FFh

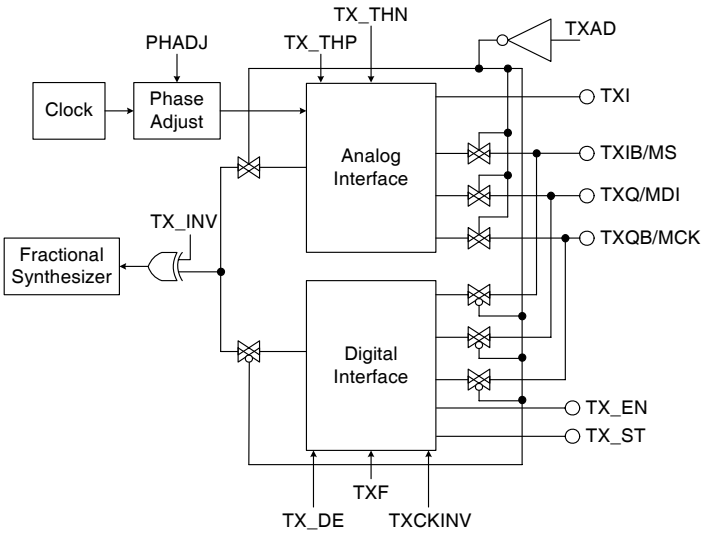
GMSK Modulation Interface

The GMSK modulation interface can be configured to accept analog I/Q inputs or digital data bits with or without differential encoding. This interface multiplexes some of the same pins for analog and digital modes, and consists of the following: TXI analog input (TXI), TXIB analog input or Modulation Sync input/output (TXIB/MS), TXQ analog input or Modulation Data Input (TXQ/MDI), TXQB analog input or Modulation Clock input/output (TXQB/MCK), Transmit Enable (TXEN), and Transmit Start (TXST). The SDI bit TXAD defines the state of the interface, if programmed false it will operate in analog mode and programmed true will operate in digital mode. If digital mode is selected, the TXI input is disabled. The diagram below documents the GMSK modulation interface to the fractional synthesizer, showing all programmable SDI bits necessary for setup.

The GMSK modulator block diagrams block performs the necessary pulse shaping to the decoded data bits in order to achieve GMSK modulation. Since this is done in the digital domain, there is a delay associated with this block of approximately 14.1µs. The I and Q transmit data should be sent early relative to the start of the burst to account for this delay.

Input analog or digital data may be differentially encoded in the RF6001 before the modulator. By setting the SDI bit TX_DE high (1), input data is differentially encoded by the RF6001. In addition, the initial state of the internal differential encoder may be selected with the DE_INIT bit. If the data has already been differentially encoded by the baseband, set the TX_DE bit low (0).

Transmit Modulation Interface



Digital Mode

Programming the TXAD bit high puts the GMSK modulation interface in digital mode, and the TXI input is disabled. The MS and MCK signals can be generated by either the RF6001 or the baseband, as configured by SDI bit TXD_MODE.

The data on MDI can be differentially encoded by setting SDI bit TX_DE true. If the data has already been differentially encoded by the baseband, the TX_DE should be set false to bypass the differential encoder.

TX_INV inverts the data at the output of the differential encoder.

The RF6001 also contains a 312 bit FIFO. The FIFO allows up to two timeslots of GMSK data to be loaded before the transmission begins.

Addition of Delay on MCK

The FIFO needs a rising edge on MCK to set the pointer before data is read on the falling edge of MCK. If MCK is inactive high then there is no rising edge on the first transfer as MCK is already high.

A rising edge is thus created by ANDing MCK and MS. This is fine except at the end of the data transfer. At this point the baseband simultaneously drops MS to zero and returns MCK to the inactive high state. If MCK occurs slightly earlier than MS then there will be a glitch pulse from the AND of MS and MCK and a garbage data bit will be read. As this is a situation of two digital signals changing simultaneously then unpredictable behavior is to be expected.

To fix this a 3nsec delay was added to MCK with an SDI select in the SPARES field called MCK_SEL. This fixes the issue by insuring that MS falls before MCK rises so there will be no glitch. But this could be dangerous if the PC board layout adds delay to MS relative to MCK. The added delay could not be greatly increased as the maximum tolerance delay would then cause an issue with the last valid data bit.

Case 1: GMSK Clocking Signals Generated by Baseband, TXD_MODE=1, TXF=00

Transmission is initiated by setting the TXST or TXEN pins to a logical high. The baseband will generate a 13/48MHz clock that is applied to MCK. If SDI bit TXCKINV is low, then on every rising edge of MCK the baseband will assert an NRZ data bit on MDI. The RF6001 will read this data on every falling edge of MCK if TXCKINV is set. If TXCKINV is set high, the baseband will assert an NRZ data bit on the falling edge of MCK and the RF6001 will read this data bit on every rising edge of MCK. The diagram below summarizes the operation of this interface.

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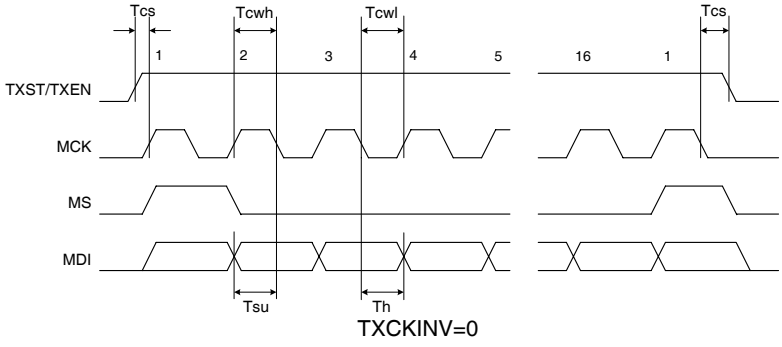
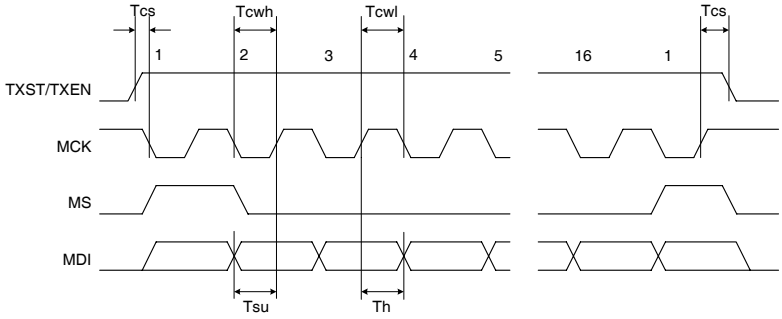
Case 2: GMSK Clocking Signals Generated by RF6001, TXD_MODE=0, TXF=00

Transmission is initiated by setting the TXST or TXEN pins to a logical high. The RF6001 will then respond by outputting a 13/48MHz clock on MCK and a pulse on MS on every 16th MCK period. The baseband IC will respond with an NRZ data bit on MDI at every rising edge of MCK if SDI bit TXCKINV is low. The RF6001 will read this data on every falling edge of MCK if TXCKINV is set low. If TXCKINV is set high, the baseband will assert an NRZ data bit on the falling edge of MCK and the RF6001 will read this data bit on every rising edge of MCK. MS serves to synchronize the baseband IC by providing a new word pulse to refresh the output register of the baseband IC. The diagram below summarizes the operation of this interface.



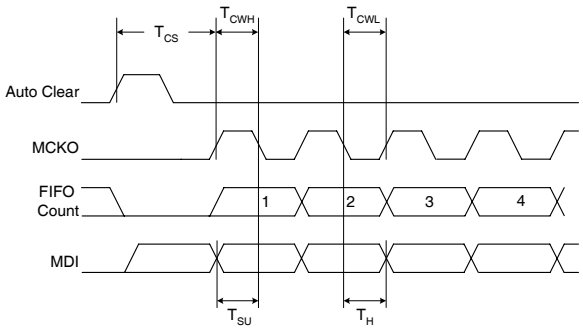
TXCKINV=0



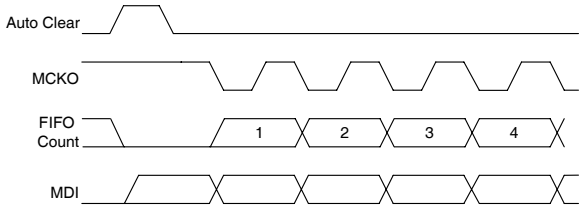
TXCKINV=1

Case 3: GMSK FIFO Clocking Signals Generated by Baseband, TXD_MODE=1, TXF=01
The FIFO will automatically clear under three conditions: 1) if the SDI reset field is programmed; 2) at the end of any transmission burst following the end of the ramp down; and, 3) if the SDI field FCLR is set. This will clear the contents of the FIFO memory and designate the next bit written as the first output bit of the FIFO. The baseband will then generate a clock of less than or equal to 26MHz applied to MCK. On every rising edge of MCK, the baseband will assert an NRZ data bit on MDI if TXCKINV is low. The RF6001 will read this data on every falling edge of MCK if TXCKINV is set low. If TXCKINV is set high, the baseband will assert an NRZ data bit on the falling edge of MCK and the RF6001 will read this data if MS is high on every rising edge of MCK. This data will be stored in a First In First Out (FIFO) register of length 1024 bits in the RF6001. The diagram below summarizes this part of the interface.

Transmission is initiated by setting the TXST or TXEN pins to a logical high. If TX_ST is set high, an internal timer (TXENU) is programmed to delay the rise of TX_EN. A second timer (MD_DLY) determines then the modulation stored in the FIFO will begin to be output relative to the rising edge of TX_ST. Data will be output at a 13MHz/48 rate. New data CAN be loaded into the FIFO input while the output is active. The second diagram below summarizes the operation of the second step of this interface.



TXCKINV=0, TXF=01



TXCKINV=1, TXF=01

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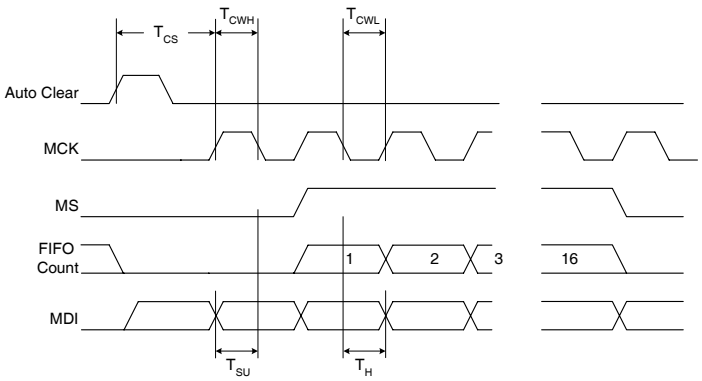
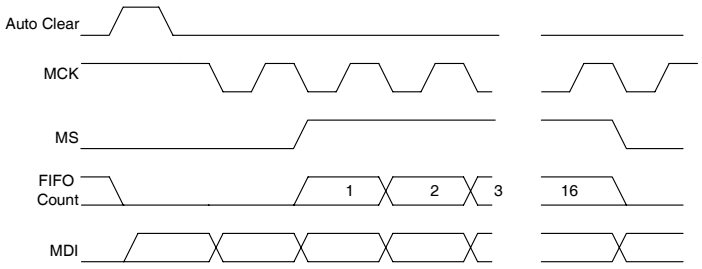
Case 4: GMSK FIFO Clocking Signals Generated by Baseband, TXD_MODE=1, TXF=10
The FIFO will automatically clear under three conditions: 1) if the SDI reset field is programmed; 2) at the end of any transmission burst following the end of the ramp down; and, 3) if the SDI field FCLR is set. This will clear the contents of the FIFO memory and designate the next bit written as the first output bit of the FIFO. The baseband will then generate a clock of less than or equal to 26MHz applied to MCK. On every rising edge of MCK, the baseband will assert an NRZ data bit on MDI if TXCKINV is low. The RF6001 will read this data if MS is high on every falling edge of MCK if TXCKINV is set low. If TXCKINV is set high then the baseband will assert an NRZ data bit on the falling edge of MCK and the RF6001 will read this data bit if MS is high on every rising edge of MCK. This data will be stored in a FIFO register of length 1024 bits in the RF6001. The diagram below summarizes this part of the interface. This is the same as Case 5 except that the data is framed by MS.

Transmission is initiated by setting the TXST or TXEN pins to a logical high. If TX_ST is set high then an internal timer, TXENU, is programmed to delay the rise of TX_EN. A second timer, MD_DLY, determines when the modulation stored in the FIFO will begin to be output relative to the rising edge of TX_ST. Data will be output at a 13MHz/48 rate. New data CAN be loaded into the FIFO input while the output is active. The second diagram below summarizes the operation of the second step of this interface.



TXCKINV=0, TXF=10



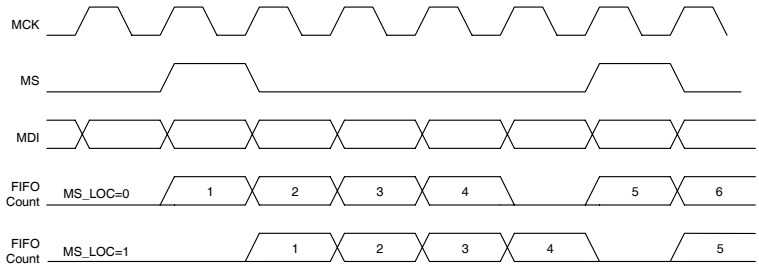
TXCKINV=1, TXF=10

Case 5: GMSK FIFO Clocking Signals Generated by Baseband, TXD_MODE=1, TXF=11
In this FIFO mode, the baseband will generate a pulse equal to one clock period on the MS line to signify the beginning of a FIFO data transfer. If the SDI bit MS_LOC is programmed low then the transfer of the first data bit will occur on the same clock period as the pulse on MS. With MS_LOC low there does not have to be any idle clock pulses between transfer intervals. If MS_LOC is high then the transfer of the first data bit will occur on the next clock period after the pulse on MS. With MS_LOC high there must be at least one idle clock pulse between the end of the last transfer interval and the beginning of the next.

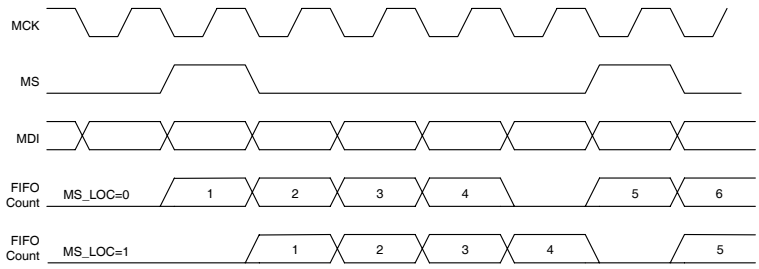
The baseband will then generate a clock of less than or equal to 26MHz applied to MCK. On every rising edge of MCK, the baseband will assert an NRZ data bit on MDI if TXCKINV is low. The RF6001 will read this data on every falling edge of MCK if TXCKINV is set low. If TXCKINV is set high then the baseband will assert an NRZ data bit on MDI on every falling edge of MCK and the RF6001 will read the data bit on every rising edge of MCK. This data will be stored in a FIFO register of length 1024 bits in the RF6001.

Data will continue to be read in until the number of bits read becomes equal to the setting of the SDI word MS_LEN. MS_LEN can be set to 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 16, 24, 32, or 48 bits. Once this occurs, no further data will be read until another pulse is applied to MS to start the process over.

The diagram below summarizes this mode of the interface.



TXCKINV=0, MS_LEN=4, TXF=11



TXCKINV=1, MS_LEN=4, TXF=11

Transmission is initiated by setting the TXST or TXEN pins to a logical high. If TX_ST is set high then an internal timer, TXENU, is programmed to delay the rise of TX_EN. A second timer, MD_DLY, determines when the modulation stored in the FIFO will begin to be output relative to the rising edge of TX_ST. Data will be output at a 13MHz/48 rate. New data CAN be loaded into the FIFO input while the output is active. The diagram below summarizes the operation of the second step of this interface.

Note that there are NOT TXD_MODE=0 cases for the FIFO system (i.e., the baseband is always the master of FIFO data transfers.)

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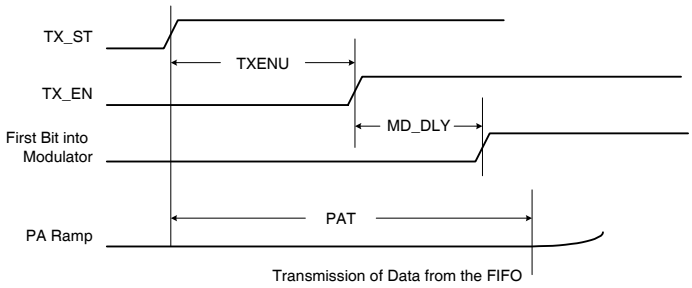


Analog I/Q Mode
Programming the TXAD bit low puts the GMSK modulation interface in analog mode.

In this mode, programmable comparators are used to determine the symbols contained in the I and Q baseband waveforms at each symbol time.

The positive and negative thresholds used for the differential I and Q channel comparison are set by SDI bits TX_THP[3:0] and TX_THN[3:0] according to the following formulae.

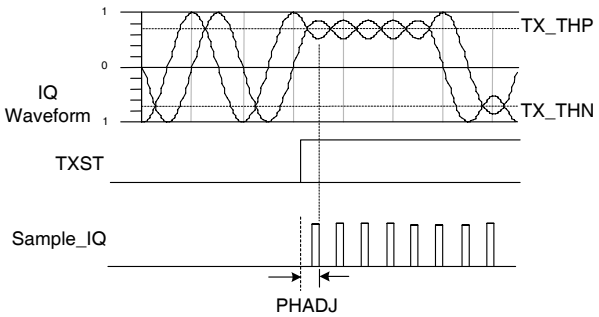
Vth (positive)=0.05*(TX_THP+2) where TX_THP is the value between 0 and 15 that is programmed into that register.
Vth (negative)=-0.05*(TX_THN+2) where TX_THN is the value between 0 and 15 that is programmed into that register.

Each threshold should be set as close as possible to 0.625 times the peak differential I or Q voltage.

The following table indicates the appropriate threshold SDI settings for a given peak voltage of modulation waveform from the baseband.

V_{PK} from Baseband (V)	Vth (V)	Recommended Programming Value	
		TH_THP[3:0]	TH_THN[3:0]
0.16	0.10	0	0
0.24	0.15	1	1
0.32	0.20	2	2
0.40	0.25	3	3
0.48	0.30	4	4
0.56	0.35	5	5
0.64	0.40	6	6
0.72	0.45	7	7
0.80	0.50	8	8
0.88	0.55	9	9
0.96	0.60	10	10
1.04	0.65	11	11
1.12	0.70	12	12
1.20	0.75	13	13
1.28	0.80	14	14
1.36	0.85	15	15

The phase of the symbol clock used to make I and Q threshold decisions will need to be set so that I/Q sampling occurs at the maximum eye opening. Ideally, the time measured from the maximum eye opening to the rising edge of TX_ST will be an integer multiple of 3.69µs. This will assure that the RF6001 is sampling at the instance of maximum eye opening. If this time is not an integer multiple of 3.69µs, the PHADJ(5:0) bits will need to be set according to the following procedure. Enable the Sample_IQ pulse used by the analog interface to sample the I/Q waveforms with the following SDI settings, TSEL(1:0)=01 and TMUX(2:0)=010. This pulse will be output on the LDT0 pin of the RF6001. Program the PHADJ(5:0) bits to align the falling edge of this pulse with the maximum eye opening as shown in the diagram below:



PHADJ(5:0) is adjustable from 0 to 63 (6-bit number) representing phase offsets from 0µs up to 4.846µs in approximately 77ns steps. As with the threshold settings, this phase will be specific to a radio platform and needs to be determined by the user.

Also note that in TX mode DAGC will affect the analog amplitude of the 8PSK signal. DAGC is expected to be set to 03h (for 0dB gain) and should be programmed as such prior to a TX burst accordingly.

Detailed Ramp-Up

The above development demonstrated the overall PA control methodology. Depending on the mode used within the RF6001 the detailed PA control methodology will now be developed.

Several SDI parameters must be properly set to properly time the ramp up. These parameters are as defined as follows:

G_DEF (GMSK default)

G_DEF will be the input value to the GMSK modulator when the modulator data input is not active.

G_CNT (garbage count)

The purpose of this SDI field is to allow the baseband to transmit a programmable number of undefined bits at the beginning of each transmission. There are four possible modes of operation of this field depending on how the data is loaded into the RF6001.

1. FIFO mode=00 When using FIFO mode 00 the FIFO is not active and the serial mode is active. If UAM is true then G_CNT will begin when TX_ST rises between two GPRS bursts. The RF6001 will continue to fill data from G_DEF until G_CNT expires. MS will rise on the last rising edge of MCK before G_CNT expires. Thus the last MCK during G_CNT is used to load data in the baseband register (if MS is used).
   If UAM is false then G_CNT will begin when MD_DLY2 expires in a transition between two GPRS bursts.
   G_CNT is not used on the first burst. The first 16 MCK's after MD_DLY1 expires on the first burst ramp up will always be ignored and data will fill from G_DEF.
2. FIFO mode =01 When using FIFO mode 01 this field has NO EFFECT. (This is because we would have no way of knowing when the next group of FIFO bits begins loading.)
3. FIFO mode=10 When using FIFO mode 10 the IC will ignore the first G_CNT data bits occurring on the first G_CNT MCK cycles after MS rises. This affects only the FIFO loading and has no effect in FIFO read during actual transmission.
4. FIFO mode=11 When using FIFO mode 11 this field has NO EFFECT.

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G_DLY (GMSK delay)
This field will increase the latency of the GMSK modulator in 1/16 symbol increments. The modulator delay can be adjusted from 12.2 qst to 19.95 qst.

G_DLY will hold the GMSK modulator in reset until G_DLY expires. The data flow to the modulator is also delayed by the same amount. This will add latency to the GMSK modulator. During the reset time the data held in the GMSK modulator shift register is frozen and the output of the modulator is frozen. When G_DLY expires then the shift register loads the new data bit that was present at the start of G_DLY. The shift register and modulator output are then released.

The G_DLY operation is performed on the occurrence of the first valid data bit of each time slot in a GPRS transmission if EALGN is true.

If EALGN is false then the G_DLY operation is performed only at the first valid data bit of the first timeslot.

EALGN
The purpose of this bit is to realign the GMSK data flow to the trigger signal if the trigger signal is not on the symbol clock raster defined by the first rising edge of TX_ST.

If all timing is aligned to the symbol raster then EALGN can be set to zero and timing advances based on the initial rising edge of TX_ST. In this case the guard time between GPRS bursts will be an integer multiple of symbol times. This represents a timing slip of ¼ symbol from the ETSI requirement.

If this bit is true then the data clocks used for GMSK are reset on the first valid data bit of each timeslot. In FIFO mode the first valid data bit occurs when MD_DLY1 or MD_DLY2 time out. In serial mode the first valid data bit occurs on the first falling MCK edge after MD_DLY1 or MD_DLY2 expire. (G_CNT is ignored) If UAM is true then MD_DLY2 is not used and the trigger point is then the rise of TX_ST or MD_DLY1 expiring.

When the clocks reset then a phase glitch will occur. In GMSK mode the glitch will be at the modulator output at the end of the G_DLY interval. This is because GMSK uses a lookup table system and thus resetting the clock glitches the output as soon as the G_DLY parameter releases the output.

UMS (use MS)
If this bit is set high then the first 16 MCK data bits loaded after MD_DLY1 expires in serial mode will be filled with G_DEF as opposed to loading data from the FIFO or serial interface. This is used in serial mode with MS as the system needs to know to fill the first 16 bits with the default as the first MS is blanked. The 16 bits occur ONLY on the first burst of a GPRS transmission.

MD_DLY1 (Modulation Delay 1)
This field sets the delay from the rising edge of TX_ST to the beginning of the modulation.

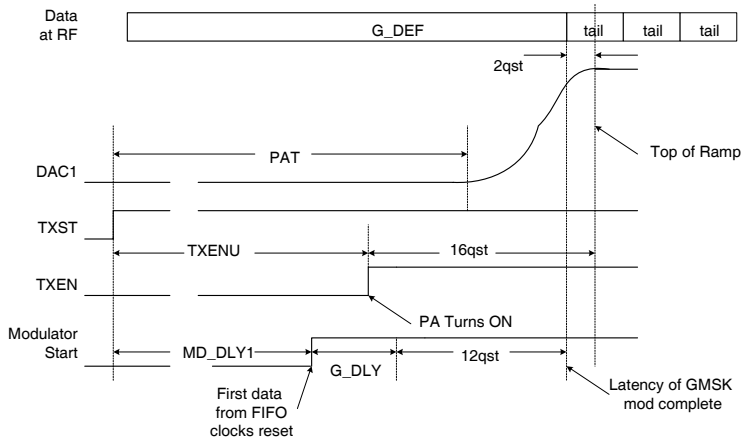
Counter resolution will be 1/8 symbol time to allow the user to fine tune for the modulator latency. When TX_ST rises the modulators become active and receive data from the internal default data fields called G_DEF. When MD_DLY expires the GMSK modulator shifts from the default value to the input data stream.

If FIFO modes are used then the data flow from the FIFO begins when MD_DLY1 expires.

In serial mode if MS is active then the first MS after MD_DLY1 expires is blanked. Thus there are always 16 MCK pulses before the first rising MS. These first 16 pulses use the internal RF6001 default values. In serial mode, MD_DLY1 only functions if MCK is supplied by the RF6001.

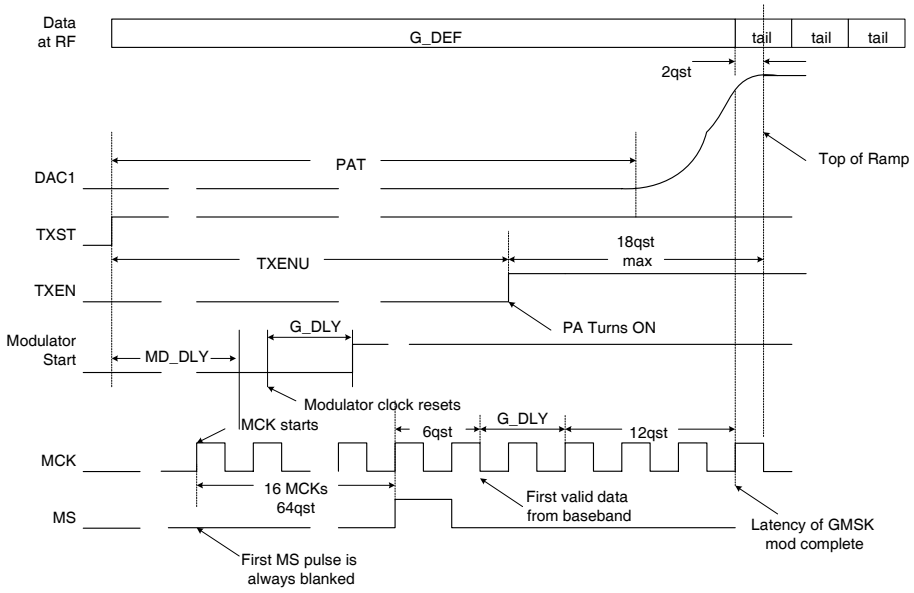
GMSK Ramp-Up

The diagram below presents the ramp up for GMSK in the FIFO mode of operation. The latency is the sum of G_DLY and the basic GMSK latency of 12qst. The sum of the two is 18qst and is selected to match the 8PSK latency in this example. Any glitch will occur when the clock resets at the end of G_DLY and thus is at a low power level. This allows G_DEF to be used for the guard bits if desired. (Note that 8qst ramps have been used for these examples; 13qst or 16qst ramps could be used equally well.)



FIFO GMSK Start-up Mode, EALGN=1

If data is loaded with the serial mode system using MS, then the diagram below presents the operation of the system.



Serial GMSK Mode using MS, MCK and MS are Output from RF6001, EALGN=1

TX_EN is set to occur 18qst before the top of the ramp so as to not violate the ETSI time mask at the -30dBc point. MD_DLY1 is set to start the modulator 66qst plus G_DLY before TX_EN so that the first valid data symbol is the first tail symbol. G_CNT will have to be set to one in this case so that the initial state of the differential encoder is set at the correct time. If the baseband differential encoding is used then G_CNT does not matter.

Note that the user could also send the guard symbols if MD_DLY1 is further advanced.

Since the new data flow starts well in advance of the burst, then there should be no issue with phase transitions if the delay from the rise of TX_ST to the end of MD_DLY1 is not an integer number of symbol times. Any such transition will occur at minimum output power levels if MD_DLY1 is advanced far enough.

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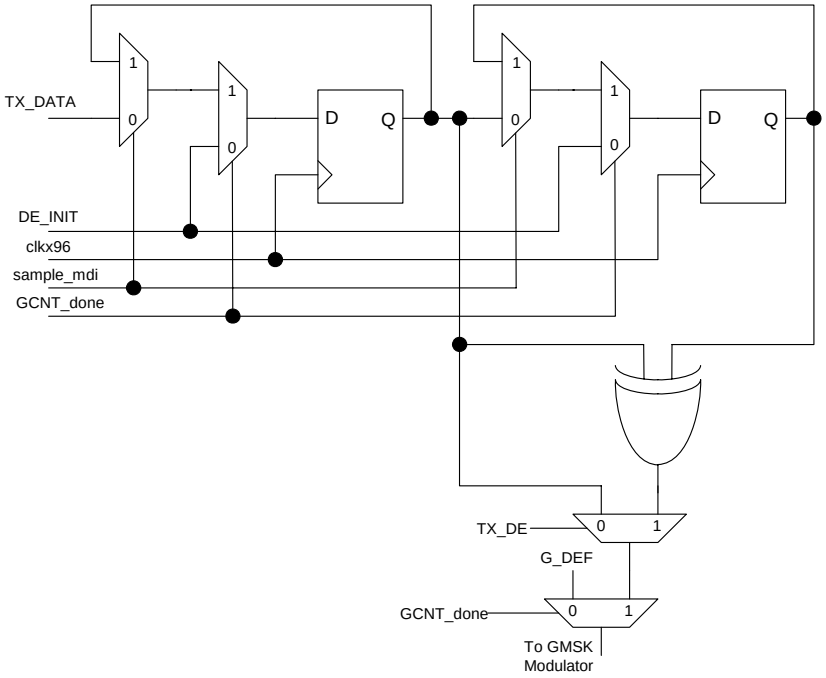
Controlling Initial Data Flow

The RF6001 can be configured to control the dummy bits and guard bits that occur before the tail bits of the burst. The RF6001 can also be configured to allow the user to control these bits instead.

The block diagram shown below is a useful representation of how the data flow works within the RF6001 for this functionality. The actual system has other control modes but for the purposes of this discussion only this part is shown.



TX_DATA is the data flow from the FIFO or the serial interface

DE_INIT is the initial state of the differential encoder system set from SDI.

Clkx96 is the 26MHz system clock.

sample_mdi is the internal trigger signal that reads TX_DATA

GCNT_done is an internal trigger signal that signifies that the “garbage count” is completed.

TX_DE selects internal differential encoding or not.

G_DEF is the default states of the modulator when not selected for active data.

MD_DLY1 triggers when active data is released to the modulators.

Control of guard bits using RF6001 in GMSK

In GMSK mode ETSI specifies that the guard bits are all ones and the tail bits are all zeroes. This results in a differentially encoded output of 000000100ddddd. Where “d” represents the data bits.

If TX_DE is low then differential encoding is done in baseband. In this case DE_INIT is held at zero and G_DEF is held at zero. The output to the GMSK modulator will be zero until MD_DLY1 expires. Once MD_DLY1 expires then TXDATA will port to the GMSK modulator with differential encoding as defined by baseband. Thus MD_DLY1 timing is set to switch over at the first tail bit.

If TX_DE is high then the differential encoding is done within the RF6001. In this case DE_INIT is held at one and G_DEF is held at zero. The output of the internal differential encoder will then be zero for the guard bits and the internal state of the differential encoder will be held at one during this time. When MD_DLY1 expires then the input to the differential encoder will receive a zero for the first tail bit. This will encode with the internal state of one to an output of one at the differential encoder. Subsequent tail bits of zero will differentially encode with the previous state and result in zero. MD_DLY1 will be timed to expire at the first tail bit.

Note that when MD_DLY1 expires then this triggers GCNT to begin and all transitions actually occur when GCNT is done. If all bits are valid then GCNT is zero and GCNT_done is the same as MD_DLY1 expiring.

Also note that GCNT works on the output data flow only in serial input mode. In FIFO mode GCNT works as the FIFO is loaded but not when the FIFO is read. Thus GCNT is effectively zero in FIFO mode for data output.

Control of guard bits using Baseband in GMSK

This is a fairly trivial case. MD_DLY1 is set to expire some time before the ramp up interval. The baseband sends data and by the time the transition from guard bits to tail bits occurs the differential encoder has been initialized long ago.

Detailed GPRS Burst Transition Operation

In a GPRS transmission multiple timeslots can be transmitted.

Several SDI parameters must be properly set to properly time the transitions. These parameters are as defined as follows: (All of the previously defined parameters from the ramp up section still apply.)

MD_DLY2 (Modulation Delay 2)

In a GPRS transmission, when TX_ST falls at the end of the present TX timeslot, the data from the FIFO stops and the value of G_DEF is used till MD_DLY2 expires. MD_DLY2 begins counting at the end of the present data bit being sent when TX_ST falls.

If UAM is true then MD_DLY2 begins counting at the next rising edge of TX_ST. Data will continue to be taken from GDEF until MD_DLY2 expires and then will switch to the FIFO or the serial interface.

UAM (use Alternate Mode)

The RF6001 has two modes of transitioning between GPRS timeslots. This first mode uses MD_DLY2 to trigger the data flow and TX_ST edges to start the ramps. This is referred to as the “normal” mode. If UAM is set high then the “alternate” mode of operation is activated. In this mode TX_ST triggers the data flow. Ramp up and ramp down are then controlled by two timers triggered from TX_ST as described below.

RD_DLY (Ramp Down Delay)

RD_DLY is a 5-bit field that will determine the start of the ramp down relative to the falling edge of TX_ST in quarter symbol times (qst). This is only used if UAM is true.

RU_DLY (Ramp Up Delay)

RU_DLY is a 5-bit field that will determine the start of the ramp up relative to the rising edge of TX_ST in qsts. This is only used if UAM is true.

In order to properly align the data upon making a transition between modes, the rising edge of TX_ST must be aligned to the data stream.

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GMSK to GMSK Transitions

GMSK to GMSK EALGN=1 "Normal" FIFO Mode

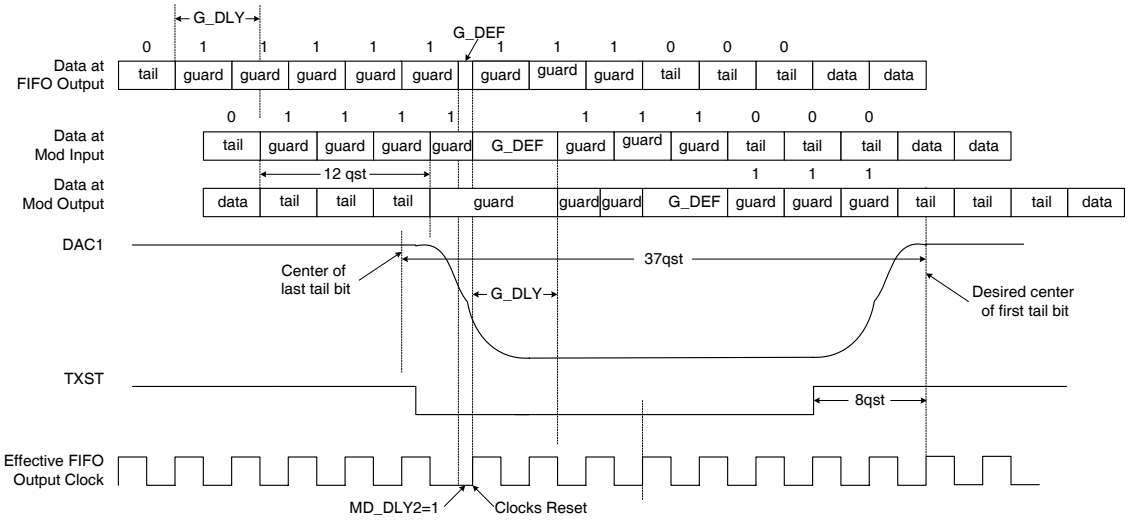
This is the transition mode between two GMSK bursts in "normal" mode with EALGN set to one. Any "garbage" bits are blanked during the FIFO loading process and have no effect during the transmit time.

The rules for MD_DLY2 with UAM=0 are as follows:

1. MD_DLY2 begins counting at the end of the current symbol after TX_ST falls on the first burst.
2. While MD_DLY2 is active, data is held in the FIFO and the serial interface stops. When MD_DLY2 expires the next bit is released from the FIFO and the effective FIFO output clock has a rising edge. In serial mode MCK has a rising edge on the last G_CNT after MD_DLY2 expires.
3. During the time MD_DLY2 is active the data at the output of the FIFO or serial input is multiplexed to the SDI bit called G_DEF.
4. If MD_DLY2 is set to zero then MD_DLY2 is disabled.
5. When MD_DLY2 expires then G_CNT begins. (serial only)
6. On the last count of G_CNT, MS pulses. (serial only)
7. If MD_DLY2 is set to zero then G_CNT is ignored and MS will NOT pulse until the next normally occurring 16MCK boundary. (serial only)

If UAM=1 then the rules change as follows:

1. MD_DLY2 begins counting after TX_ST rises on the next burst.



In this example, the rising edge of TX_ST is aligned to be 8qst before the center of the first tail symbol. The modulator uses data loaded from the FIFO. MD_DLY2 is set to one to cause a 1qst shift in the transition width and thus exactly meet the ETSI 8.25 symbol guard time.

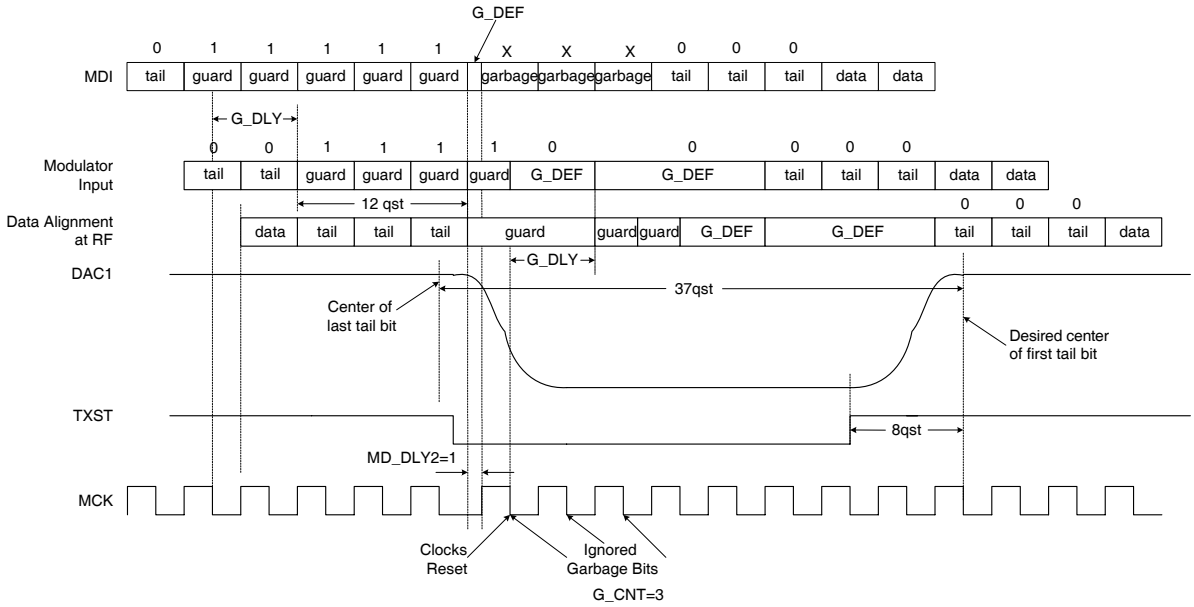
Once MD_DLY2 expires, the G_DLY is set to 6qst. During the 6qst of G_DLY the data at the modulator input is replaced by G_DEF. The output of the modulator is held at the guard value. At the end of G_DLY, the tail bit data present at the beginning of G_DLY is fed to the modulator.

The quarter-symbol shift will cause a phase transition to occur at the start of G_DLY. This transition will occur during the ramp down region and could be a problem. If the previous 4 symbol times are all 1, as shown in the diagram above, then the modulation is "pinned" to maximum deviation and there will be no glitch when the clocks reset. Also note that this transition does not exist for EALGN=0 and G_DLY=0.

In GMSK mode, there is a latency of approximately 12qst (12.2qst, actually) from the center of a data symbol entering the modulator to the maximum RF effect of the symbol. Thus DAC1 is aligned with the "Data at output" field and is 12qst delayed from the data at the input of the GMSK modulator. The data at the input of the modulator is delayed by 6qst from the data at the FIFO output by G_DLY. Thus the total delay is 18qst and matches the 8PSK delay.

Note that none of the tail bits are punctured.

GMSK to GMSK, EALGN=1, "Normal" Serial Mode
If the serial mode interface is used instead of the FIFO then the diagram below presents the transition. MD_DLY2 is active in serial mode as well as FIFO mode. The rules for MD_DLY2 are as follows:



Data changes at MDI on the rising edges of MCK and is read on the falling edges of MCK. In this example G_DLY is set to 6qst so the Modulator input is delayed a net of 8 qst from the data at MDI.

In this diagram G_CNT is set to three to blank the first three serial bits from the baseband system. MD_DLY2 is set to 1 to exactly meet the ETSI 8.25 symbol guard time. G_DEF fills the three garbage symbols and the 1 qst from MD_DLY2.

There will be a phase glitch at the start of G_DLY due to the quarter bit shift. This will occur during the ramp down. As in the last case this should not be a problem if the previous four symbols are all 1s or 0s.

Note that the falling edge of TX_ST is delayed 1qst. This is not a timing mask issue as there is no timing mask between GPRS bursts other than the maximum power level.

If the serial mode interface is used with MS then the only difference is that MS will pulse on the last G_CNT count.

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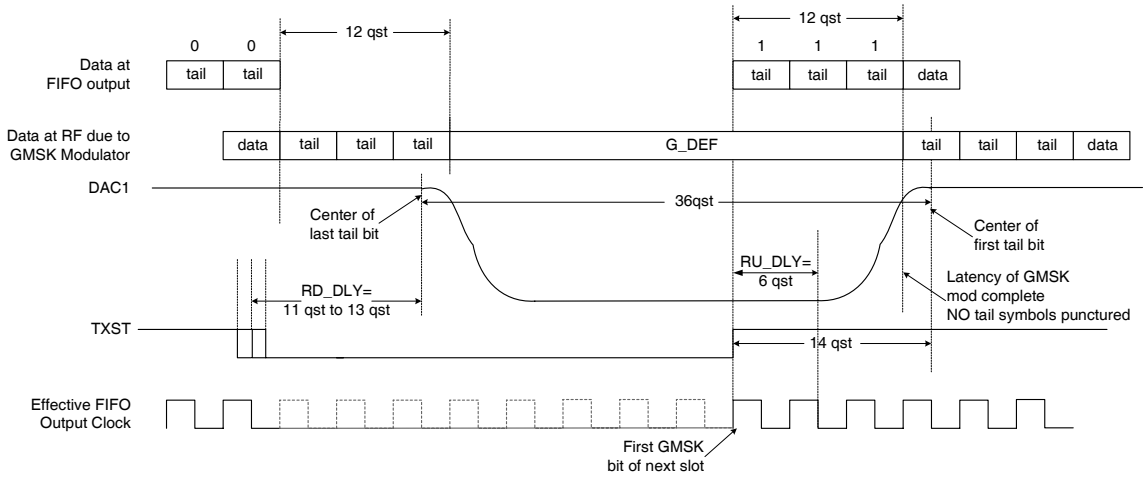
GMSK to GMSK EALGN=0, "Alternate" FIFO Mode
The diagram below presents the transition between two GMSK timeslots in alternate mode.



The falling edge of TX_ST can be located in one of three positions to turn off the data after the last tail symbol of the first burst. RD_DLY is adjusted depending on the qst chosen. The rising edge of TX_ST is aligned to be 14qst before the center of the first tail symbol of the second burst so that the effective FIFO clock starts at the correct time to align the first tail symbol to the desired time.

In GMSK mode there is a latency of approximately 12qst (12.2qst actually) from the center of a data symbol entering the modulator to the maximum RF effect of the symbol. Thus DAC1 is aligned with the "Data at output" field and is 12qst delayed from the data at the output of the FIFO.

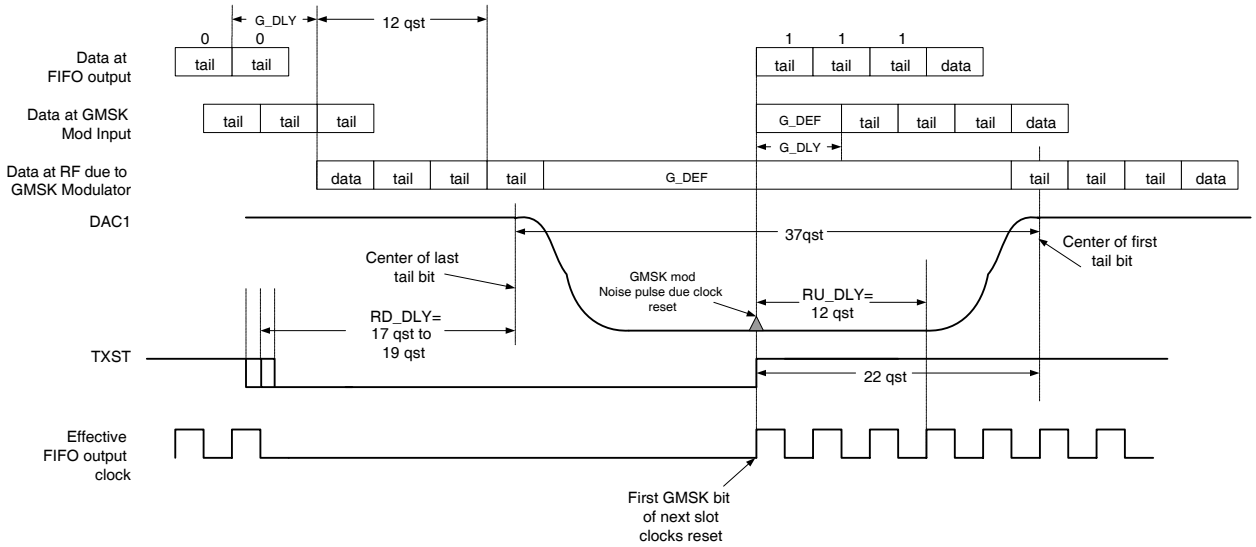
Note that none of the tail bits are punctured.

In this method of operation (EALGN=0) the rising edge of TX_ST for the second and later bursts must be an integer number of symbol times relative to the first rising edge of TX_ST. The timing is aligned with the first rising edge of TX_ST and will not change if subsequent TX_ST transitions are aligned to this raster. (Since G_DLY is not zero then if TXST moves off the raster the system would realign the clocks as if EALGN=1.)

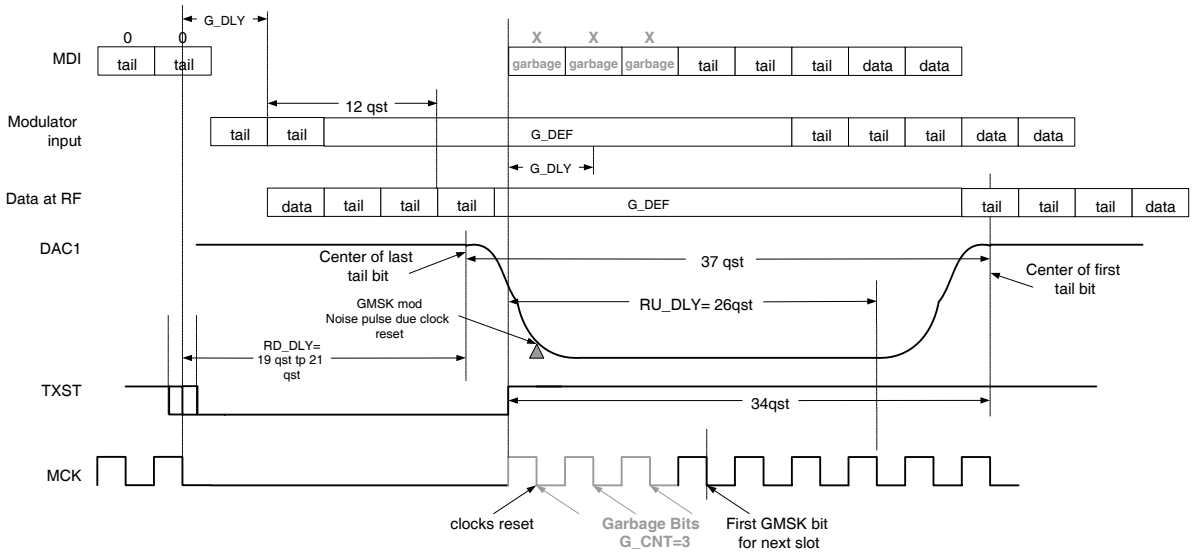
This means that the guard time will be an integer number of symbols and will ignore the quarter symbol shift specified by ETSI. There will be no glitch in this mode.

GMSK to GMSK EALGN=1, "Alternate" FIFO Mode
The quarter symbol shift CAN be accounted for by setting EALGN to 1. The diagram below presents this situation.

As before there will be a glitch at the rising edge of TX_ST due to the clock reset function causing a phase discontinuity. This occurs during minimum output power and should not be a problem.



GMSK to GMSK EALGN=1, "Alternate" Serial Mode
If the serial mode interface is used instead if the FIFO then the diagram below presents the transition.



Data changes at MDI on the rising edges of MCK and is read on the falling edges of MCK.

In this diagram G_CNT is set to three to blank the first three serial bits from the baseband system. G_DEF fills the three garbage symbols.

If the serial mode interface is used with MS then the only difference is that MS will pulse on the last G_CNT count.

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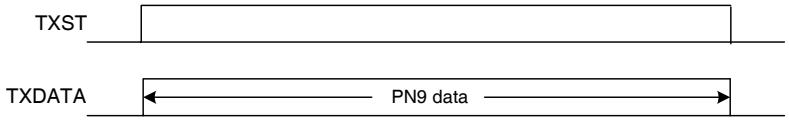
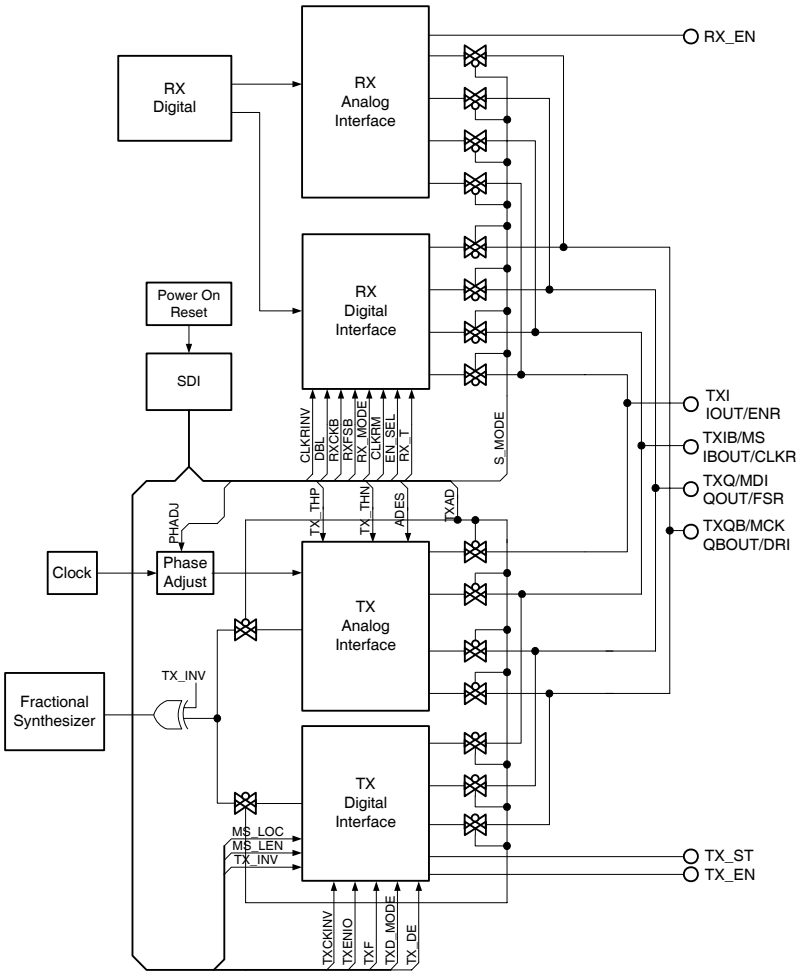
Transmit Test Mode

There is a test mode in the RF6001 to assist in transmitter testing. This mode is invoked by setting SDI bit TXTEST=1. Pseudo-random data based on a PN9 sequence is used as the data source to the GMSK modulator. The data sequence is initiated by a rising edge on TXST and ends on the falling edge of TXST. The Transmit Turn-On Sequence defined in an earlier section should be followed to allow proper VCO warm-up and PA ramping to take place when using this test mode. This test mode is shown in the diagram below:



Multiplexed RX and TX Busses

The RF6001 RX interface can be connected to the TX interface to result in a single interface to baseband as shown in the diagram below.



Regardless of the TX mode chosen the TX signals are all inputs and will not conflict with the RX signals. The RX outputs must be set to analog mode by programming S_MODE low and holding RX_EN low during transmit times. This is to avoid a conflict between the idle ground states of the digital RX outputs and the external TXI and Q signals.

Synthesizer Information

Fractional-N Synthesizer

The RF6001 contains a charge-pump based, fractional-N phase locked loop (PLL) for controlling the receive VCO's on the RF2722 and the transmit VCO's on the RF6001. The PLL includes integrated loop filters and automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable locktime and noise performance. The PLL is intended to use a 26MHz reference frequency signal for operation within GSM Cellular Radio systems, but may be programmed to use lower frequency reference signals if desired; however, noise performance will degrade if a lower reference frequency is used.

Enabling the PLL

The PLL can be enabled by the TXST, TXEN, or RXEN signals in addition to the PLLEN(1:0) bits. This allows automatic timing of the complete Polaris chipset warm-up from a single pin in either TX or RX mode.

The PLL interfaces to both the integrated VCO's on the RF6001 or can interface to an external VCO via the FIN and VT pins. The VT_EN and VCOSEL bits determine the mode of operation. When VT_EN is set to 0, the internal loop filter is disconnected from the VT pin. When VCOSEL(1:0) is set to 00, an external VCO can be used with the input through FIN. With VT_EN set to 1, the internal loop filters are connected and the internal VCO is selected using the VCOSEL(1:0). With VCOSEL(1:0)=10, the integrated VCO1 is active; with the VCOSEL(1:0)=11, the integrated VCO2 is active.

PLL Configuration

The RF6001 PLL provides options for use of internal and external VCO's, internal or external loop filter, automatic calibrations, etc. These settings require three 18-bit registers (54-bits). In order to provide rapid switching between operating modes, the serial interface provides four groups of 'PLL Preset' registers. Each group contains three registers. The active PLL Preset register group is determined by the PLLSEL(1:0) bits, as shown in the following table.

PLLSEL(1:0)	Active PLL Preset Register Group
00	PLL0x (PLL00, PLL01, PLL02)
01	PLL1x (PLL10, PLL11, PLL12)
10	PLL2x (PLL20, PLL21, PLL22)
11	PLL3x (PLL30, PLL31, PLL32)

The PLL Preset registers share the addresses 000101, 000110 and 000111. For example, if PLLSEL(1:0)=00, then the PLL0x group is active, and address 000101 writes to PLL00, address 000110 writes to PLL01, address 000111 writes to PLL02, and the PLL will use the settings in PLL00, PLL01 and PLL02.

If PLLSEL(1:0)=10, then the PLL2x group is active, these addresses write to PLL20, PLL21, PLL22, and the PLL will use the settings in these registers.

Loop Filters

The PLL contains loop filters optimized for the VCO's it controls. The resistor and capacitor values of the loop filters (and the DAC filters) are calibrated by an RC Calibration System that runs for up to 20μs when the PLLs or DACs are enabled. The RC_EN bit in the CAL register determines whether the RC calibration system runs. It is recommended that the RC_EN bit be set to true (1) always, to allow the system to run each time the PLL or DACs are enabled, to accommodate environmental variations. The PLL loop filter can be bypassed such that the VT pin will then be directly connected to the output of the PLL charge pump, using the VT_EN and LPF serial interface bits. In this manner, the PLL can be used with an external VCO and external loop filter.

Charge Pump Currents

The PLL employs a deadzone-free phase detector for fast, low-jitter locking performance. The base current in the charge pump can be selected using the CPI(0)bit. With CPI(0) set to 0, the charge pump is in a low current setting for use in receive mode with the RF2722. With CPI(0) set to 1, the charge pump is in a higher current setting for transmit mode with internal VCO's.

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Tuning Gain Calibration
PLL employs a tuning gain calibration algorithm to compensate for tuning gain variations in the integrated VCO's. This system eliminates loop gain and bandwidth variations across the VCO tuning range, ensuring that the GSM spectral mask is met. It is recommended to set the KV_EN bit to true (1) to allow the system to calibrate. Calibration takes approximately 20μs after the loop has attained lock.

Lock Detection
The PLL contains a lock detect circuit which can be routed to the "lock-detect/test output" LDTO pin via the test multiplexer. This circuit provides a rough indication of whether the PLL is operating properly. The LDTO pin voltage will move from ground to VDD when the loop is close to lock for several cycles of the loop reference frequency. The LDTO pin voltage will return to ground if the PLL is out of lock. This signal can be monitored in transmit mode to shut down the transmitter if the PLL/VCO system fails.

Frequency Control
The fractional-N PLL provides very fine frequency resolution capability, requiring a total of 36 bits to set the frequency. In most cellular systems it is acceptable to have much coarser frequency control. Fine frequency control can be separated into an AFC (automatic frequency control) register.

The frequency of the PLL/VCO is primarily determined by two registers: the offset register, OFFS(17:0); and, the AFC register, AFC(17:0). The OFFS register value programs the VCO frequency in multiples of 5kHz. With 18 bits, this gives a range of 2^18*5kHz=1.31GHz.

In order to cover all cellular bands, a base frequency is used, determined by the FBASE(1:0) bits, as shown in the following table.

FBASE(1:0)	F_{BASE}	Frequency Range	Comment (Freq. Band)
00	0Hz	0 to 1310.72MHz	GSM/US Cellular
01	832MHz	832MHz to 2142.72MHz	DCS/PCS
10	1664MHz	1664MHz to 2974.72MHz	DCS/PCS/W-CDMA
11	1664MHz	1664MHz to 2974.72MHz	DCS/PCS/W-CDMA

The equation for the PLL/VCO frequency is:

$$F_{VCO} = F_{BASE} + OFFS \times 5kHz + AFCD \times \left(\frac{26MHz}{2^{24}}\right)$$

The change in frequency versus the AFCD is as follows:

$$\Delta F = AFCD \cdot \frac{F_{REFERENCE}}{2^{24}}$$

$$AFCD = \frac{2^{24}}{F_{REFERENCE}} \cdot \Delta F$$

Each step on AFCD will change the TX frequency (both bands) by

$$\frac{26MHz}{2^{24}} \approx 1.55Hz$$

In high band RX mode, the LO frequency will change by the same amount.
In low band RX mode, the LO frequency will change by

$$\frac{1}{2} \cdot \frac{26MHz}{2^{24}} \approx 0.775Hz$$

Note that the relationship between frequency error and AFCD is reversed (negative) with high side injection receive mode. The AFC register will provide fine tuning over a ±203kHz range for both TX bands and high band RX. For low band RX, the AFC register will provide fine tuning over a ±101.5kHz tuning range.

AFCD(17:0) is an 18-bit twos complement signed value.

000000000000000000 to 011111111111111111 = 0 (0Hz) to 131071 (203.16005kHz) @ 1.55Hz resolution.

111111111111111111 to 100000000000000001 = -1 (-1.55Hz) to -13071 (-203.16005kHz) @ 1.55Hz resolution.

The host/DSP could decide to use the GSM channel number to generate the OFFS value. The base frequency in the RF6001 is different than that used by the ETSI standard so an offset needs to be added, and the channel number needs to be multiplied by 40 to obtain the proper multiple of 5kHz (GSM channels are in 200kHz increments). For example, for E-GSM channel number 'n', the OFFS value may be calculated by:

$$OFFS = 40n + \left(\frac{890MHz}{5kHz}\right) = 40n + 178000$$

For 892.2MHz, E-GSM channel number 11, we obtain:

$$OFFS = 40 \times 11 + 178000 = 178440$$

Using the above equation for F_{VCO}, we obtain

$$F_{VCO} = 0 + 178440 \times 5kHz = 892.2MHz$$

Note that 832MHz is 32 times 26MHz and 1664MHz is 64 times 26MHz. This may simplify calculations in the baseband processor. These calculations assume a 26MHz reference crystal frequency. The 26MHz reference can be divided by 1, 2, or 4 internally in the RF6001 for use in the PLL, and the frequency calculation will hold. If a different reference crystal frequency is used, the actual VCO frequency will be calculated by multiplying F_{VCO} above by F_{XTAL}/26MHz.

Reference Oscillator Input

A 26MHz system clock provided by crystal oscillator circuitry must be connected directly to the OSCA and OSCB pins. All of the internal clocks, the OSCO buffered oscillator output, and the gated clock output on LDTO are derived from the reference clock circuitry. The output of the DAC2 pin is used to fine-tune the crystal oscillator frequency.

The OSCM pin is used to control the input buffer circuitry. When OSCM=0, all input buffer circuitry is turned off. When OSCM=1, the input buffer circuitry is turned on. OSCM must be held low during power-up.

Instead of a crystal, a 26MHz system clock (TCXO output) can be connected to the OSCA pin through a decoupling capacitor. This pin possesses a DC voltage of approximately 1.25V. The output of the DAC2 pin is used to fine tune the TCXO frequency.

The figure below illustrates how a TCXO or crystal reference can be connected to the RF6001. Only one of the two options may be used at one time.

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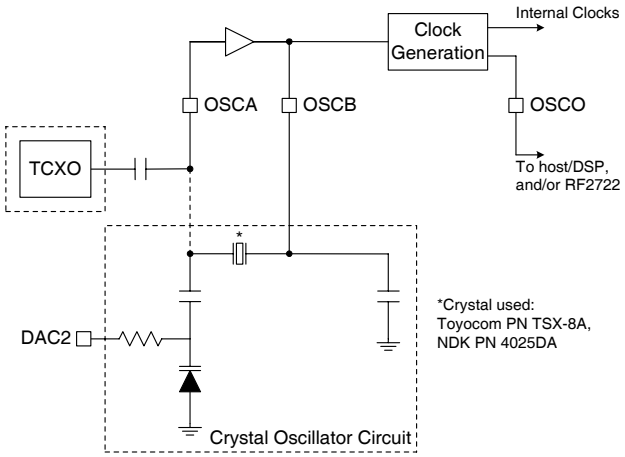


Clock Outputs

The OSCO output may be used to drive the RF2722, or it can provide the system clock for the radio. The OSCOM pin determines the frequency of the buffered OSCO output signal. If OSCOM is low, the output signal is 13MHz. When OSCOM is high, the output signal is 26MHz.

The RF2722 may also be provided a 26MHz clock from the LDTO pin by setting the DC_CLK bit true. This will output a 26MHz clock via the LDTO pin for an amount of time set by DC_TIME3 after RXEN is asserted.

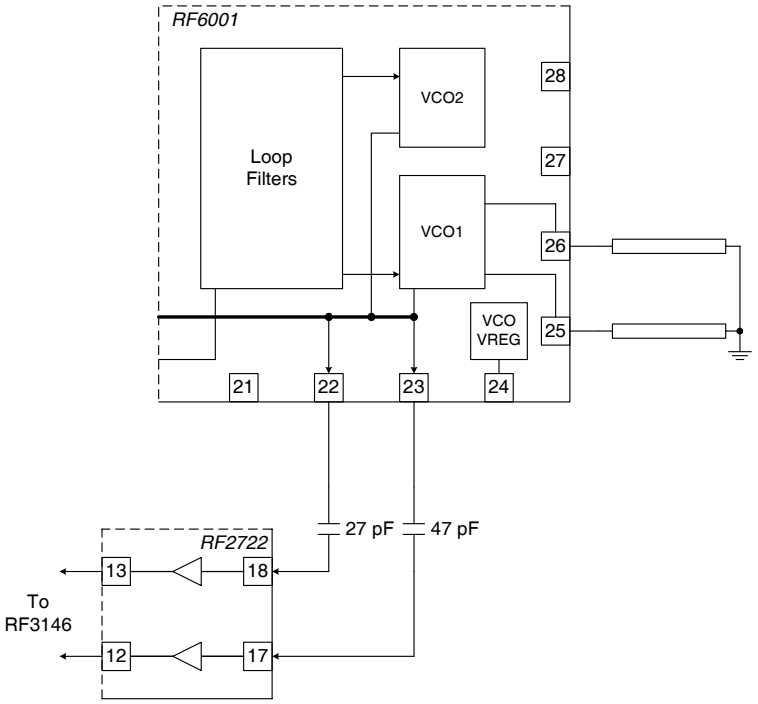
Additional circuitry is included to prevent glitches, or incomplete pulses on the OSCO buffered output pin. This circuitry requires a few stable clock cycles before the output is enabled.

VCO's

The internal power VCO's on the RF6001 are completely integrated and controlled by the on-chip Fractional-N PLL. Both low-band (VCO1) and high-band (VCO2) RF outputs can be matched to 50Ω with a single series capacitor. VCO1 requires external inductors to ground of approximately 2.2nH with ±5% tolerance and Q≥30 on pins 25 and 26. Using standard FR4 material (DK=4.25@1GHz, loss tangent=0.014) the inductor physical dimensions can be printed according to the table below based on the distance from top layer metal to RF ground plane:

Inductance (nH)	Line Width (mils)	Line Length (mils)	Gnd Plane Spacing (mils)
2.5	10	350	5
2.5	10	250	10
2.5	10	210	15
2.5	10	190	20

The output of the VCO's should be connected to the transmit buffers located in the RF2722, as shown in the diagram below:



General Purpose Output Control

The RF6001 provides three general purpose output pins, GPO1, GPO2, and GPO3; a timing control unit is implemented within the RF6001. This timing control is identical to that in the RF2722 for the GPO's with added GPO control in TX modes. The timing controls are set by the DCTIME2 (11:0) and TRD bits in the TRSW register. The GPO values used during the startup of RX or TX bursts are defined by the TRDCRX (2:0) and TRDCTX (2:0) bits in the CFG3 register. This allows the RF6001 to control the TX/RX switch to provide more isolation during DC offset correction in RX mode, or to provide more isolation for the PA output power before ramping up in TX mode.

Power Supplies and Control Signals

The RF6001 has four primary supply pins: V_{DD}, V_{CC}, V_{CCV}, and V_{DDRX}. These pins require a 2.7V to 3.0V supply, usually from a voltage regulator on the application circuit board. These four supply pins must be maintained within 0.3V of each other. That is, all four supplies should be power up or down together. The part is not designed to allow one supply to be at 2.7V to 3V with the others at 0V.

The recommended start-up and power-on sequence for the RF6001 is described below.
1) Power-down: all power supplies and enable lines are low (OSCM, RXEN, TXST, TXEN).
2) Standby Mode: Board regulators to V_{DD}, V_{CC}, V_{CCV}, and V_{DDRX} are enabled. All enable lines are low. The internal digital voltage regulator (between V_{DD} and DCD) requires approximately 50us to settle, triggering the internal power-on reset (POR) circuit. It is recommended that the baseband processor send a RESET op-code to the RF6001 at this point, as well.
3)Idle Mode: The reference oscillator input circuits and output buffer (OSCO) are enabled by setting the OSCM pin high. The oscillator input and output circuits require up to 1ms to settle.
4) Active Mode (either Receive or Transmit): The required Receive or Transmit signal path and PLL/VCO circuits are enabled by the RXEN or TXST pin, respectively.

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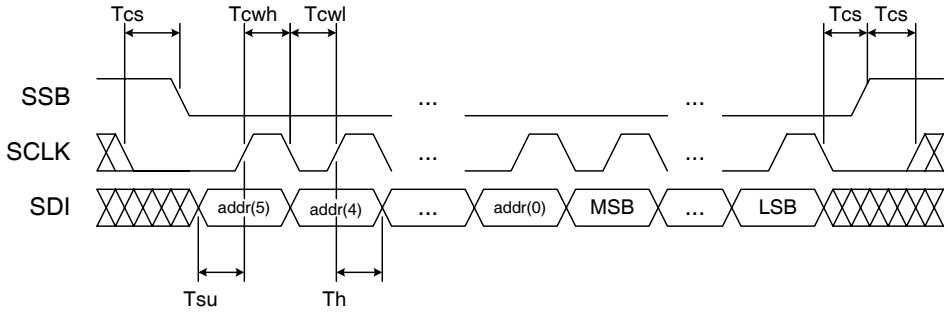
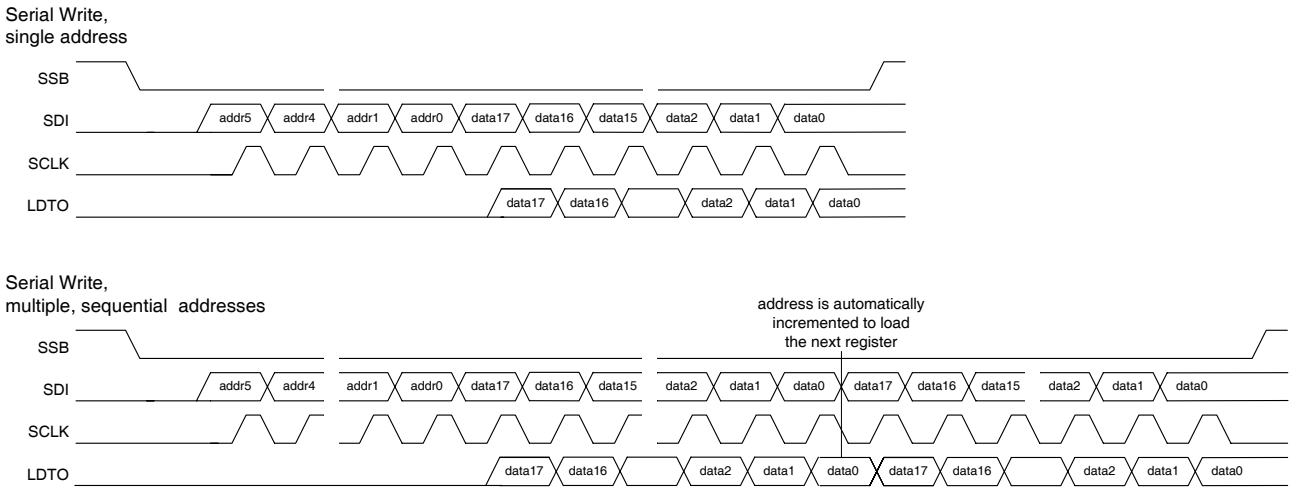
Serial Data Interface and Device Control

A three wire serial data interface allows user programming of the internal control registers in the RF6001. The serial data interface consists of the serial select (SSB), serial data in (SDI) and serial clock (SCLK) pins. The lock detect/test out (LDTO) pin is by default configured as an output from the serial interface, but may be used to monitor various internal PLL signals, as well. The serial interface contains a set of 32 18-bit registers that are individually accessed by 6-bit addresses.

The figure below shows a timing diagram for a serial transfer to the RF6001 serial data interface. Refer to the Electrical Specifications for the timing margin requirements. The SSB pin is normally high. A serial transfer is initiated by taking SSB low. The address and data bits on the SDI pin are shifted in on rising edges of the SCLK pin, MSB first. The data is latched and changes take effect on the falling edge of the clock pulse corresponding to the last (18^{th}) data bit in the addressed register. If the transfer is interrupted, such that the 18th data bit clock pulse does not occur, then no data is written to the register.



Data may be written to the registers in two ways: one register per serial transfer, or several sequential (adjacent) registers per serial transfer. These actions are illustrated in the following figure.



The serial interface provides the capability of reading from the registers. If a register is written while the TEN SDI bit is set to zero, then the previous contents of that register will be serially shifted out on the LDTO pin.

The following table illustrates the RF6001 Register Map. A serial transfer is initiated on the falling edge of SSB, and serial data is shifted in MSB first, starting with the register address and then the data.

The RESET opcode (011111) is unique in that once the 011111 opcode is written, the RF6001 is reset, and held in reset until the SSB pin is taken high. It is recommended to reset the RF6001 upon initial power-up of the system by writing the 011111 serial interface opcode. This ensures that the part will start up with the default register settings and that it will not be drawing current unless enabled.

The RMPSEL bit in register PARMP1 determines which set of PA ramp registers (PARMP 3-11) is accessed for both serial transfers and PA ramping. If RMPSEL=0, then a first set of 10 registers is accessed. If RMPSEL=1, then the second set of 10 registers is accessed by the same addresses.

The individual registers and bits are described below. The default values are set upon reset and are binary unless notated with an h (hexadecimal).

RF6001 Register Map

Serial Transfer:	MSB																							LSB
Bit Number:	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	**Address**						**Data**																	
Configuration 1 (CFG1)	000000						CFG1(17:0)																	
Configuration 2 (CFG2)	000001						CFG2(17:0)																	
Configuration 3 (CFG3)	000010						CFG3(17:0)																	
Frequency Offset (OFFS)	000011						OFFS(17:0)																	
Digital AFC Offset (AFCD)	000100						AFCD(17:0)																	
PLL x0 (PLLx0)	000101						PLLx0(17:0)																	
PLL x1 (PLLx1)	000110						PLLx1(17:0)																	
PLL x2 (PLLx2)	000111						PLLx2(17:0)																	
TX Modulation (TXMOD)	001000						TXMOD(17:0)																	
PA Ramp 1 (PARMP1)	001001						PARMP1(17:0)																	
PA Ramp 2 (PARMP2)	001010						PARMP2(17:0)																	
PA Ramp 3 (PARMP3)	001011						PARMP3(17:0)																	
PA Ramp 4 (PARMP4)	001100						PARMP4(17:0)																	
PA Ramp 5 (PARMP5)	001101						PARMP5(17:0)																	
PA Ramp 6 (PARMP6)	001110						PARMP6(17:0)																	
PA Ramp 7 (PARMP7)	001111						PARMP7(17:0)																	
PA Ramp 8 (PARMP8)	010000						PARMP8(17:0)																	
PA Ramp 9 (PARMP9)	010001						PARMP9(17:0)																	
PA Ramp 10 (PARMP10)	010010						PARMP10(17:0)																	
PA Ramp 11 (PARMP11)	010011						PARMP11(17:0)																	
DAC1 Control (DAC1)	010100						DAC1(17:0)																	
DAC2 Control (DAC2)	010101						DAC2(17:0)																	
Calibration (CAL)	010110						CAL(17:0)																	
TR Switch Control (TRSW)	010111						TXTR(17:0)																	
Test (TEST)	011110						TEST(17:0)																	
Reset (RESET)	011111						X(don't care)																	
Calibration 2 (CAL2)	110000						CAL2 (17:0)																	
SSI (SSI)	110001						SSI(17:0)																	
BLANK (BLANK)	110011						BLANK (17:0)																	
DELAY (DELAY)	110100						DELAY (17:0)																	
D_FILL (D_FILL)	110101						D_FILL (17:0)																	
TX_DLY (TX_DLY)	110110						TX_DLY (17:0)																	

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Configuration Register 1 (CFG1)-Address 000000

Location	Bit Name	Default	
CFG1(17)	SMP_SEL	0	Selects the A/D RX sampler. Use 0 for interface to an RF27SS with a common mode voltage of mid-supply ±200mV. Use 1 for interface to other front-ends with common mode voltage outside of this range.
CFG1(16:15)	PLL_EN(1:0)	00	PLL Enable Method Selection 0x=PLL is enabled by RXEN | TXEN | TXST 10=PLL is always disabled 11=PLL is always enabled
CFG1(14)	UAM	0	Use Alternate mode of PA ramping and data gating. If enabled, the RU_DLY[4:0] and RD_DLY[4:0] registers are used to delay the DAC1 ramp up and ramp down, respectively, relative to the TXST signal. In addition, user data is gated into the GMSK modulator while TXST is high. While TXST is low, G_DEF is gated into the modulator. 0=disabled 1=enabled
CFG1(13)	reserved	0	reserved, program to zero (0)
CFG1(12)	UMS	0	If this bit is set high then the first 16 MCK data bits loaded after MD_DLY1 expires in serial mode will be filled with G_DGF as opposed to loading data from the FIFO or serial interface. This is used in serial mode with MS, as the system needs to know to fill the first 16 bits with the default as the first MS is blanked. The 16 bits occur only on the first burst of a multiburst transmission.
CFG1(11)	MCKSEL	0	If programmed high, a nominal delay of 3nsec is added to the MCK input.
CFG1(10)	reserved	0	reserved, program to zero (0)
CFG1(9)	GPRS_TX2	0	Enables GPRS mode 2. In this GPRS mode, the DAC1 will ramp down before ramping to the next power level. Between bursts, the ramp down is initiated by TXST falling. The ramp up is initiated with TXST rising. 0=GPRS mode 2 disabled 1=GPRS mode 2 enabled
CFG1(8)	GPRS_TX1	0	Enables GPRS mode 1. In this GPRS mode, the DAC1 will ramp to the new power level without ramping down to low power. This mode supports the RF6001 legacy PA ramping modes. 0=GPRS mode 1 is disabled 1=GPRS mode 1 is enabled
CFG1(7:5)	RXMODE(2:0)	000	Digital RX Interface Mode 000=I and Q data are multiplexed on the DRI pin with 12-bit accuracy, 13MHz clock rate 001=I and Q data are presented on the DRI and DRQ pins with 16-bit accuracy, 13MHz clock rate 010=I and Q data are presented on the DRI pin with 16-bit accuracy, 8.667MHz clock rate 011=I and Q data are presented on the DRI pin with 16-bit accuracy, 13MHz clock rate 100=I and Q data are presented on the DRI pin with 16-bit accuracy, 26MHz clock rate 101=I and Q data are presented on the DRI pin with 12-bit accuracy, 26MHz clock rate 110=I and Q data are presented on the DRI and DRQ pins with 16-bit accuracy, 26MHz clock rate 111=same as 000
CFG1(4)	S_MODE	1	RX Interface Mode 0=analog mode 1=digital mode
CFG1(3)	DBL	0	SSI Word Rate 0=SSI word rate is equal to the GSM symbol rate 1=SSI word rate is equal to twice the GSM symbol rate
CFG1(2:0)	TRDC_RX(2:0)	000	TRD Receive Mode Settings When RXEN is high, {GPO3, GPO2, GPO1 pins}=TRDC_RX(2:0) for a period defined by DC_TIME3, reverts back to normal GPO settings at the end of this time. When RXEN is low, {GPO3, GPO2, GPO1 pins}={GPO3, GPO2, GPO1}.

Configuration Register 2 (CFG2)-Address 000001

Location	Bit Name	Default	
CFG2(17)	VDS	0	VLIF or DCR Select 0=VLIF 1=DCR
CFG2(16)	QINV	0	Inverts the Q signal path. 0=uninverted, normal polarity 1=inverted polarity
CFG2(15)	IQSWPI	0	Swaps the I and Q signal paths at the input to the digital VLIF processor. 0=normal, unswapped 1=swapped
CFG2(14)	IQSWPO	0	Swaps the I and Q signal paths at the baseband output of the digital VLIF processor. 0=normal, unswapped 1=swapped
CFG2(13)	TRD	0	Transmit/Receive GPO Switch Control. If programmed to 1 then the functionality described by TRDC_TX and TRDC_RX is activated. If programmed to zero then the GPO pins follow the GPO programming at all times.
CFG2(12)	ADEN	1	DC Correction System Enable 1=enabled 0=disabled
CFG2(11)	AD2EN	1	DC Correction System Enable 2 0=DC correction system will continue to operate after the adapt time is elapsed, at the rate defined by ADCLK. 1=DC correction system will stop at the end of the adapt time.
CFG2(10:9)	ADCLK(1:0)	11	DC Correction System Clock Rate, after adapt time is elapsed. Default is 13MHz/48, for slowest adapt. 00=13MHz 01=13MHz/12 10=13MHz/24 11=13MHz/48
CFG2(8:3)	DCAD(5:0)	13h	Fine DC correction fast adapt time. Programs in steps of (48/13) μs. Default is 70μs.
CFG2(2:0)	CHBW(2:0)	010	Selects the channel filter 3dB bandwidth 000=80kHz 001=85kHz 010=90kHz 011=95kHz 100=100kHz 101=110kHz 110=120kHz 111=135kHz

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Configuration Register 3 (CFG3)-Address 000010

Location	Bit Name	Default	
CFG3(17)	GPO3	0	General Purpose Output Pins. Pins are set high or low as programmed, unless overridden by TR settings, controlled by TRD, TRDC_RX, TRDC_TX, and the RXEN and TXEN pins.
CFG3(16)	GPO2	0	
CFG3(15)	GPO1	0	
CFG3(14:12)	TRDC_TX(2:0)	000	TRD Transmit Mode Settings. When TXST is high, {GPO3, GPO2, GPO1 pins}=TRDC_TX(2:0) for a period defined by TXENU, reverts back to normal GPO settings at the end of this time. When TXST is low, {GPO3, GPO2, GPO1 pins}={GPO3, GPO2, GPO1}
CFG3(11:10)	PLLSEL(1:0)	00	PLL Preset Selection, determines the active set of PLLxx registers. 00=PLL00, PLL01, PLL02 registers are active 01=PLL10, PLL11, PLL12 registers are active 10=PLL20, PLL21, PLL22 registers are active 11=PLL30, PLL31, PLL32 registers are active
CFG3(9)	reserved	0	reserved, program to zero (0)
CFG3(8)	reserved	0	reserved, program to zero (0)
CFG3(7)	RMPSEL	0	PA Ramp Table Select, determines the active set of PA ramp registers. 0=ramp table 0 is active 1=ramp table 1 is active
CFG3(6)	R1316B	0	Changes the ramp up and ramp down time from 16quarter symbols to 13quarter symbols. 0=ramp time is 16qst 1=ramp time is 13qst
CFG3(5)	reserved	0	reserved, program to zero (0)
CFG3(4)	reserved	0	reserved, program to zero (0)
CFG3(3:0)	DAGC(3:0)	3h	Digital Gain Control Gain is equal to -18dB+DAGC*6dB, from -18dB to +60dB. Default is 0dB. 0000=gain of -18dB 0001=gain of -12dB ... 1100=gain of +54dB 1101=gain of +60dB 1110=gain of +60dB 1111=gain of +60dB

Frequency Offset Register (OFFS)-Address 000011

Location	Bit Name	Default	
OFFS(17:0)	OFFS(17:0)	0	PLL Frequency Offset The PLL/VCO Lock Frequency is determined by the equation: $F_{VCO}=F_{BASE}+OFFS*5kHz+AFCD*26MHz/2^{24}$, where F_{BASE} is set according to the $F_{BASE}(1:0)$ value, and AFCD is set according to the AFCD register value. See the AFCD and PLLx0 register descriptions. The RF6001 takes changes in R and VCODIV into account in the calculation of F_{VCO}. However, if the frequency present at the OSCA pin is not 26MHz, the VCO frequency will be $F_{VCO}'=F_{VCO}*F_{REF}/26MHz$, where F_{VCO}' is the actual VCO frequency with a non 26MHz reference, and F_{REF} is the actual frequency present at the OSCA pin.

Digital AFC Offset Register (AFCD)-Address 000100

Location	Bit Name	Default	
AFCD(17:0)	AFCD(17:0)	0	Digital AFC offset adjustment for PLLs. This is a two's component (signed) value. See the OFFS register description for more information on setting the PLL/VCO frequency.

PLL Register x0 (PLLx0)-Address 000101

Location	Bit Name	Default	
PLLx0(17)	CPI_SW	1	Charge pump current switch during calibration. 0=Constant Current 1=Switches high during calibration
PLLx0(16)	VT_EN	0	VT pin enable 0=Charge Pump/Internal Loop Filter are disconnected from VT pin 1=Charge Pump/Internal Loop Filter are connected to VT pin
PLLx0(15)	LD_EN	0	Lock Detect Enable for PLL This must also be selected via the test mux; see the TEST register description for more information.
PLLx0(14)	VTC_EN	1	VCO Coarse Tune Enable 0=VCO coarse tuning system is disabled 1=VCO coarse tuning system is enabled
PLLx0(13)	KV_EN	1	KV Calibration Enable 0=disabled 1=enabled
PLLx0(12)	LPFBW	0	Loop Filter Bandwidth Selector 0=External RX RF2722 1=Internal TX VCO's
PLLx0(11)	LPF	0	Loop 1 Filter Bypass 0=Internal Loop Filter is used 1 =Internal Loop Filter is bypassed
PLLx0(10)	CPL	0	Charge Pump Leakage Current 0=minimum value 1=2*minimum value
PLLx0(9)	CPI	0	Charge Pump Current 0=low current setting, used for RX with the RF2722 1=high current setting, used for TX with internal VCOs
PLLx0(8)	PDP	0	Loop 1 Phase Detector Polarity 0=negative, VCO freq decreases with increasing tuning voltage, used for RX with the RF2722 1=positive, VCO freq increases with increasing tuning voltage, used for TX with the internal VCOs
PLLx0(7:6)	P(1:0)	00	Prescaler Modulus The prescaler is set as follows: 0x=prescaler is bypassed, (0MHz to 500MHz at prescaler input) 10=4/5 Mode (494MHz to 2GHz at prescaler input) 11=8/9 Mode (1.95GHz to 2.5GHz at prescaler input)
PLLx0(5:4)	VCOSEL(1:0)	00	VCO Select 00=external VCO, FIN pin is used as input 10=integrated VCO1 11=integrated VCO2
PLLx0(3:2)	VCODIV(1:0)	00	VCO Post Divider 0x=The VCO is directly coupled to the Prescaler. 10=The VCO is followed by a fixed divide by 2. 11=The VCO is followed by a fixed divide by 4. This setting is used with the RF2722.
PLLx0(1:0)	reserved	00	Program to zero (0).

PLL Register x1 (PLLx1) - Address 000110

Location	Bit Name	Default	
PLLx1(17:14)	LPF_V(3:0)	3h	VCO Coarse Tune Voltage
PLLx1(13:12)	CT_NOFFS (1:0)	2h	VCO Coarse Tune Offset Adjustment
PLLx1(11:9)	TLOCK(2:0)	3h	KV Calibration Wait Time
PLLx1(8:0)	DN(8:0)	96h	Delta-N Value for KV Calibration

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PLL Register x2 (PLLx2) - Address 000111

Location	Bit Name	Default	
PLLx2(17:16)	FBASE(1:0)	00	Base Frequency 00=F_{BASE} is 0Hz 01=F_{BASE} is 832MHz 1x=F_{BASE} is 1664MHz See the OFFS register description for more information on setting the PLL/VCO frequency.
PLLx2(15:11)	CT_DEF(4:0)	0	VCO Coarse Tune Coefficient
PLLx2(10:8)	CT_MOFFS(2:0)	3h	VCO Coarse Tune Offset
PLLx2(7:6)	CTN(1:0)	01	VCO Coarse Tune Type 00=3 bits 01=4 bits (Internal VCO1 or External RF2722 VCO) 10=5 bits (Internal VCO2) 11=reserved
PLLx2(5:0)	KV_DEF(5:0)	20h	KV Calibration Setting

TX Modulation Register (TXMOD) - Address 001000

Location	Bit Name	Default	
TXMOD(17)	TXAD	0	TX Interface Mode 0=analog TX interface 1=digital TX interface
TXMOD(16)	reserved	0	reserved, program to zero (0)
TXMOD(15)	TX_DE	0	Differential Encoder, used with digital TX interface 0=input data on MDI is not differentially encoded 1=input data on MDI is differentially encoded
TXMOD(14)	TX_INV	0	Symbol Polarity after differential encoding 0=data is not inverted 1=data is inverted
TXMOD(13:8)	PHADJ(5:0)	0	Symbol Clock Phase Offset offset=(PHADJ/13)µs
TXMOD(7:4)	TX_THP(3:0)	0	TX Analog Interface, positive threshold $TX\_THP \approx (12.5 \cdot V_{PK}) - 2$
TXMOD(3:0)	TX_THN(3:0)	0	TX Analog Interface, negative threshold $TX\_THN \approx (12.5 \cdot V_{PK}) - 2$

PA Ramp Register 1 (PARMP1) - Address 001001

Location	Bit Name	Default	
PARMP1(17:10)	PAT(7:0)	9Ah	PA Ramp Delay, delay time from the rising edge on the TXST pin to the start of the ramp. Delay=PAT*(12/13)µs.
PARMP1(9:0)	PAG(9:0)	3AEh	PA Ramp Gain, used as a scaling factor on the PA Ramp Waveform Gain=(PAG/1024)

PA Ramp Register 2 (PARMP2) - Address 001010

Location	Bit Name	Default	
PARMP2(17)	TXENIO	1	TXEN pin direction 0=TXEN is input 1=TXEN is output, generated by PA ramping system
PARMP2(16)	PAEN	1	PA Ramp Enable 0=disabled, DAC1 is controlled by DAC1EN and DAC1V 1=enabled, DAC1 is controlled by PA ramp control system, initiated by a rising edge on TXEN or TXST pins
PARMP2(15:14)	reserved	0	reserved, program to zero (0)
PARMP2(13:6)	TXENU(7:0)	98h	TXEN rising edge delay from TXST Delay=TXENU*(12/13)µs
PARMP2(5:0)	TXEND(5:0)	6h	TXEN falling edge delay from end of PA ramp Delay=TXEND*(12/13)µs

PA Ramp Registers 3 through 11 (PARMP3-PARMP11) - Addresses 001011 to 010011

Location	Bit Name	Default	
PARMP3(17:16)	reserved	0	reserved, program to zero (0)
PARMP3(15:6)	PAR[0,9:0]	see text	PA Ramp Waveform, step 0
PARMP3(5:0)	PAR[1,9:4]	see text	PA Ramp Waveform, step 1
PARMP4(17:14)	PAR[1,3:0]	see text	PA Ramp Waveform, step 1, cont.
PARMP4(13:4)	PAR[2,9:0]	see text	PA Ramp Waveform, step 2
PARMP4(3:0)	PAR[3,9:6]	see text	PA Ramp Waveform, step 3
PARMP5(17:12)	PAR[3,5:0]	see text	PA Ramp Waveform, step 3, cont.
PARMP5(11:2)	PAR[4,9:0]	see text	PA Ramp Waveform, step 4
PARMP5(1:0)	PAR[5,9:8]	see text	PA Ramp Waveform, step 5
PARMP6(17:10)	PAR[5,7:0]	see text	PA Ramp Waveform, step 5, cont.
PARMP6(9:0)	PAR[6,9:0]	see text	PA Ramp Waveform, step 6
PARMP7(17:8)	PAR[7,9:0]	see text	PA Ramp Waveform, step 7
PARMP7(7:0)	PAR[8,9:2]	see text	PA Ramp Waveform, step 8
PARMP8(17:16)	PAR[8,1:0]	see text	PA Ramp Waveform, step 8, cont.
PARMP8(15:6)	PAR[9,9:0]	see text	PA Ramp Waveform, step 9
PARMP8(5:0)	PAR[10,9:4]	see text	PA Ramp Waveform, step 10
PARMP9(17:14)	PAR[10,3:0]	see text	PA Ramp Waveform, step 10, cont.
PARMP9(13:4)	PAR[11,9:0]	see text	PA Ramp Waveform, step 11
PARMP9(3:0)	PAR[12,9:6]	see text	PA Ramp Waveform, step 12
PARMP10(17:12)	PAR[12,5:0]	see text	PA Ramp Waveform, step 12, cont.
PARMP10(11:2)	PAR[13,9:0]	see text	PA Ramp Waveform, step 13
PARMP10(1:0)	PAR[14,9:8]	see text	PA Ramp Waveform, step 14
PARMP11(17:10)	PAR[14,7:0]	see text	PA Ramp Waveform, step 14, cont.
PARMP11(9:0)	PAR[15,9:0]	see text	PA Ramp Waveform, step 15

DAC1 Control Register (DAC1) - Address 010100

Location	Bit Name	Default	
DAC1(17)	DAC1EN	0	DAC1 Enable, this bit unconditionally turns on DAC1. Should be programmed to zero (0) for normal PA operation (PAEN=1). 0=disable 1=enabled
DAC1(16)	TXENFSD	0	TXEN Failsafe Disable. The failsafe circuitry prevents TXEN from staying high for more than eight timeslots, to prevent PA damage. 0=TXEN failsafe circuit enabled 1=TXEN failsafe circuit disabled
DAC1(15:0)	DAC1V(15:0)	147Bh	DAC1 Value If PAEN=1, then DAC1V(15:0) is used as the minimum value of the DAC1/VRAMP pin output voltage.

DAC2 Control Register (DAC2) - Address 010101

Location	Bit Name	Default	
DAC2(17)	DAC2EN	0	DAC2 Enable 0=disable 1=enabled
DAC2(16)	FNZ	0	If programmed high, the modulation to the fractional divider is forced to zero. This is a test mode.
DAC2(15:0)	DAC2V(15:0)	0	DAC2 Value

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Calibration Register (CAL) - Address 010110

Location	Bit Name	Default	
CAL(17:16)	VCOI(1:0)	10	VCO Bias Setting 00=Current1 (lowest) 01=Current2 10=Current3 11=Current4 (highest)
CAL(15)	VSUEN	0	VCO Bias Startup Inhibit 0=VCO bias startup circuit is disabled 1=VCO bias startup circuit is enabled
CAL(14:10)	TVCO(4:0)	8h	VCO Warm-up Time Sets the time allotted for the VCO to warm up before calibrations or other PLL operations begin. Warm-up time=TVCO*(32/26e6)μs
CAL(9)	RC_EN	1	RC Calibration System Enable 0=disabled 1=enabled
CAL(8:5)	RCOFFS(3:0)	0	RC Calibration Offset
CAL(4:0)	RC_DEF(4:0)	Ch	RC Calibration Default Value

TR Switch Control (TRSW) - Address 010111

Location	Bit Name	Default	
TRSW(17)	REGEN	0	Controls the DCAD and DCO regulators. Program to zero in normal operation.
TRSW(16)	DC_CLK	0	DC Offset Correction Clock 0=DC clock function disabled 1=26MHz clock is sent to RF2722 via the LDTO pin for the amount of time set by DC_TIME3. This timer is activated by asserting RXEN.
TRSW(15:10)	reserved	0	reserved, program to zero (0)
TRSW(9:0)	DC_TIME3(9:0)	51h	Sets the number of 26MHz clock cycles from the rising edge of TX_ST or RX_EN. These clocks are ported out of LDTO to the front-end IC. Programs in steps of Tsymbol/3.

Test Register (TEST) - Address 011110

Location	Bit Name	Default	
TEST(17)	TM_BIT	0	Test Mode Enable 0=normal functional mode 1=scan mode
TEST(16:15)	ADTM(1:0)	00	ADC test mode, routes the outputs of the I or Q ADCs to DRI and DRQ pins 0x=normal mode 10=output of I ADC quantizers are present on DRI and DRQ 11=output of Q ADC quantizers are present on DRI and DRQ
TEST(14)	TXTEST	0	Transmit Test Enable, enables PN txdata sequence generator 0=disabled 1=enabled
TEST(13)	ADTEST	0	PLL ADC Test mode 0=disabled 1=enabled
TEST(12)	reserved	0	reserved, program to zero (0)
TEST(11:10)	CALSEL(1:0)	00	Calibration read back select 00=(cpr, vtc, kv) 01=(13'b0, rc) 10=(1'b0, di_fn) 11=(18'b0)
TEST(9)	reserved	0	reserved, program to zero (0)
TEST(8)	DATEST	0	PLL DAC Test Mode 0=disabled 1=enabled
TEST(7)	CPU	0	Charge Pump Up 0=no effect 1=forces charge pumps to pump up (source) on PLL1 and PLL2
TEST(6)	CPD	0	Charge Pump Down 0=no effect 1=forces charge pumps to pump down (sink) on PLL1 and PLL2
TEST(5)	TEN	0	Test Mux Enable 0=LDTO pin provides output of serial interface 1=LDTO pin provides output of Test Multiplexer
TEST(4:3)	TSEL(1:0)	00	Test Mux Selection 00=PLL Test Mux 01=Transmit Test Mux 1x=reserved
TEST (2:0)	TMUX(2:0)	000	Test Multiplexer Output Selection, IF TSEL=00 then TMUX is defined as: 000=Lock Detect 001=Prescaler Output 010=modulus control 011=N Divider Output, Fv 100=R Divider Output, Fr 101=pump up 110=pump down 111=lock detect IF TSEL=01 then TMUX is defined as: 000=TX data 001=CLK_TX_ANIN 010=Sample_IQ 011=Sample_MDI 100=ISample[1] 101=ISample[0] 110=QSample[1] 111=QSample[0]

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Reset - Address 011111

Location	Bit Name	Default	
RESET (17:0)	reserved	0	reserved, program to zero (0) The RF6001 IC is forced into reset (default state) when the RESET address is written. The part is held in reset until the SSB signal is taken high after the address is written.

Calibration Register 2 (CAL2) - Address 110000

Location	Bit Name	Default	
CAL2(17:15)	reserved	0	reserved, program to zero (0).
CAL2(14)	R0816B	0	If programmed high, then every other PAR starting with PAR[1] is used to form the ramp. This shortens the ramping time to 8 quarter symbol times. If programmed low, the ramping time is 16 quarter symbol times.
CAL2(13)	EALGN	0	Resets the GMSK modulator symbol raster when the modulator input transitions from G_DEF to user data. This can by used in conjunction with G_DLY to allow finer control of the GMSK modulator latency. 0=GMSK modulator symbol raster set by TXST 1=GMSK modulator symbol raster set by user data
CAL2(12:0)	reserved	0	reserved, program to zero (0).

SSI - Address 110001

Location	Bit Name	Default	
SSI(17:16)	CLKRM(1:0)	00	CLKR Mode 0=CLKR is enabled when ENR=1, but operates only during the active data portion of the transfer (disabled during any blank data portion). 01=CLKR is enabled when ENR=1 and remains on regardless of the state of DBL. 1x=CLKR is always disabled.
SSI(15)	RXCKB	0	Receive Clock Source 0=CLKR is an output 1=CLKR is an input
SSI(14)	RXFSB	0	Receive Frame Sync Source 0=FSR is an output 1=FSR is an input
SSI(13)	FS_LOC	0	Frame Sync Location 0=FSR coincident with MSB of I data 1=FSR occurs on clock before MSB of I data
SSI(12)	EN_SEL	0	Receive SSI Mode 0=RXSSI starts with ENR 1=RXSSI starts with RXEN
SSI(11)	RX_T	0	RXSSI Trailing Clock Pulses. Adds clocks to the end of an RXSSI transfer. 0=No extra clock cycles are added to the end of an RXSSR transfer. 1=5 extra clock cycles are added to the end of an RXSSR transfer.
SSI(10)	CLKRINV	0	Inverts the CLKR signal. 0=Uninverted, normal polarity 1=Inverted polarity
SSI(9)	TXD_MODE	0	TX Digital Interface Mode 0=Digital TX interface, MCK and MS are outputs 1=Digital TX interface, MCK and MS are inputs
SSI(8:7)	TXF(1:0)	00	Controls the FIFO Interface Modes 00=TX FIFO disabled 01=No MS mode. FIFO will shift in bits on every falling edge of MCK, regardless of the MS signal. 10=MS FRAME mode. FIFO will shift in bits on every falling edge of MCK, if MS is high. 11=MS PULSE mode. At every MS pulse, the FIFO will shift in a predetermined number of bits. The position of MS, relative to the first data bit is controlled by MS_LOC. The number of bits shifted in is determined by MS_LEN[4:0].
SSI(6)	TXCKINV	0	TX Clock Invert 0=Data is latched on the falling edge of MCK 1=Data is latched on the rising edge of MCK
SSI(5)	INTNEN	0	Test bit. Program to 0.
SSI(4:1)	MS_LEN(3:0)	0	MS Pulse Length. In TXF=11 mode, MS_LEN controls the number of bits the TX FIFO will shift in, on every MS pulse. MS_LEN=0: 4 bits MS_LEN=6: 10 bits MS_LEN=12: 24 bits MS_LEN=1: 5 bits MS_LEN=7: 11 bits MS_LEN=13: 26 bits MS_LEN=2: 6 bits MS_LEN=8: 12 bits MS_LEN=14: 32 bits MS_LEN=3: 7 bits MS_LEN=9: 13 bits MS_LEN=15: 48 bits MS_LEN=4: 8 bits MS_LEN=10: 14 bits MS_LEN=5: 9 bits MS_LEN=11: 16 bits
SSI(0)	MS_LOC	0	MS Pulse Location 0=transfer of first data bit occurs on same clock period as the pulse on MS 1=transfer of first data bit occurs on the next clock period after the pulse on MS

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RX Blanking (BLANK) - Address 110011

Location	Bit Name	Default	
BLANK (17)	MSR	0	Controls the behavior of the MS pulse in a GPRS serial TX burst, if the RF6001 is the bus master. If MSR is high, then an MS pulse will occur every 16 MCK clock pulse, even between GPRS bursts. If MSR is low, the MS pulse will appear with the first MCK pulse of each burst, regardless of how MCK pulses have elapsed since the last MS pulse. 0=MS resume disabled 1=MS resume enabled
BLANK (16:14)	G_CNT(2:0)	000	This field allows variable blanking of user data bits. In FIFO, this bit is only active in MS PULSE mode (TXF=2). On the rising edge of MS, the FIFO will ignore the first GCNT bits on the serial interface. In TX serial mode, the GMSK differential encoder and modulator will ignore the first GCNT bits. During this time, G_DEF will be gated to the modulator. In GPRS mode, GCNT is only active in the first burst.
BLANK (13)	DE_INIT	0	Power on default of the differential encoder starting value.
BLANK (12)	reserved	0	reserved, program to zero (0).
BLANK (11:6)	BLK_DLY(5:0)	18h	Channel filter blanking delay. Delay=BLK_DLY*3.69us.
BLANK (5:0)	AGC_DLY(5:0)	26h	RX output blanking delay. Delay=AGC_DLY*3.69us.

DELAY - Address 110100

Location	Bit Name	Default	
DELAY (17)	ADEN_2	1	Second DC Correction System Enable
DELAY (16)	AD2EN_2	1	Second DC Correction System Enable 2 0=DC correction system will continue to operate after the adapt time is elapsed, at the rate defined by ADCLK. 1=DC correction will stop at the end of the adapt time.
DELAY (15:14)	ADCCLK_2 (1:0)	11	DC Correction System Clock Rate, after adapt time is elapsed. Default is 13MHz/48, for slowest adapt. 00=13MHz 01=13MHz/2 10=13MHz/24 11=13MHz/48
DELAY (13:8)	DCAD_2(5:0)	25h	Fine DC correction fast adapt time. Programs in steps of (48/13)us. Default is 70us.
DELAY (7:0)	reserved	0	reserved, program to zero (0).

TX Data Control (DFILL) - Address 110101

Location	Bit Name	Default	
DFILL (17)	FCLR	0	If FCLR is set high, the FIFO will be cleared. Once the operation is complete, the SDI bit will automatically revert low.
DFILL (16)	G_DEF	0	G_DEF is the input value to the GMSK modulator when the modulator data input is not active.
DFILL (15)	reserved	0	reserved, program to zero (0).
DFILL (14:10)	G_DLY(4:0)	0	This field will increase the latency of the GMSK modulator in 1/16 symbol increments. The modulator delay can be adjusted from 12.2 quarter symbol times (qst) to 19.95qst. G_DLY cannot be used without EALGN.
DFILL (9:5)	RD_DLY(4:0)	0	In UAM mode, RD_DLY can be used to delay the ramp down in 1/8S increments, relative to the falling edge of TXST. This field is not used if UAM is low.
DFILL (4:0)	RU_DLY(4:0)	0	In UAM mode, RU_DLY can be used to delay the ramp up in 1/8S increments, relative to the rising edge of TXST. Note that this field is only used in GPRS mode because PAT always controls the first ramp up delay.

TX_DLY - Address 110110

Location	Bit Name	Default	
TX_DLY (17:9)	MD_DLY2(8:0)	0	In a GPRS transmission, with UAM=0, when TX_ST falls at the end of the present TX timeslot, the data from the FIFO stops after the present data symbol completes and the value of G_DEF is used until MD_DLY2 expires. MD_DLY2 timing begins in this mode with the end of the symbol after the fall of TX_ST. If UAM is true then data flow restarts after MD_DLY2 expires AFTER the rising edge of TX_ST. In this mode MD_DLY2 is timed from the rising edge of TX_ST.
TX_DLY (8:0)	MD_DLY1(8:0)	0	Sets the delay in 1/8 symbol time increments from the first rising edge of TX_ST to the start of data into the modulator. G_DEF fills the input data before MD_DLY1. In serial mode, MD_DLY1 functions only if MCK is an output from the RF6001.

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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

A = 0.64 x 0.28 (mm) Typ.
B = 0.28 x 0.64 (mm) Typ.
C = 5.50 (mm) Sq.

Dimensions in mm.

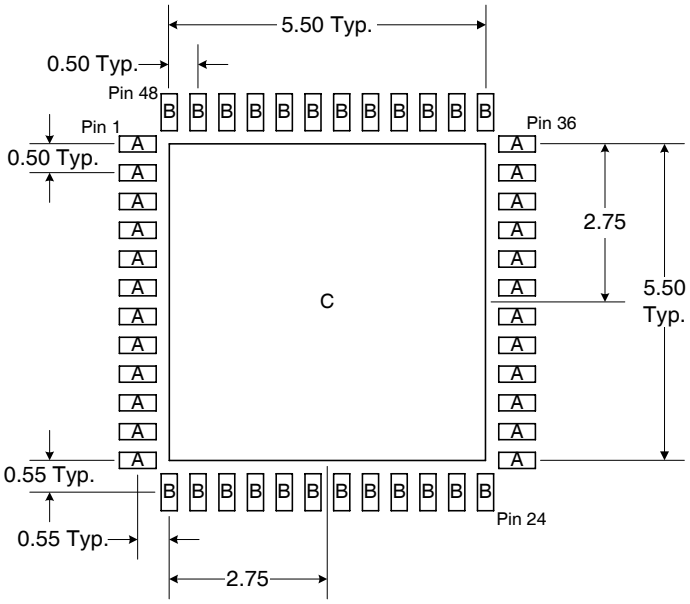

Figure 17. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

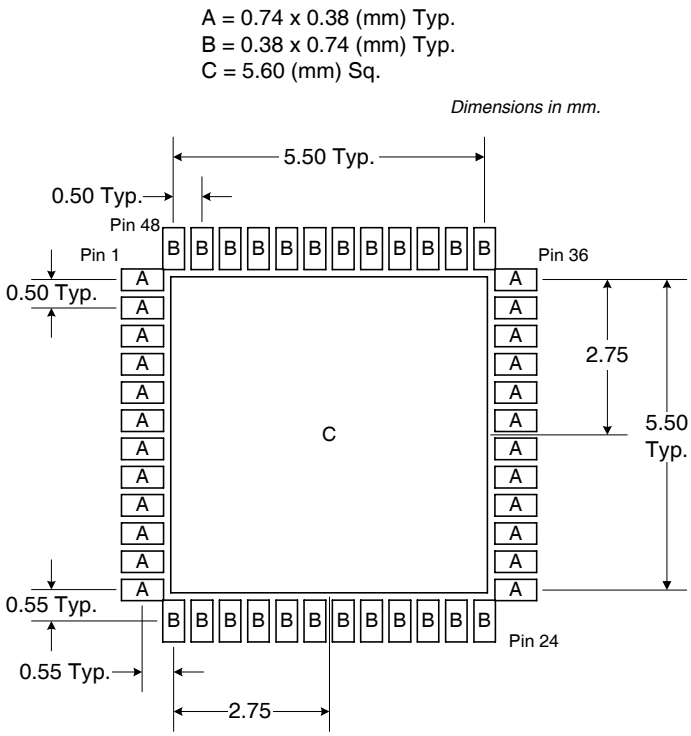

Figure 18. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB Metal Land Pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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Revision Data

Prelim 040414	LY	Specification Table *Power Supply, Maximum Current by Pin:* added four rows under this heading. Application Information *Power Supplies and Control Signals:* replaced with "General Purpose Output Control" and "Power Supplies and Control Signals". Register Tables *RF6001 Register Map, Calibration (CAL):* changed data from "CAL5(17:0)" to "CAL(17:0)". *RF6001 Register Map, TX Data (TXDT):* deleted row. *RF6001 Register Map, Calibration 2 (CAL2):* added row. *RF6001 Register Map, BLANK (BLANK):* added row. *RF6001 Register Map, DELAY (DELAY):* added row. *RF6001 Register Map, D_FILL (D_FILL):* added row. *RF6001 Register Map, TX_DLY (TX_DLY):* added row.
Prelim 040310	LY	*Initial Datasheet. (Based on 6001-29, revision code Prelim 040309.) Reasons for new revision:* • Improved OSCO driver swing and load capability. (The level of the clock drive was too low into the capacitive load which was presented to it by some customers. The specification on this revision is to be able to drive a capacitive load up to 30pF.) • The TXDT register was removed. • Changed default value of TLOCK to "3'd3". • Added MSKSEL bit in CFG1(11). • PLL and phase detector changes to improve slew rate and overall settle time. (KV_DEF is now used for KV_VAL during KV calibration.) • AFC DAC output is tri-stated when DAC2EN bit is low. Specification Table *PLL Specification, Frequency Range, internal*: added line with min specification of "0MHz" and max specification of "2100MHz". *PLL Specification, Frequency Range, FIN Pin*: existing line with min specification of "0MHz" and max specification of "550MHz". *Oscillator Output Buffer, Output Voltage (V_{OUT})*: changed min specification from "600mV$_{P-P}$" to "800mV$_{P-P}$". *Oscillator Output Buffer, Load Capacitance*: changed min specification from "1pF" to "5pF", and max specification from "10pF" to "30pF". *DAC1 and DAC2 Specifications, DAC2 (AFC) Tri-State Output Impedance*: added. Application Information *Transmit Modulation Interface Digital Mode*: added second and fourth paragraphs. *Addition of Delay on MCK*: added. *Transmit Test Modes*: changed to "Transmit Test Mode"; first paragraph updated to reflect single test mode, and "TXTEST=1, TXTM=0" added to first paragraph; "TXTEST=1, TXTM=1" section removed. Register Tables *CFG1, CFG1(11:10)*: changed to "CFG1(10)". *CFG1, CFG1(11)*: added as "MCKSEL" bit. *PLLx1, PLLLx1(11:9)*: default value changed from "0" to "3h". *TXDT*: table removed.
Prelim 040317	LY	Application Information *Synthesizer Information, VCO's:* replaced two paragraphs following table with one paragraph; updated diagram.
Rev A0 040930	JM	Banner: Changed from "Proposed" to "Preliminary". PCB Design Requirements: added.
Rev A1 041118	JM	Banner: "Preliminary" banner removed. Trademark Information: added.
Rev A2 050602	PB	Application Information *Analog I/Q Mode:* replaced first paragraph with seven new paragraphs and a table. Register Tables *TXMOD, TXMOD(7:4):* changed equation. *TXMOD, TXMOD(3:0):* changed equation.
Rev A3 050929	Admin	"RoHS-Compliant & Pb-Free" notation and RoHS information added.

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