RF6549

2.7V to 4.4V, 915MHz Transmit/Receive Module; Thru Mode 400MHz to 928MHz

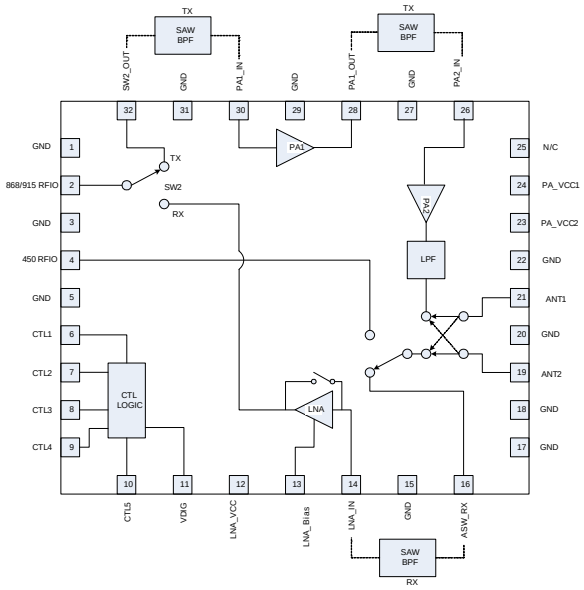
Package: LGA, 32-Pin, 6mm x 6mm

Features

- Tx Output Power: 27dBm
- Single 50Ω Bi-directional Transceiver Interface
- Thru Path Insertion Loss: 1dB
- Antenna Diversity Switch
- LNA with Bypass mode

Applications

- Wireless Automated Metering
- Wireless Alarm Systems
- Portable Battery Powered Equipment
- Smart Energy
- 868MHz/900MHz ISM Band Application
- 450MHz Rx Thru Path
- Single Chip RF Front End Module



Functional Block Diagram

Product Description

This module is intended for 915MHz AMR solutions. It provides separate ports for Rx and Tx paths and two ports on the output for connecting a diversity solution or a test port. The PA section provides a nominal output power of 28dBm. The device is provided in a 6mm x 6mm, 32-pin package.

Ordering Information

RF6549	ISM Band Transmit/Receive Module w/ Diversity Antenna Switch
RF6549PCK-410	Fully Assembled Evaluation Board and 5 loose pieces
RF6549SB	5-Piece Bag
RF6549SQ	25-Piece Bag
RF6549SR	100-Piece Reel
RF6549TR7	Standard 750-Piece Reel
RF6549TR13	Standard 2500-Piece Reel

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Absolute Maximum Ratings

Parameter	Rating	Unit
Voltage	5.25	V
Storage Temperature Range	-40 to 150	°C
Operating Temperature Range	-40 to 85	°C
Maximum Input Power to PA, pin 30, 2 (no damage)	+3	dBm
Maximum Input Power to PA, pin 26 (no damage)	+23	dBm
Maximum Input Power to LNA, pin 19,22 (no damage)	+10	dBm
Thermal Resistance	52	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					Specifications are at nominal supply voltage, control voltage, and temperature - Characterization will be done over full voltage and temperature range specified
Frequency	868	902 to 928		MHz	
Frequency	400		928	MHz	Thru Mode Only, Pin#4 to Pin#19,21
RF Port Impedance		50		Ω	
ESD, Human Body Model	500			V	RF pins
ESD, Human Body Model	500			V	All other pins
ESD, Charge Device Model	500			V	RF pins
ESD, Charge Device Model	500			V	All other pins
Moisture Sensitivity Level	MSL3				
PA Section					
Transmit Mode					Pa V_{CC}, V_{DIG} = 4.2V CNTL1 = High or Low; CNTL2, 3 and 5 = Low; CNTL4 = High; T = 25°C, P_{OUT} = 26.5dBm. Unless otherwise noted.
Power Supply Operating Voltage - Electric	4	4.2	4.4	V	PA V_{CC}
Power Supply Operating Voltage – Gas/water	2.7	3.6	3.7	V	PA V_{CC}
Input Power	0		2	dBm	Pin #30
CW Output Power – near saturation	27	27.5		dBm	
Output Power - electric	26	26.5		dBm	V_{CC} = 4.2V. P_{OUT} at ANT1/2
Output Power – gas/water	24.5	25		dBm	V_{CC} = 3.6V. P_{OUT} at ANT1/2
Output Power Droop – gas/water		23		dBm	PA V_{CC} = 2.7V, P_{OUT} at ANT1/2
Current - Electric		250	300	mA	PA V_{CC} = 4.2V, P_{OUT} = +26.5dBm
Current –gas/water		210	250	mA	PA V_{CC} = 3.6V and P_{OUT} = +25dBm
Droop Current –gas/water		175	250	mA	PA V_{CC} = 2.7V, P_{OUT} at ANT1/2, P_{OUT}=23dBm
Large Signal Gain Overall	27.0	30.0	33.0	dB	P_{IN} = 0dBm at Pin#30 to ANT1/2
Second Harmonic		-30		dBc	P_{OUT}=27dBm
Third – Tenth Harmonic		-67		dBc	P_{OUT}=27dBm

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PA Section (continued)					
Input Return Loss	10			dB	Measured at PA-IN Port at Pin #30
PA Leakage Current		0.5	5	µA	PA V_{CC} = 5.0V, PD_SEL Logic = 0.0V
Noise Power at ANT1/2 – Electric Only At -8MHz Offset from carrier		-132		dBm/Hz	PA V_{CC} voltage of 4.2V and P_O = +26.5dBm, PA2 only zero noise contribution from PA1
LNA Section (LNA-IN Pin #14 to RFIO 900 Pin #2)					
HIGH GAIN Rx MODE					Pa V_{CC}, V_{DIG} = 4.2V CNTL1 = High or Low; CNTL2, 3 and 4 = High; CNTL5 = Low; T = 25°C, Unless otherwise noted.
Operating Voltage	2.7	4.2	4.4	V	LNA V_{CC}
Gain at High Bias (HB)	15.0	17.0		dB	LNA V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Gain at HB	13	15		dB	LNA V_{CC} = 2.7V; LNA Bias = High Bias
Noise Figure at HB		1.5	2.0	dB	LNA V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Noise Figure at HB		2	3	dB	LNA V_{CC} = 2.7V; LNA Bias = High Bias
Input IP3 at HB	5	8		dBm	LNA V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Input IP3 at HB	2	5		dBm	LNA V_{CC} = 2.7V; LNA Bias = High Bias
Input Return Loss	10			dB	Measured at LNA-IN Port at Pin #14
Output Return Loss	10			dB	Measured at RFIO 900 Pin #2
Power Supply Current	6	8	10	mA	
Rx LNA BYPASS MODE					Pa V_{CC}, V_{DIG} = 4.2V CNTL1 = High or Low; CNTL2 and 4 = High; CNTL3 and 5 = Low; T = 25°C, Unless otherwise noted.
Operating Voltage	2.7	4.2	4.4	V	LNA V_{CC}
Gain	-3.0	-2.5	-2.0	dB	
Noise Figure		2.5	3.0	dB	
Input IP3	12	18		dBm	
Input Return Loss	10			dB	
Output Return Loss	10			dB	
Power Supply Current		3	4	mA	
LNA Leakage Current		0.5	5	µA	LNA V_{CC} = 4.2 , PD_SEL = LOW
RF Switch Section					
Insertion Loss RFIO 900 to ISW-TX		0.4	0.5	dB	Pin #2 to Pin #32, TXRX_SEL = LOW
Insertion Loss RX-COM		0.4	0.5	dB	TXRX_SEL Logic = HIGH
Isolation RFIO 900 to ISW-TX	20	25		dB	Pin #2 to Pin #32, TXRX_SEL = HIGH
Isolation RX-COM	20	25		dB	TXRX_SEL Logic = LOW
Isolation TX-RX	20	25		dB	Tx or Rx State
ISW-COM Port Return Loss	12	15		dB	Measured at Pin #2, Tx or Rx State
ISW-TX Port Return Loss	12	15		dB	Measured at Pin #32, TXRX_SEL = LOW
Rx Return Loss	12	15		dB	TXRX_SEL Logic = HIGH

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Antenna Switch Section					
Insertion Loss TX-ANT1		1	1.2	dB	TXRX_SEL Logic = LOW , ANT_SEL Logic = HIGH
Insertion Loss TX-ANT2		1	1.2	dB	TXRX_SEL Logic = LOW , ANT_SEL Logic = LOW
Insertion Loss ANT1 - ASWRX		1	1.2	dB	TXRX_SEL Logic = HIGH , ANT_SEL Logic = HIGH
Insertion Loss ANT2 - ASWRX		1	1.2	dB	TXRX_SEL Logic = HIGH , ANT_SEL Logic = LOW
Insertion Loss RFIO 450		1	1.2	dB	RFIO 450 pin 4 to Ant1/2 at 450MHz
Insertion Loss RFIO 450		1.5	1.8	dB	RFIO 450 pin 4 to Ant1/2 at 915MHz
Isolation	20			dB	Any used port to any unused port
Tx Return Loss	10	15		dB	TXRX_SEL Logic = LOW , ANT_SEL Logic = HIGH
ANT1 Port Return Loss (Tx Mode)	8	12		dB	Measured at Pin #21, TXRX_SEL = LOW, ANT_SEL = HIGH
ANT2 Port Return Loss (Tx Mode)	8	12		dB	Measured at Pin #19, TXRX_SEL = LOW, ANT_SEL = LOW
ASWRX Port Return Loss	10	15		dB	Measured at Pin #16, TXRX_SEL = HIGH, ANT1/ANT2 State
ANT1 Port Return Loss (Rx Mode)	10	15		dB	Measured at Pin #21, TXRX_SEL = HIGH, ANT_SEL = HIGH
ANT2 Port Return Loss (Rx Mode)	10	15		dB	Measured at Pin #19, TXRX_SEL = HIGH, ANT_SEL = LOW
Logic Circuit and Power Supply Section					
VCC_DIG	2.7	4.2	4.4	V	Digital Supply Voltage. Always on
VCC_DIG Supply Current -Rx Mode		0.75	3	mA	In Any Module Rx Mode
VCC_DIG Supply Current -Tx Mode		3	6	mA	In Any Module Tx Mode
VCC_DIG Power Down Current		5	10	µA	All 5 Logic Inputs = LOW
Select Control Logic = HIGH	V_{DIG} 0.2		V_{DIG}	V	All Five (5) Logic I/O's. VDig – 0.2V
Select Control Logic = LOW	0.0		0.3	V	All Five (5) Logic I/O's
Select Control Logic High Current		5	10	µA	All Five (5) Logic I/O's
Select Control Logic Low Current		0.1	2	µA	All Five (5) Logic I/O's (sink Current)

Logic Table					
Operating Mode	**CTL1**	**CTL2**	**CTL3**	**CTL4**	**CTL5**
Tx 900 - ANT1	High	Low	Low	High	Low
Tx 900 - ANT2	Low	Low	Low	High	Low
Rx 900 ANT1 Hi gain	High	High	High	High	Low
Rx 900 ANT2 Hi Gain	Low	High	High	High	Low
Rx 900 ANT1 LNA Bypass Mode	High	High	Low	High	Low
Rx 900 ANT2 LNA Bypass Mode	Low	High	Low	High	Low
TX/RX 450 ANT1	High	High	Low	High	High
TX/RX 450 ANT2	Low	High	Low	High	High
Power Down	Low	Low	Low	Low	Low

All logic states other than defined in the above table are “undefined” and not recommended, Operation in the undefined states shall not result in permanent damage.

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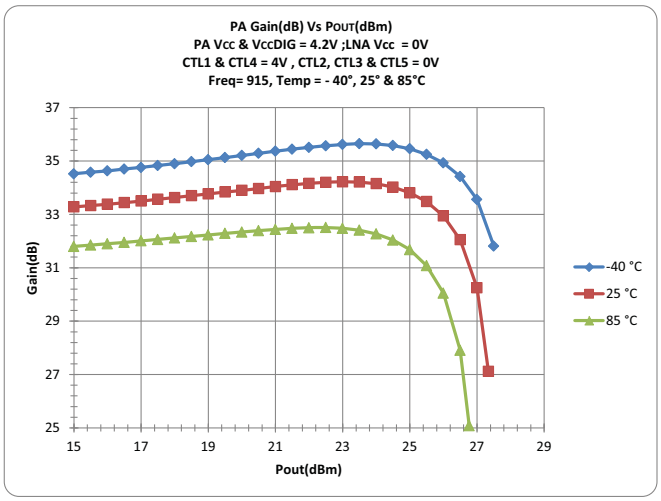
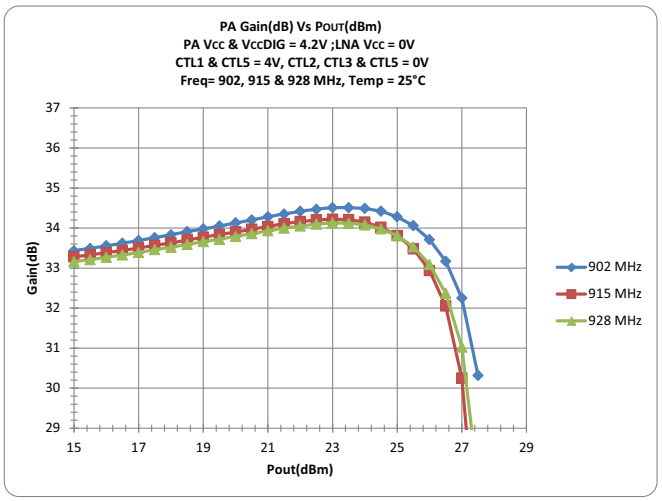
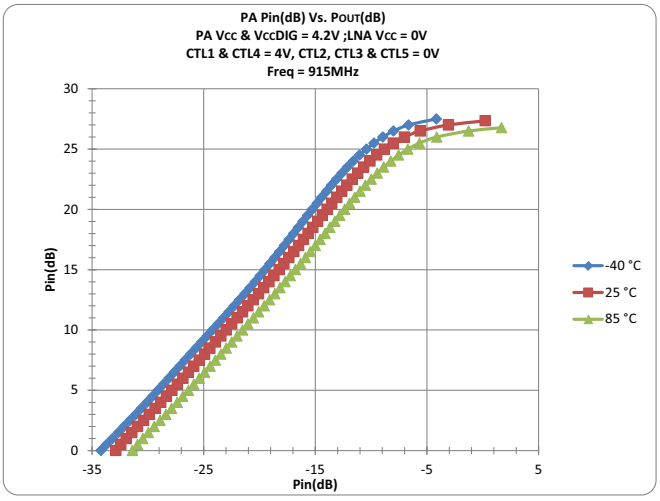
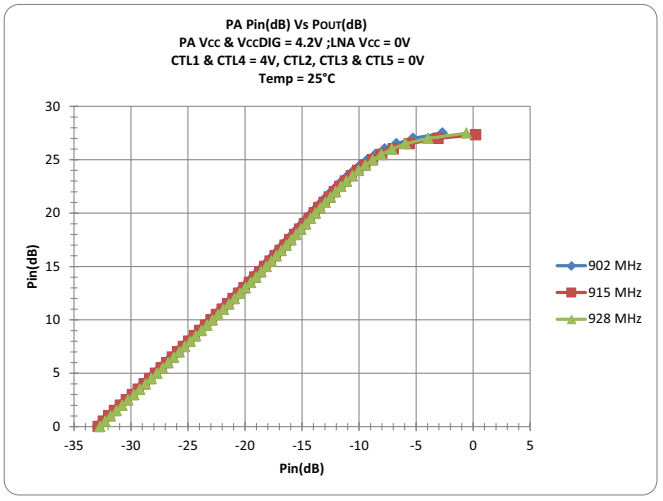
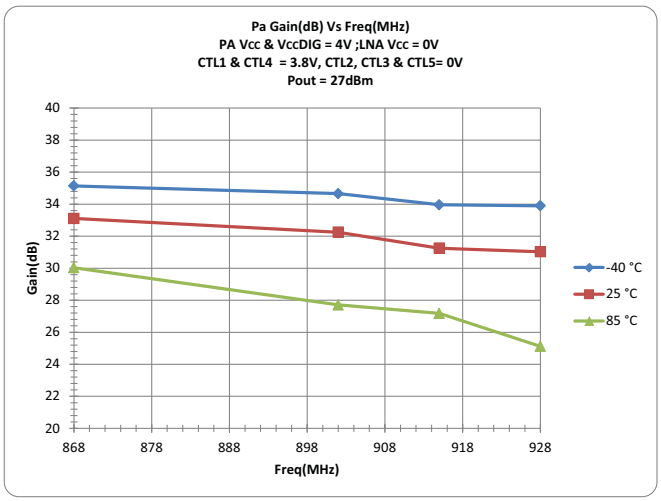
Typical Performance

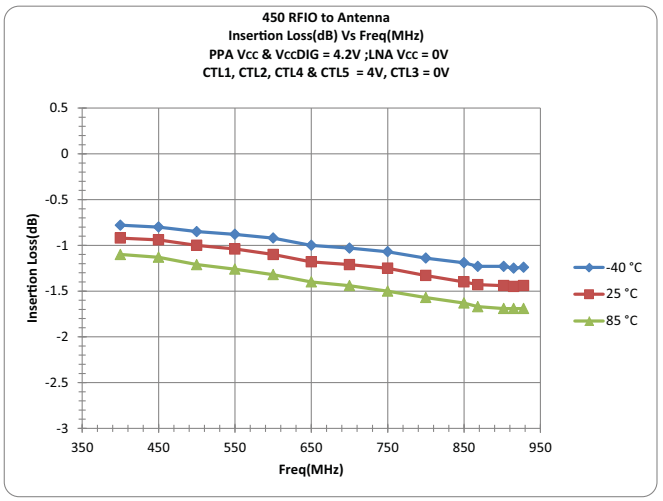












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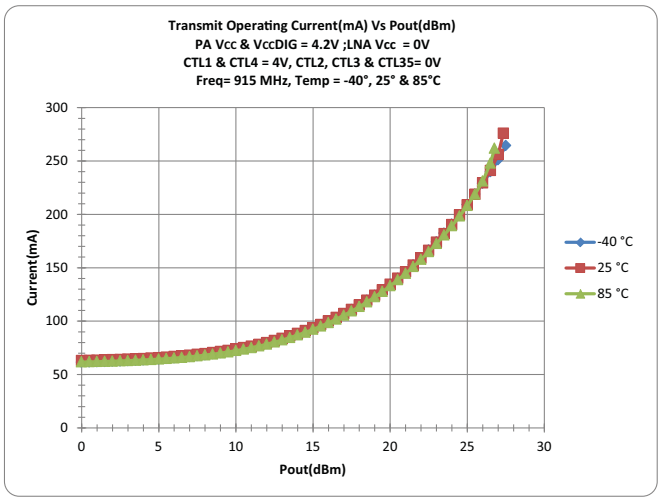

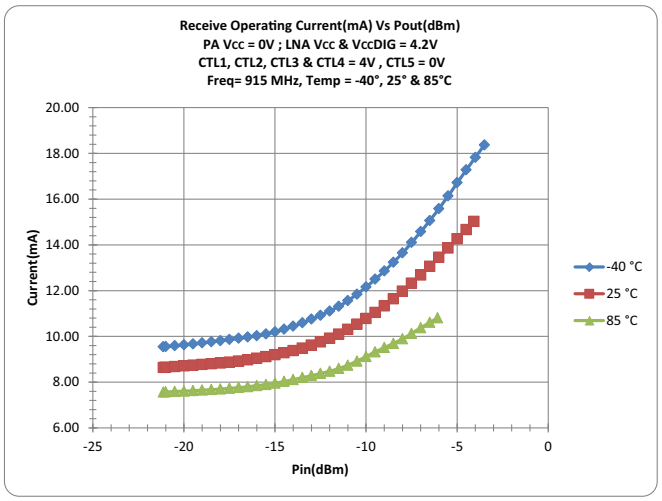

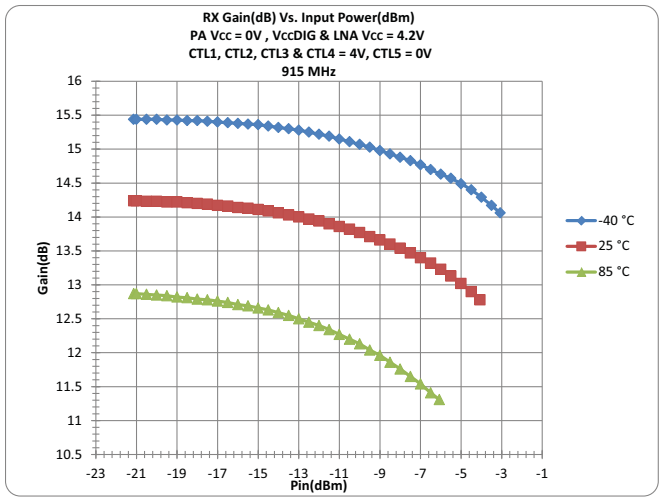

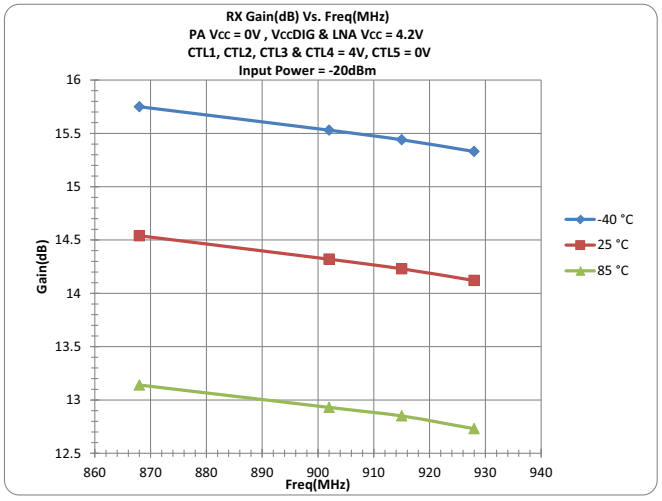

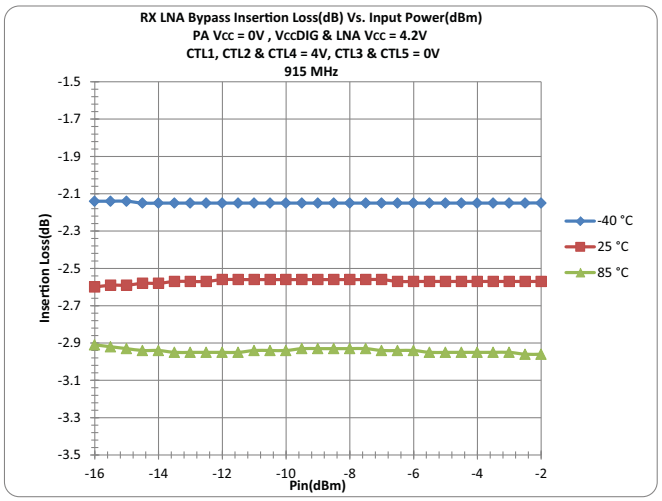

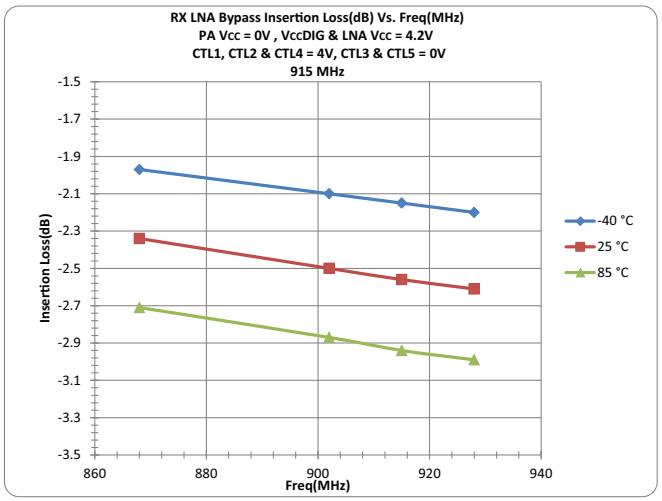

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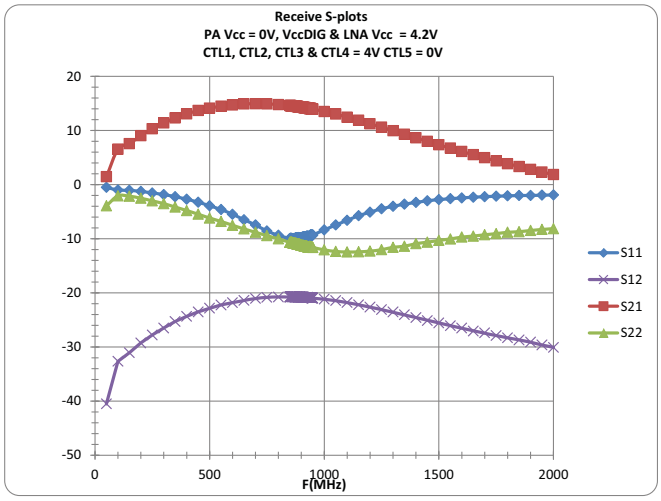

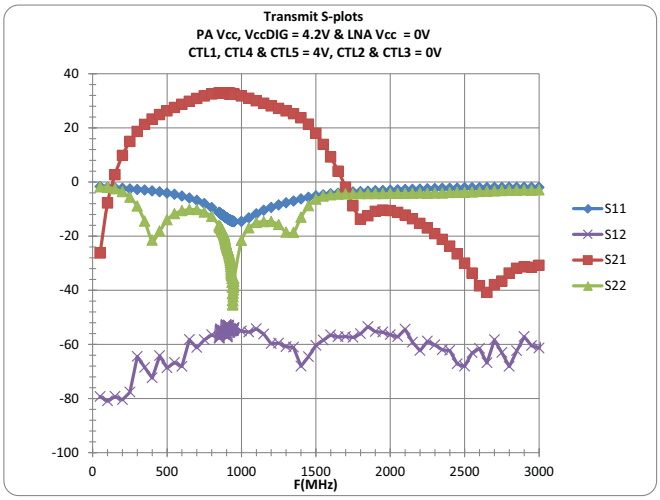

Pin Names and Description

Pin	Name	Description
1	GND	Ground I/O
2	900 RFIO	Input Switch Common Port
3	GND	Ground I/O
4	450 RFIO	Thru Path I/O
5	GND	Ground I/O Antenna 1 & Antenna 2 Select
6	CTL1	ANT Select
7	CLT2	TxRx Select
8	CTL3	LNA Select
9	CTL4	PD Select
10	CTL5	Thru Select
11	VDIG	Digital Vcc
12	LNA_VCC	LNA Vcc
13	LNA_BIAS	LNA linearity bias
14	LNA_IN	LNA Signal Input
15	GND	Ground I/O
16	ASW_RX	Antenna Switch Receive Output
17	GND	Ground I/O
18	GND	Ground I/O
19	ANT2	Antenna 2 Output/Input
20	GND	Ground I/O
21	ANT1	Antenna 1 Output/Input
22	GND	Ground I/O
23	PA VCC2	PA Battery Bias for Second Stage
24	PA VCC1	PA Battery Bias for First Stage
25	GND	Ground I/O
26	PA2_IN	Power Amplifier 2nd Stage Signal Input Port
27	GND	Ground I/O
28	PA1_OUT	Power Amplifier 1st Stage Signal Output Port
29	GND	Ground I/O
30	PA1_IN	Power Amplifier 1st Stage Signal Input Port
31	GND	Ground I/O
32	SW2_OUT	Input switch Tx Out

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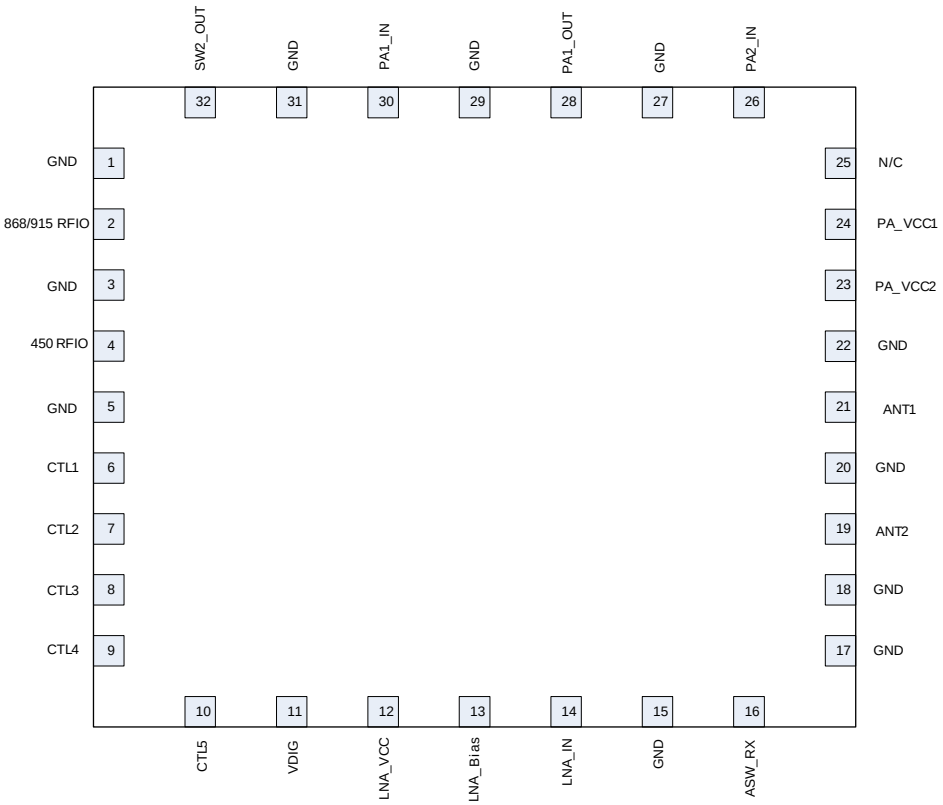
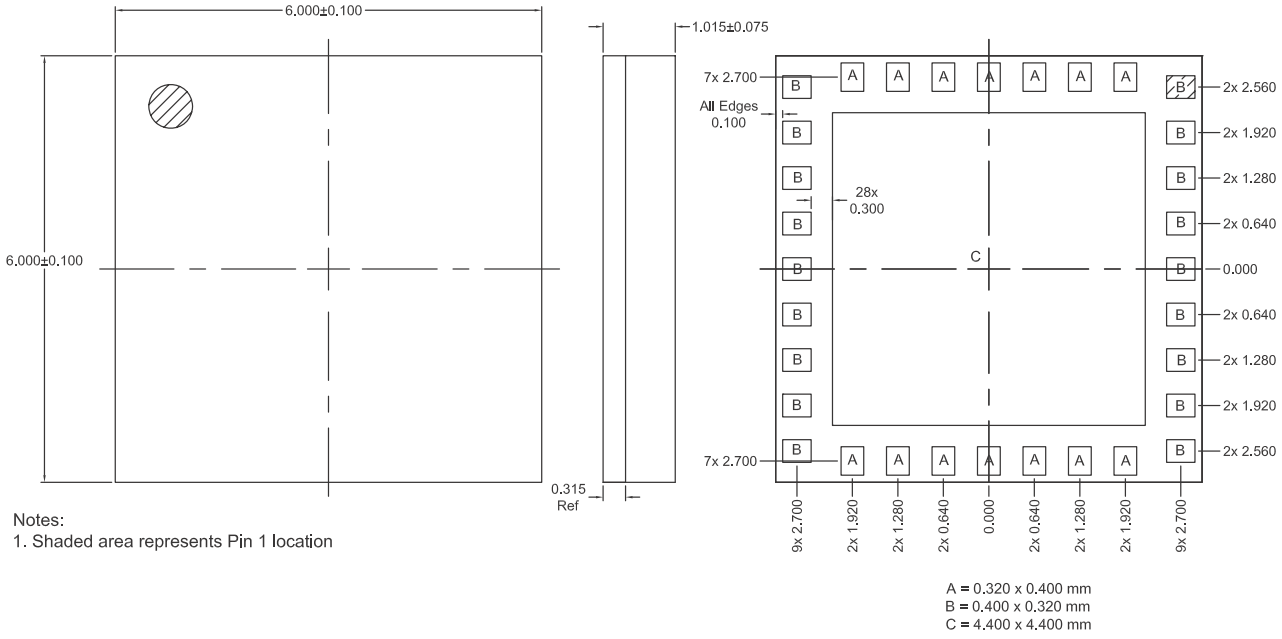
Pin Out



Package Drawing



Notes:
1. Shaded area represents Pin 1 location

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PCB Design Requirements

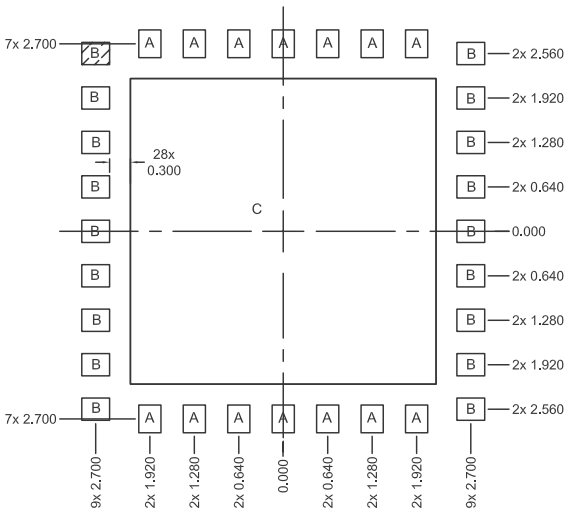
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

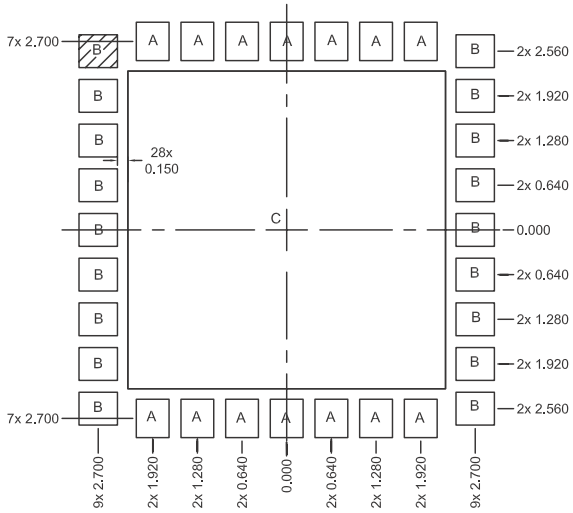
PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



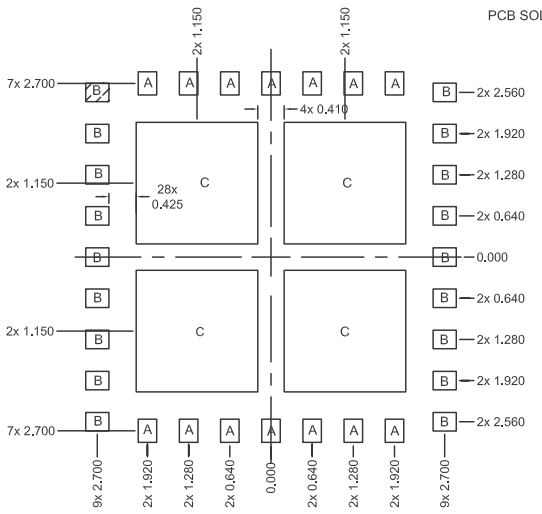
A = 0.320 x 0.400 mm
B = 0.400 x 0.320 mm
C = 4.400 x 4.400 mm

PCB M ETAL PATTERN



A = 0.470 x 0.550 mm
B = 0.550 x 0.470 mm
C = 4.550 x 4.550 mm

PCB SOLDER MASK PATTERN



A = 0.288 x 0.360 mm
B = 0.360 x 0.288 mm
C = 1.890 x 1.890 mm

PCB STENCIL PATTERN

Notes:
1. Shaded area represents Pin 1 location

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