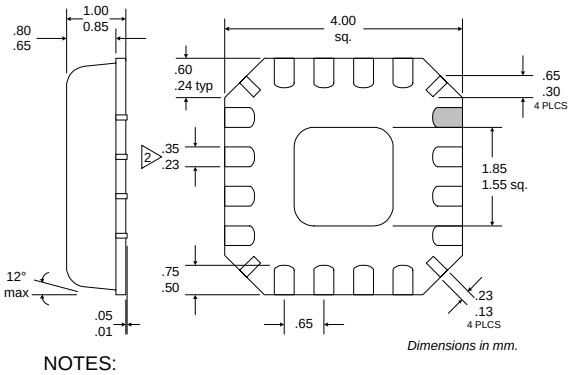
Typical Applications

- W-CDMA Systems
- EDGE Systems
- CDMA Systems
- TDMA Systems

Product Description

The RF9678 is an integrated complete quadrature modulator and IF AGC amplifier designed for the transmit section of W-CDMA applications. It is designed to modulate baseband I and Q signals, and amplify the resulting IF signals while providing 55dB of gain control range. This circuit is designed as part of RFMD's single mode W-CDMA Chipset, which also includes the RF2679 W-CDMA Receive IF AGC and Demodulator. The IC is manufactured on an advanced Silicon Bi-CMOS process, and is supplied in a16-pin leadless chip carrier.



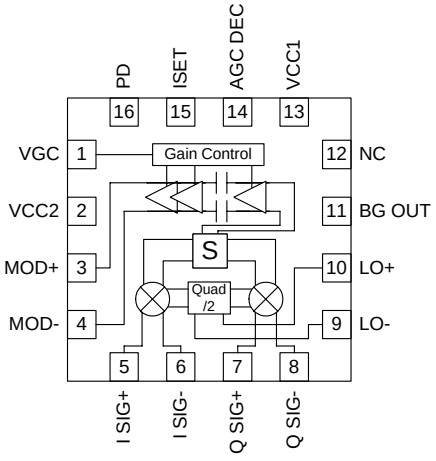
NOTES:

1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.02 mm and 0.25 mm from terminal end.
3. Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
4. Package Warpage: 0.05 max.
5. Die thickness allowable: 0.305 mm max.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS

Package Style: LCC, 16-Pin, 4x4



Functional Block Diagram

Features

- Digitally Controlled Power Down Modes
- 2.7V to 3.3V Operation
- Digital LO Quadrature Divider
- AGC Linearity/Current Consumption Var.
- IF AGC Amp with 55dB Gain Control

Ordering Information

RF9678	W-CDMA Transmit Modulator and IF AGC
RF9678 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
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http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC} + 0.7	V
I and Q Levels, per pin	1.2	V_{PP}
LO1 Level, balanced	+3	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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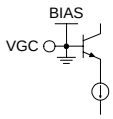
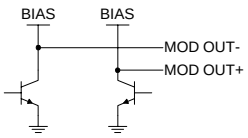
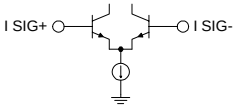
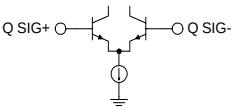
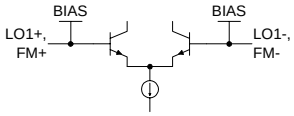
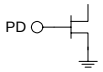
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.0V; Z_{LOAD}=200Ω; I=Q=500mV$_{PP}$, 1000mV$_{PP}$ Differential; Output externally matched
I/Q Input Frequency Range		0 to 10		MHz	Balanced
I/Q Input Impedance		20		kΩ	Balanced
I/Q Input Reference Level		1.3		V_{DC}	Per Pin
LO1 Frequency Range		0 to 1200		MHz	
LO1 Input Level	-15	-8	-5	dBm	Specifications
LO1 Input Impedance		200		Ω	Balanced (Evaluation Board Schematic)
		2		kΩ	Balanced, IC input
Sideband Suppression	45	50		dBc	I/Q Amplitude adjusted to within ±20mV
	25	30		dBc	Unadjusted
Carrier Suppression	45	50		dBc	I/Q DC Offset adjusted to within ±20mV
	20	28		dBc	Unadjusted
IF=380MHz					I=Q=500mV$_{PP}$, 1000mV$_{PP}$ Differential; LO1=760MHz; Output externally matched
Max Output Power, W-CDMA Mode	-6	-4.5	-3	dBm	W-CDMA ACPR=-50dBc, V_{GC}=2.4V_{DC}, T=-20°C to +85°C
Min Output Power, CDMA Mode	-63	-59	-56	dBm	V_{GC}=0.2V_{DC}
Output Power Accuracy	-3		+3	dB	T=-20 to +85 °C, Ref=25 °C
Adjacent Channel Power Rejection @ 5MHz			-46	dBc	W-CDMA Modulation, V_{GC}=0.2V_{DC} to 2.4V_{DC}
Adjacent Channel Power Rejection @ 10MHz			-56	dBc	W-CDMA Modulation, V_{GC}=0.2V_{DC} to 2.4V_{DC}
Output Noise Power		-135		dBm/Hz	@ 20MHz offset, V_{GC}=2.4V_{DC}
Output Impedance		200		Ω	Balanced
IF=570MHz					I=Q=700mV$_{PP}$, 1400mV$_{PP}$ Differential; LO1=1140MHz; Output externally matched
Max Output Power, W-CDMA Mode		-4		dBm	W-CDMA ACPR=-50dBc, V_{GC}=2.4V_{DC}, T=-20°C to +85°C
Adjacent Channel Power Rejection @ 5MHz			-46	dBc	W-CDMA Modulation, V_{GC}=0.2V_{DC} to 2.4V_{DC}
Adjacent Channel Power Rejection @ 10MHz			-56	dBc	W-CDMA Modulation, V_{GC}=0.2V_{DC} to 2.4V_{DC}
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption	30	39	46	mA	Over temperature
Power Down Current			<10	µA	
V_{PD} HIGH Voltage	V_{CC}-1.0			V	
V_{PD} LOW Voltage			0.9	V	
Gain Control Range	0.2		2.4	V	
V_{GC} Current			40	µA	

Pin	Function	Description	Interface Schematic
1	VGC	Analog gain control for AGC amplifiers. Valid control voltage ranges are from 0.2V_{DC} to 2.4V_{DC}. The gain range for the AGC is 55dB. These voltages are valid ONLY for a 39kΩ source impedance. A DC voltage less than or equal to the maximum allowable V_{CC} may be applied to this pin when no voltage is applied to the V_{CC} pins.	
2	VCC2	DC supply. This pin should be bypassed to ground with a 10nF capacitor.	
3	MOD+	Same as pin 4, except complementary output.	See pin 4.
4	MOD-	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. This pin requires an inductor to V_{CC} to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
5	I SIG+	One half of the balanced baseband input to the I mixer. This pin is DC-coupled and must be supplied with 1.3VDC to bias the input transistor. Input impedance of this pin is 10kΩ minimum. For maximum carrier suppression, DC voltage on this pin relative to ISIG- DC voltage may be adjusted. (In case a balun is needed, a seperate balun board (RD0102 PCBA) could be ordered as an accessory.)	See pin 8.
6	I SIG-	One half of the balanced baseband input to the I mixer. This pin is DC-coupled and must be supplied with 1.3VDC to bias the input transistor. Input impedance of this pin is 10kΩ minimum. For maximum carrier suppression, DC voltage on this pin relative to ISIG+ DC voltage may be adjusted.	
7	Q SIG+	One half of the balanced baseband input to the Q mixer. This pin is DC-coupled and must be supplied with 1.3VDC to bias the input transistor. Input impedance of this pin is 10kΩ minimum. For maximum carrier suppression, DC voltage on this pin relative to QSIG- DC voltage may be adjusted.	See pin 10.
8	Q SIG-	One half of the balanced baseband input to the Q mixer. This pin is DC-coupled and must be supplied with 1.3VDC to bias the input transistor. Input impedance of this pin is 10kΩ minimum. For maximum carrier suppression, DC voltage on this pin relative to QSIG+ DC voltage may be adjusted.	
9	LO-	One half of the balanced modulator LO1 input. In single-ended applications (100Ω input impedance), this pin is AC grounded with a 1nF capacitor.	See pin 10.
10	LO+	One half of the balanced modulator LO1 input. The other half of the input, LO1-, is AC grounded for single-ended input applications. The frequency on these pins is divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 1kΩ (balanced is 2kΩ). This pin is NOT internally DC blocked. An external blocking capacitor (1nF recommended) must be provided if the pin is connected to a device with DC present.	
11	BG OUT	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 10nF external bypass capacitor is required.	
12	NC	No connection.	
13	VCC1	DC supply. This pin should be bypassed to ground with a 10nF capacitor.	
14	AGC DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

Pin	Function	Description	Interface Schematic
15	ISET	Connected to ground through an external resistor. The value can be varied to change the current in the AGC for optimum linearity and current consumption.	
16	PD	Power down control for overall circuit. When logic "high" ($\geq V_{CC}$-0.7V), all circuits are operating; when logic "low" ($\leq$0.5V), all circuits are turned off. The input impedance of this pin is >10kΩ. A DC voltage less than or equal to the maximum allowable V_{CC} may be applied to this pin when no voltage is applied to the V_{CC} pins.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

Application Notes

Quadrature modulator performance can be correlated to a set of specifications known as Carrier and Sideband Suppression. In addition, Sideband Suppression can be correlated with the amplitude and phase balance of the In-Phase (I) and Quadrature (Q) signals and Carrier Suppression can be correlated to the DC offset between the I and Q signals (see Figure 1). For a more thorough discussion of the theory and mathematics behind these specifications refer to RF Micro Devices application note AN0001.

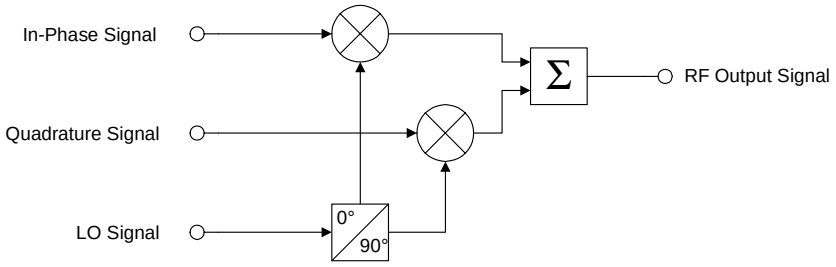


Figure 1. Quadrature Modulator Block Diagram

Effects of Carrier Suppression and Sideband Suppression on W-CDMA (QPSK) Modulation

W-CDMA signals may be displayed on a vector signal analyzer as a collection of points called a constellation. Each point in the constellation is called a symbol and is representative of a bit sequence. In QPSK modulation, there are four symbols and each symbol is representative of two data bits (see Figure 2). The I and Q signals are added together to create a vector of precise phase and amplitude. The vector is then sampled at a rate called the symbol rate and it's position at these intervals corresponds to the target symbol locations. Errors in the phase and amplitude of the I and Q signals will translate to errors in the vector's phase and amplitude. This phase and amplitude error will result in a displacement of the vector from it's target symbol point. A measurement of this error is called the Error Vector Magnitude (EVM) and it represents the magnitude of the displacement of the actual vector from it's target location.

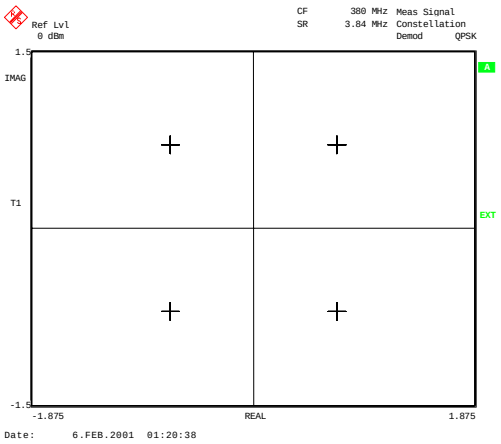


Figure 2. W-CDMA (QPSK) Constellation

QPSK constellation points exist on a circle of constant radius around the origin. Amplitude errors result in symbol points being displaced either inside or outside of their target locations on this circle. Phase errors result in symbol points being displaced on an arc either to the left or right of their target location. Finally, DC offset errors cause the origin to shift, resulting in a constant I and Q offset of all target points (see Figure 3).

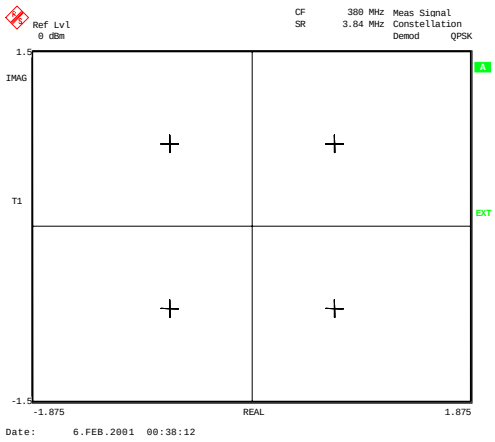


Figure 3. DC Offset Error (Carrier Feedthrough)

As is shown above, the EVM performance of a modulator can be correlated to it's carrier and sideband suppression performance.

Unadjusted Performance

A Wideband CDMA signal is a noise-like signal occupying a channel bandwidth of 3.84 MHz. When viewed on a spectrum analyzer the channel appears as a plateau raised above the noise floor (see Figure 4). In some cases, it is normal to see a spike over the center of the W-CDMA plateau. This will occur when the absolute power level of the unadjusted carrier feedthrough is higher than that of the W-CDMA channel level. The cause of this phenomenon can be understood by examining the relative powers of the carrier signal and the W-CDMA channel power.

For Example, a 1 Hz channel with a power of 0 dBm has an absolute power level of 0 dBm when viewed on a spectrum analyzer. When that 0 dBm channel power is spread over a 3.84 MHz channel, as in W-CDMA, it results in an absolute channel power level of -65.8 dBm (-10*log (BW)). The absolute channel level displayed on the spectrum analyzer will increase with the resolution bandwidth setting on the instrument although the integrated channel power will remain constant. A resolution bandwidth (RBW) of 30 kHz will increase the displayed power level by 44.7 dB (+10*log(RBW)) to -21.0 dBm. With a desired signal output power of +2.0 dBm and a carrier suppression of >20 dBc, the absolute carrier level can be as high as -18.0 dBm (P_{OUT}-Suppression=Carrier Level). This will result in a 3 dB carrier spike above the W-CDMA channel level (see Figure 4). (Note: The relative height of the carrier spike above the W-CDMA channel level is directly related to the RBW of the spectrum analyzer being used. The example above assumes a 30 kHz RBW.)

The following equations may be used to calculate W-CDMA channel and carrier feedthrough levels.

W-CDMA Channel Level=Channel Power (Integrated over BW)-[10*log*(BW)]+[10*log*(RBW)]

Carrier Feedthrough=P_{OUT} (Desired Sideband)-Carrier Suppression

The next section describes a procedure that may be used to dramatically reduce carrier feedthrough by tuning or optimizing the modulator input signals.

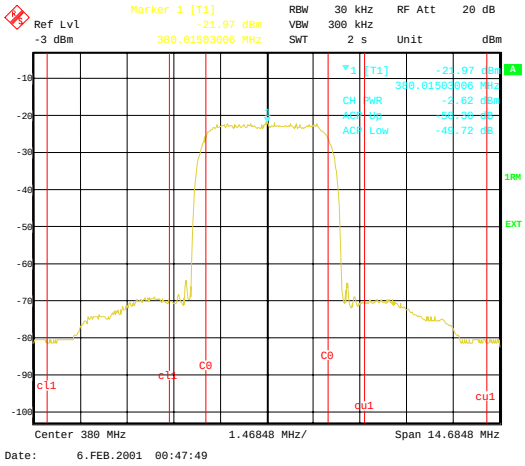


Figure 4. W-CDMA Spectral Plot

Adjusted Performance

In theory, an ideal quadrature modulator will completely suppress the carrier and sideband signals. In practice, due to process and packaging effects, real quadrature modulators lack the balance necessary to completely cancel the carrier and sideband signals. The imbalance caused by process and packaging effects is usually very small and may be corrected by preadjusting the input signals to the modulator. This process of adjusting the input signals to minimize the carrier and sideband suppression is known as optimization.

Sideband suppression results from the summing together of the I and Q channel mixer outputs. In an ideal quadrature modulator, at the summing point the sideband signals from the I and Q mixers are 180° out of phase and have equal magnitudes. In a real modulator, the amplitude and phase are not exactly balanced and 100% cancellation does not occur. The problem is corrected by introducing amplitude and phase corrections before applying a signal to the modulator. Maximum sideband suppression is achieved when the amplitude and phase errors introduced by the modulator are compensated for.

Complete carrier suppression occurs when there is no DC offset between the mixer signal input and the mixer reference voltage (i.e., ISIG+ and ISIG-). In real devices, zero DC offset is difficult to achieve. This problem is corrected by introducing a DC offset of equal and opposite magnitude before applying the signal to the modulator. The internal error is thereby canceled and maximum carrier suppression is achieved.

Procedure for RF9678 Quadrature Modulator/AGC Optimization

1) Configure the test bench as shown in Figure 5.

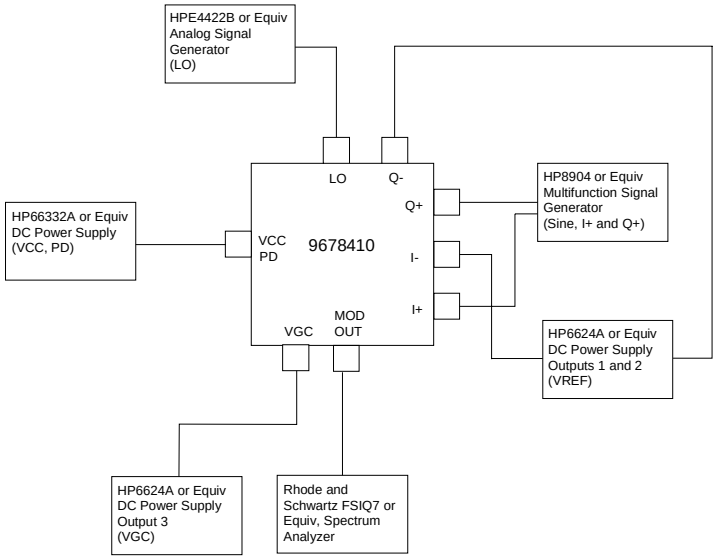


Figure 5. RF9678 Test Setup

2) Apply V_{CC} to the part. (V_{CC}=3.0V)

3) Set gain control to maximum. (V_{GC}=2.4V)

4) Apply the LO signal. (760MHz@-5dBm, for an IF out of 380MHz)

5) Apply the I+ and Q+ signals: (Single Ended)
I Signal: 150kHz@ 500mVp, Phase=0°, 1.3V DC Offset
Q signal: 150kHz@ 500mVp, Phase =90°, 1.3V DC Offset

6) Set the DC levels at I_{SIG}- and Q_{SIG}- input pins to the nominal value (1.3V). The output spectrum should look similar to Figure 6.

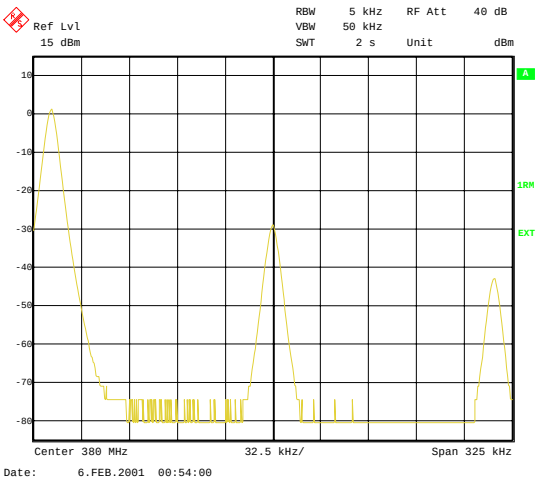


Figure 6. Unassigned Single Sideband Output

Carrier Suppression Optimization

7) While maintaining a constant DC level (1.3V) on the "ISIG-" pin, adjust the DC level of the "ISIG+" input in as small an increment (~1.0mV) as the test equipment will allow. Observe the output on the spectrum analyzer. Adjust the DC level until the carrier signal is at a minimum. Typically, the minimum will occur within a ±20mV window of the reference voltage (1.3±0.02V).

8) While maintaining a constant DC level (1.3V) on the "QSIG-" pin, adjust the DC level of the "QSIG+" input in as small an increment as the test equipment will allow (1.0mV). Observe the output on the spectrum analyzer. Adjust the DC level until the carrier signal is at a minimum. Typically, the minimum will occur within a ±20mV window of the reference voltage (1.3±0.02V).

9) Repeating Steps 7 and 8 may yield slightly better suppression. The output spectrum should look similar to Figure 7. (Note the suppressed carrier signal.)

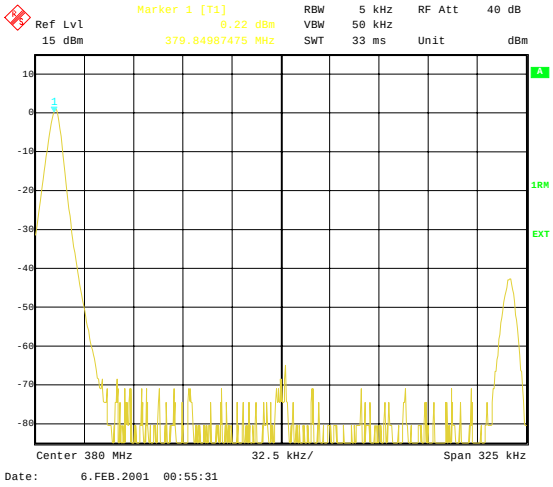


Figure 7. Optimized Carrier Suppression

Sideband Suppression Optimization

10) Adjust the AC amplitude of the "ISIG+" signal in as small an increment as the test equipment will allow (~1mV). Observe the output of the spectrum analyzer. Adjust the AC amplitude of the signal until the sideband signal is at a minimum. The minimum sideband signal level should occur within ±20mV adjustment. (0.500±0.02V)

11) Adjust the AC amplitude of the "QSIG+" signal in as small an increment as the test equipment will allow (~1mV). Observe the output of the spectrum analyzer. Adjust the AC amplitude of the signal until the sideband signal is at a minimum. The minimum sideband signal level should occur within ±20mV adjustment (0.500±0.02V).

12) Adjust the phase of the "QSIG+" signal in as small an increment as the test equipment will allow (`0.1°). Observe the output of the spectrum analyzer. Adjust the phase of the "QSIG+" signal until the sideband suppression is at a minimum. The sideband signal should reach a minimum within ±1° of adjustment (90±1°).

13) The device is now optimized for maximum carrier and sideband suppression. The output spectrum should look similar to Figure 8. (Note the suppressed carrier and sideband signals.)

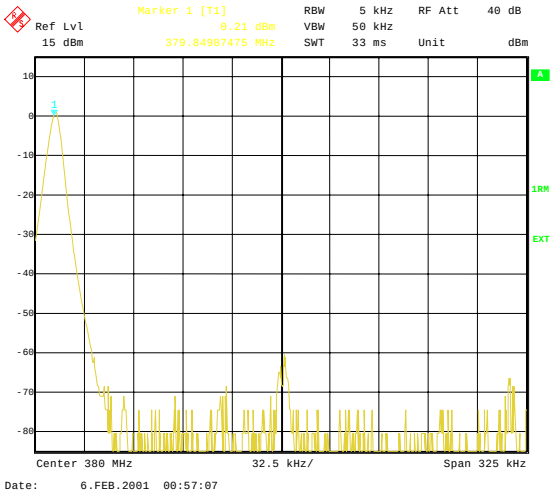
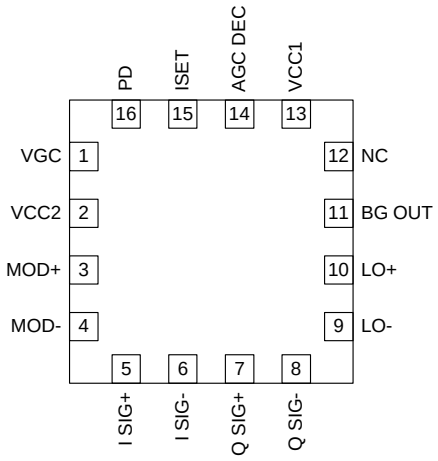
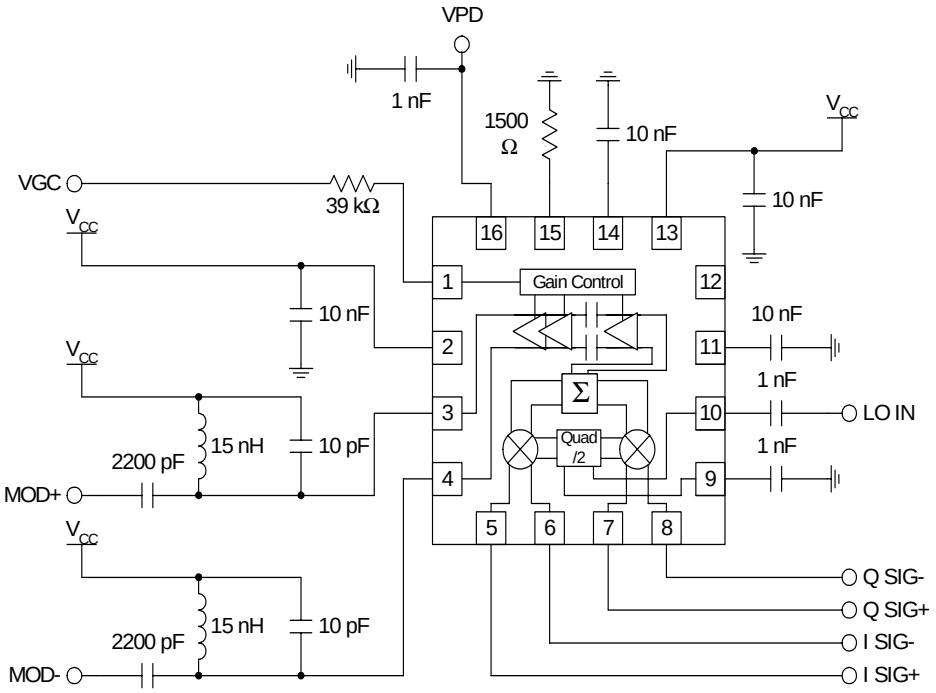


Figure 8. Optimized Carrier and Sideband Suppression

Pin Out



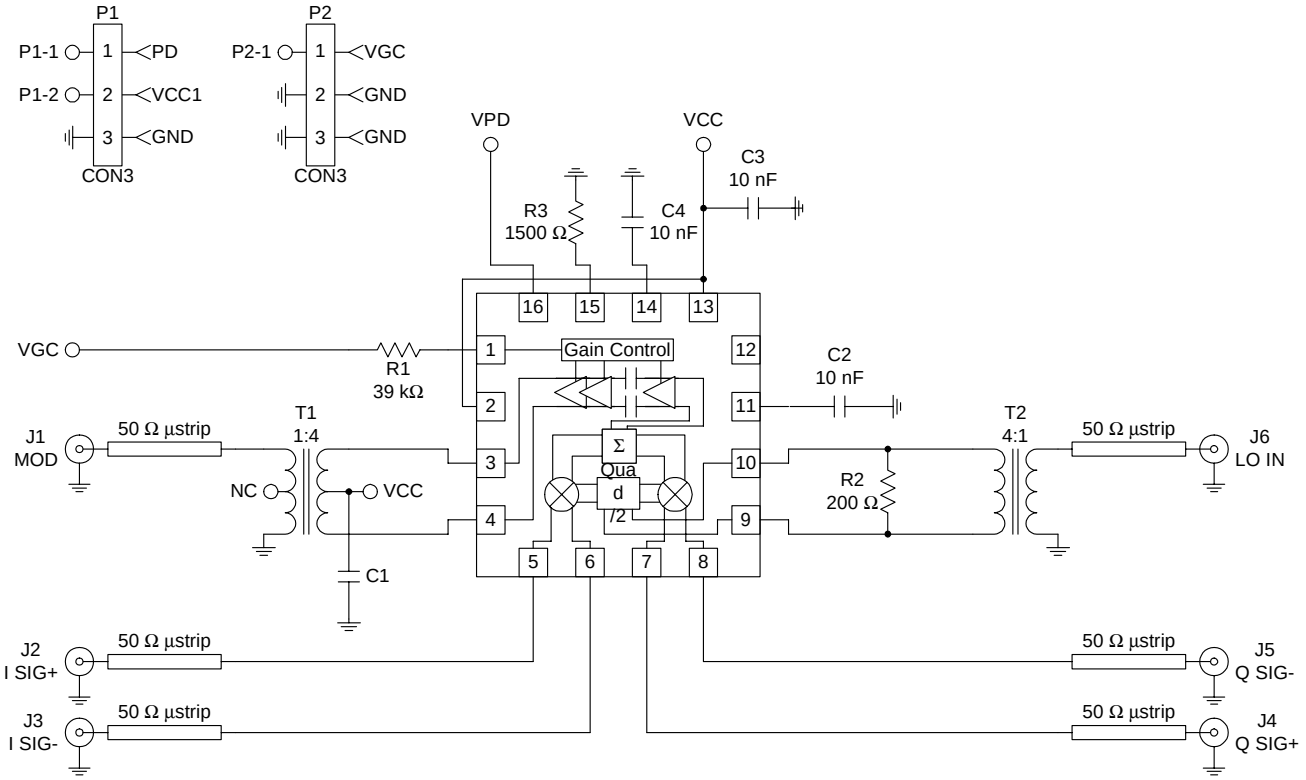
Application Schematic



5 MODULATORS AND UPCONVERTERS

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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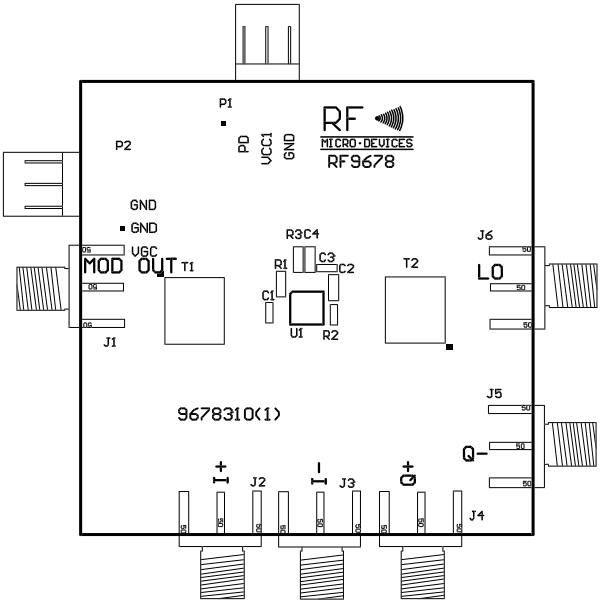
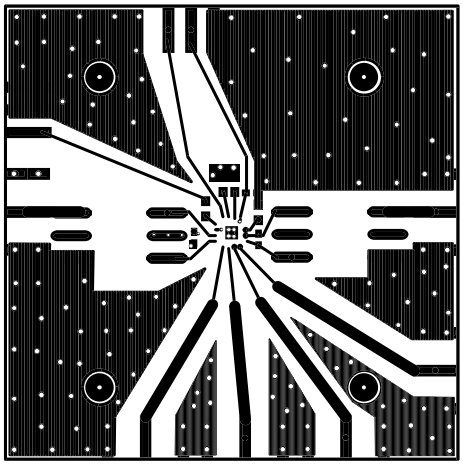
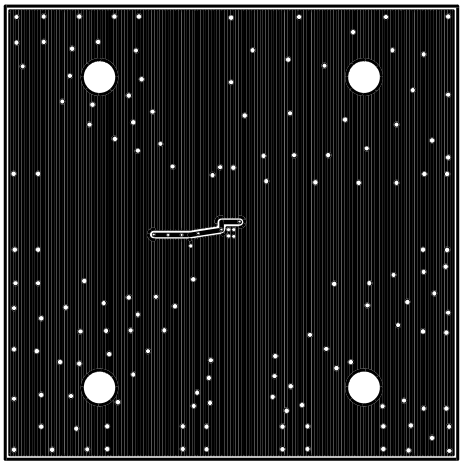
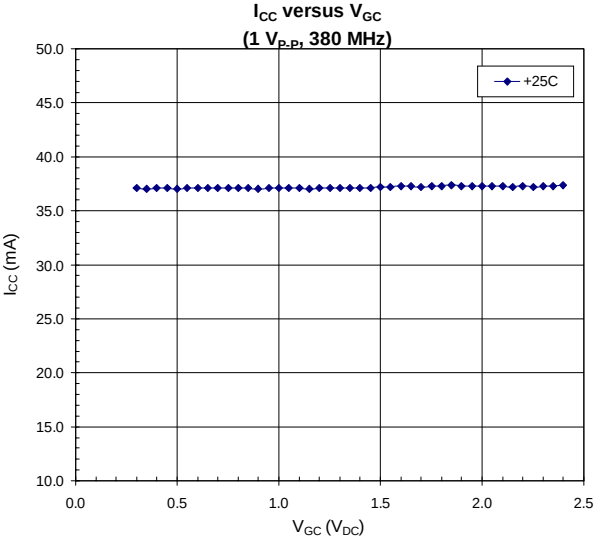
MODULATORS AND UPCONVERTERS

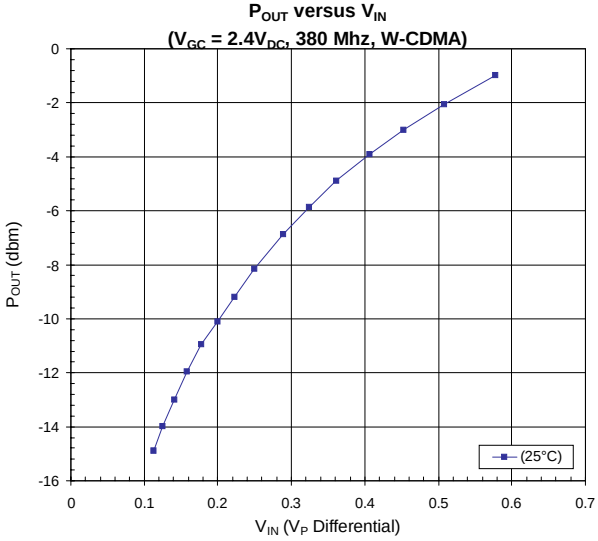
Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.031”, Board Material FR-4

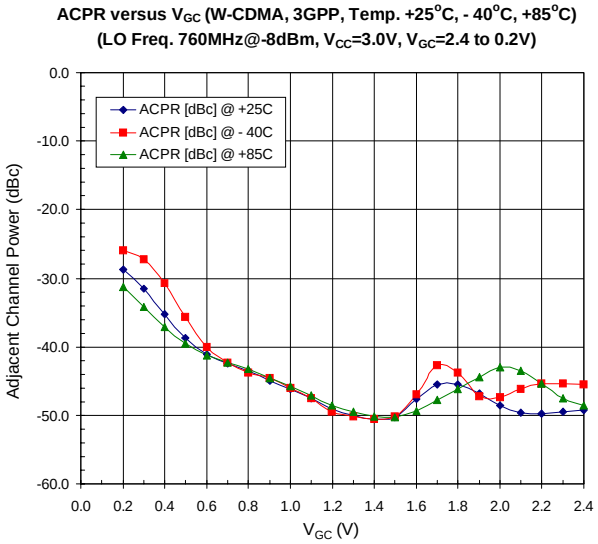


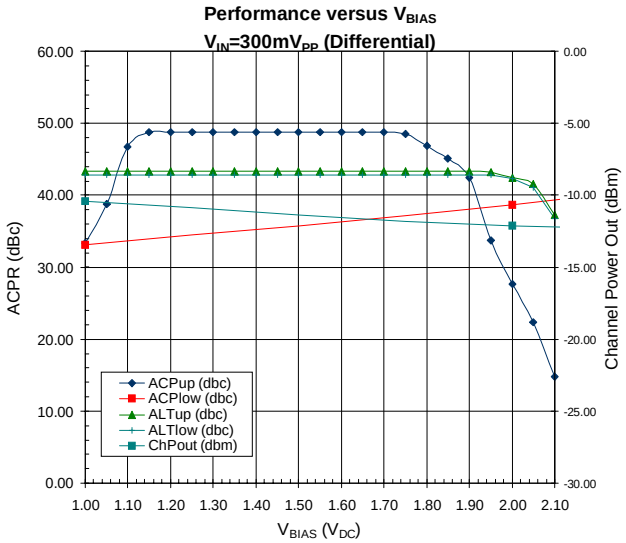


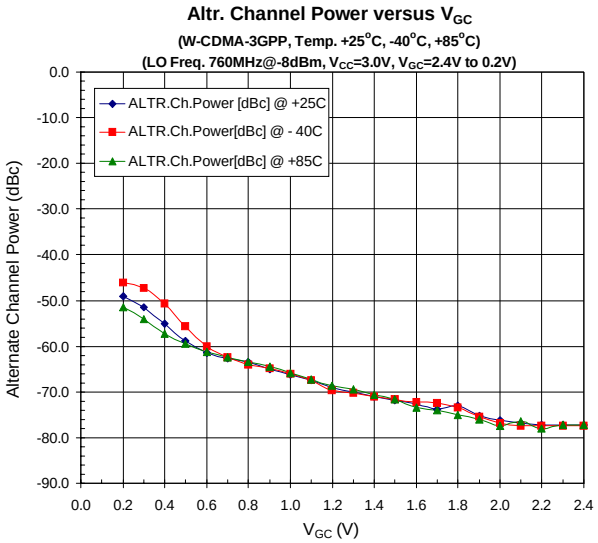


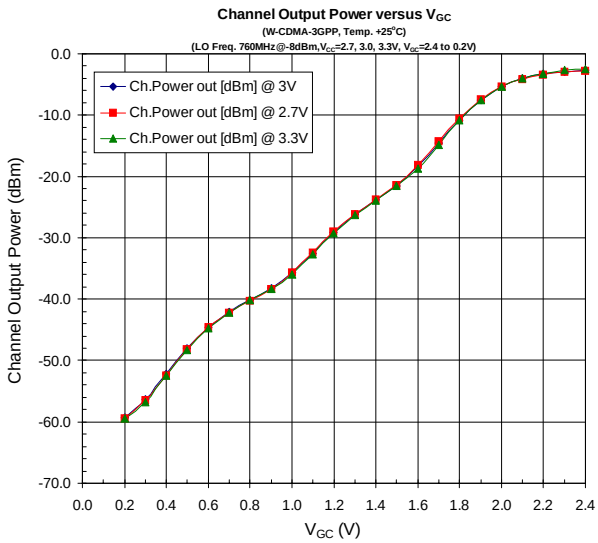

I_{CC} versus V_{GC}
(1 V_{P-P}, 380 MHz)
+25C
I_{CC} (mA)
V_{GC} (V_{DC})

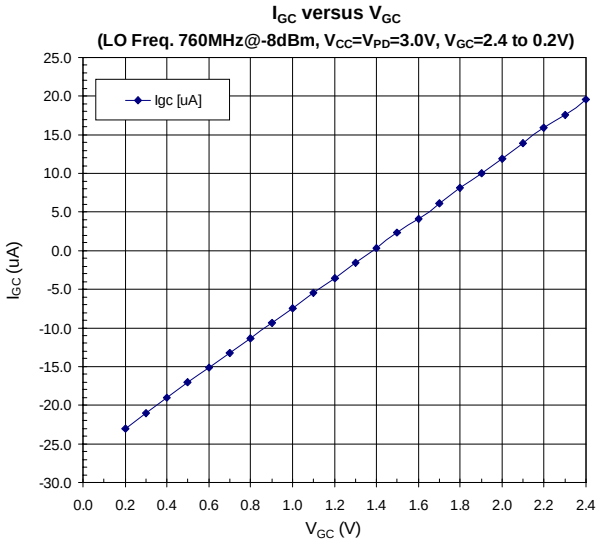

P_{OUT} versus V_{IN}
(V_{GC} = 2.4V_{DC}, 380 Mhz, W-CDMA)
(25°C)
P_{OUT} (dbm)
V_{IN} (V_P Differential)

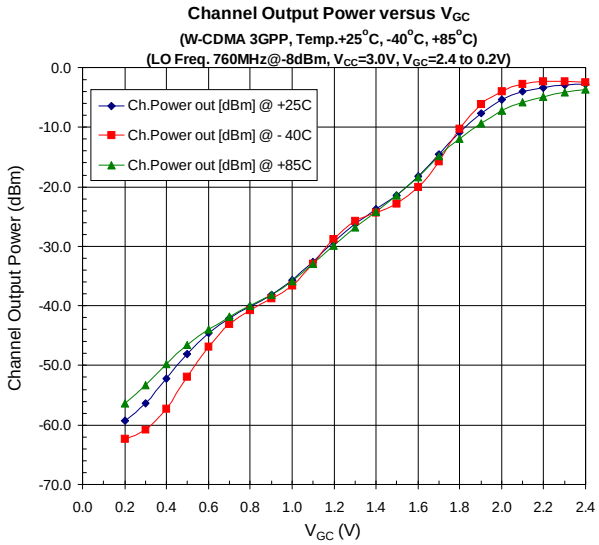

ACPR versus V_{GC} (W-CDMA, 3GPP, Temp. +25°C, - 40°C, +85°C)
(LO Freq. 760MHz@-8dBm, V_{CC}=3.0V, V_{GC}=2.4 to 0.2V)
ACPR [dBc] @ +25C
ACPR [dBc] @ - 40C
ACPR [dBc] @ +85C
Adjacent Channel Power (dBc)
V_{GC} (V)

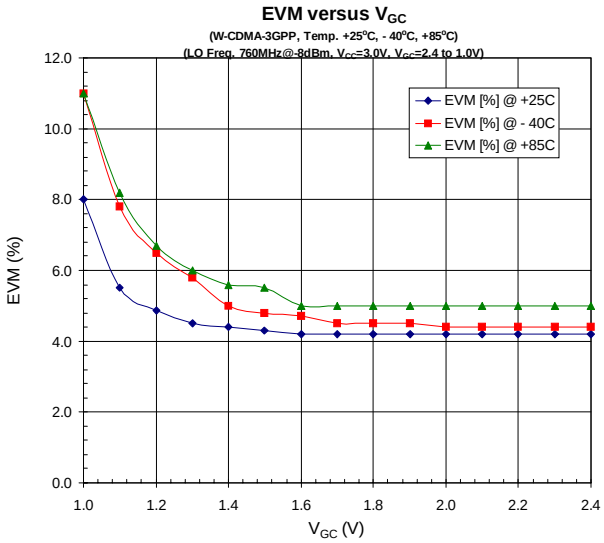

Performance versus V_{BIAS}
V_{IN}=300mV_{PP} (Differential)
ACPup (dbc)
ACPlow (dbc)
ALTup (dbc)
ALTlow (dbc)
ChPout (dbm)
ACPR (dBc)
Channel Power Out (dBm)
V_{BIAS} (V_{DC})


Altr. Channel Power versus V_{GC}
(W-CDMA-3GPP, Temp. +25°C, -40°C, +85°C)
(LO Freq. 760MHz@-8dBm, V_{CC}=3.0V, V_{GC}=2.4V to 0.2V)
ALTR.Ch.Power [dBc] @ +25C
ALTR.Ch.Power[dBc] @ - 40C
ALTR.Ch.Power[dBc] @ +85C
Alternate Channel Power (dBc)
V_{GC} (V)


Channel Output Power versus V_{GC}
(W-CDMA-3GPP, Temp. +25°C)
(LO Freq. 760MHz@-8dBm,V_{CC}=2.7, 3.0, 3.3V, V_{GC}=2.4 to 0.2V)
Ch.Power out [dBm] @ 3V
Ch.Power out [dBm] @ 2.7V
Ch.Power out [dBm] @ 3.3V
Channel Output Power (dBm)
V_{GC} (V)


I_{GC} versus V_{GC}
(LO Freq. 760MHz@-8dBm, V_{CC}=V_{PD}=3.0V, V_{GC}=2.4 to 0.2V)
Igc [uA]
I_{GC} (uA)
V_{GC} (V)


Channel Output Power versus V_{GC}
(W-CDMA 3GPP, Temp.+25°C, -40°C, +85°C)
(LO Freq. 760MHz@-8dBm, V_{CC}=3.0V, V_{GC}=2.4 to 0.2V)
Ch.Power out [dBm] @ +25C
Ch.Power out [dBm] @ - 40C
Ch.Power out [dBm] @ +85C
Channel Output Power (dBm)
V_{GC} (V)


EVM versus V_{GC}
(W-CDMA-3GPP, Temp. +25°C, - 40°C, +85°C)
(LO Freq. 760MHz@-8dBm, V_{CC}=3.0V, V_{GC}=2.4 to 1.0V)
EVM [%] @ +25C
EVM [%] @ - 40C
EVM [%] @ +85C
EVM (%)
V_{GC} (V)