

# RFL1N12L, RFL1N15L

1A, 120V and 150V, 1.900 Ohm,  
Logic Level, N-Channel Power MOSFETs

September 1998

## Features

- 1A, 120V and 150V
- $r_{DS(ON)} = 1.900\Omega$

## Ordering Information

PART NUMBER	PACKAGE	BRAND
RFL1N12L	TO-205AF	RFL1N12L
RFL1N15L	TO-205AF	RFL1N15L

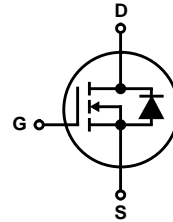
NOTE: When ordering, use the entire part number.

## Description

These are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

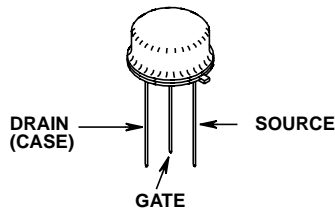
Formerly developmental type TA09528.

## Symbol



## Packaging

JEDEC TO-205AF



## RFL1N12L, RFL1N15L

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFL1N12L	RFL1N15L	UNITS	
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$	120	150	V
Drain to Gate Voltage ( $R_{GS} = 1\text{M}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	120	150	V
Continuous Drain Current . . . . .	$I_D$	1	1	A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	5	5	A
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 10$	$\pm 10$	V
Maximum Power Dissipation . . . . .	$P_D$	8.33	8.33	W
Above $T_C = 25^\circ\text{C}$ , Derate Linearly . . . . .		0.0667	0.0667	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFL1N12L RFL1N15L	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0$	120	-	-	V
			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ , (Figure 8)	1	-	2	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, T_C = 125^\circ\text{C}$	-	-	25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10\text{V}, V_{DS} = 0$	-	-	$\pm 100$	$\mu\text{A}$
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 1\text{A}, V_{GS} = 5\text{V}$ , (Figures 6, 7)	-	-	1.900	$\Omega$
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 1\text{A}, V_{GS} = 5\text{V}$	-	-	1.9	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx 1\text{A}, V_{DD} = 75\text{V}, R_G = 6.25\Omega,$ $R_L = 75\Omega, V_{GS} = 5\text{V}$ , (Figures 10, 11, 12)	-	10	25	ns
Rise Time	$t_r$		-	10	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	24	45	ns
Fall Time	$t_f$		-	30	50	ns
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ , (Figure 9)	-	-	200	pF
Output Capacitance	$C_{OSS}$		-	-	80	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	-	35	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	15	$^\circ\text{C/W}$

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = 1\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 1\text{A}, dI_{SD}/dt = 50\text{A}/\mu\text{s}$	-	150	-	ns

NOTES:

2. Pulse test: width  $\leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature.

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## Typical Performance Curves Unless Otherwise Specified

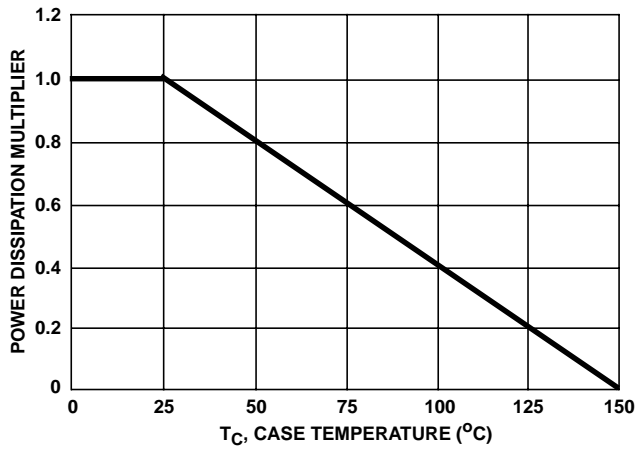


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

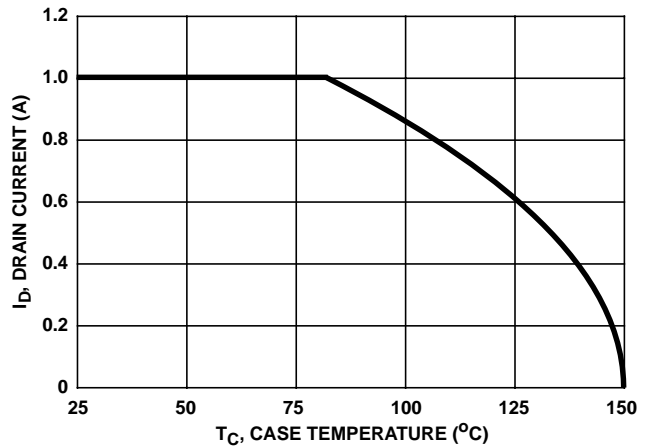


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

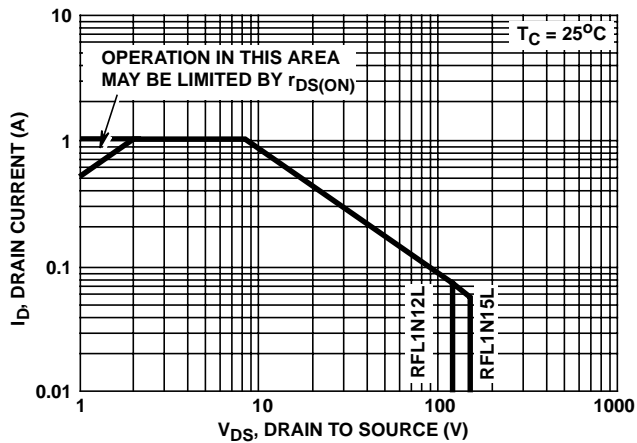


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

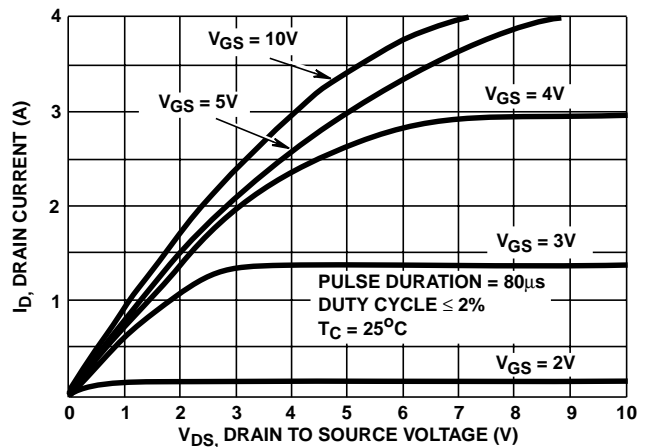


FIGURE 4. SATURATION CHARACTERISTICS

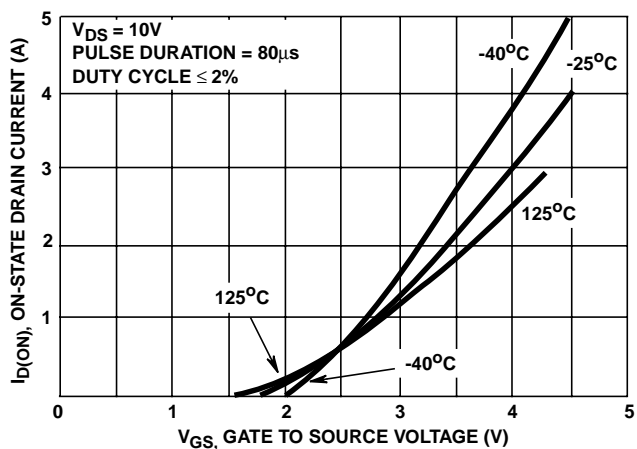


FIGURE 5. TRANSFER CHARACTERISTICS

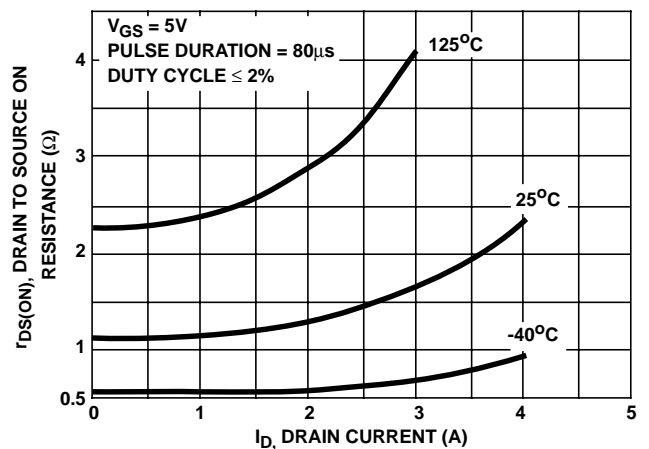


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

**Typical Performance Curves** Unless Otherwise Specified (Continued)

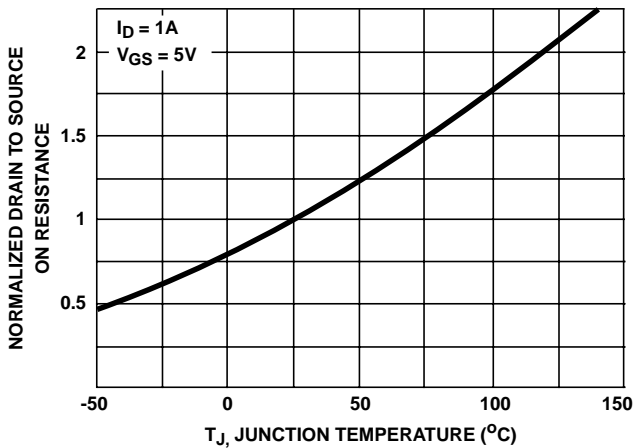


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

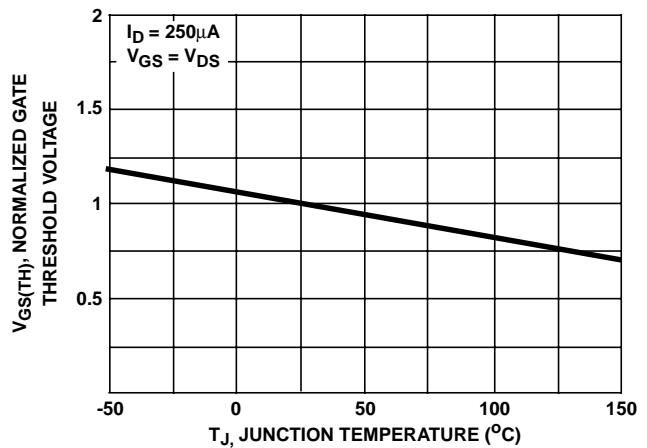


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

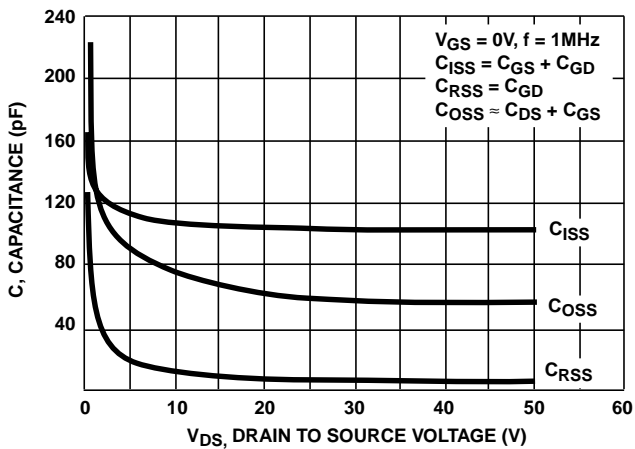
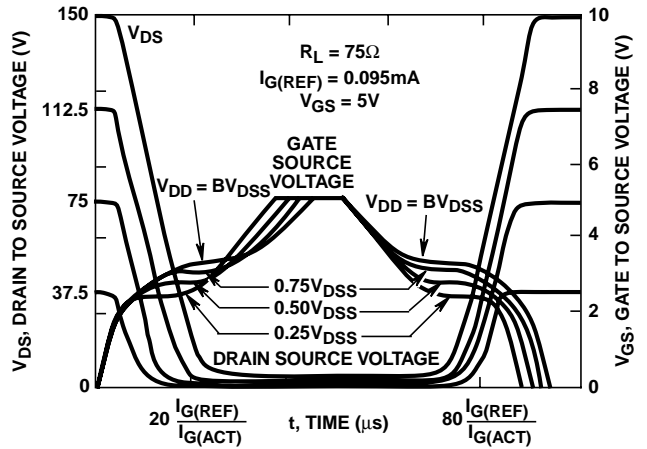


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.  
FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

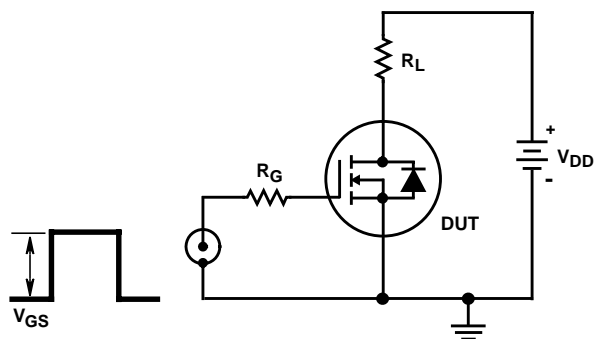


FIGURE 11. SWITCHING TIME TEST CIRCUIT

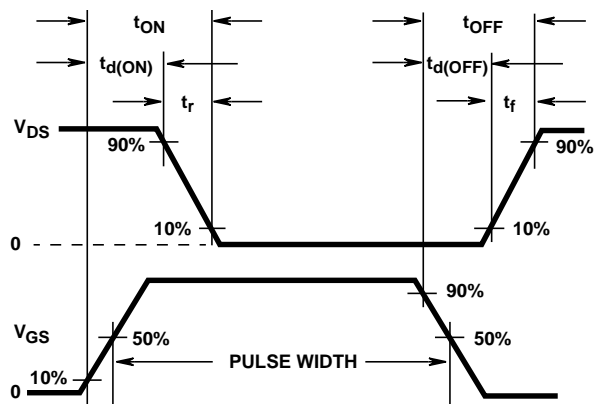


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS