Cellular/GSM 2 Watt Linear GaAs MMIC Power Amplifier

Description

The RMBA09500 is a high power, highly linear Power Amplifier. The two stage circuit uses Raytheon's pHEMT process. It is designed for use as a driver stage for Cellular/GSM base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for CDMA operation. The device is matched for 50 ohms input impedance. The bias currents of the amplifier can be adjusted to obtain optimum power, linearity and efficiency characteristics for GSM, AMPS, NADC and CDMA systems.

Features

- 2 Watt Linear output power at 38 dBc ACPR1 for CDMA operation
- Small Signal Gain of > 30 dB
- Small outline SMD package

Maximum Ratings

Rating	<u>Symbol</u>	<u>Value</u>	<u>Unit</u>
Drain Supply Voltage (Note 1)	V_D	+10	Volts
Gate Supply Voltage	V_{G}	-5	Volts
RF Input Power (from 50Ω source)	P_{RF}	+5	dBm
Operating Case Temperature Range	T_C	-30 to +85	$^{\circ}C$
Storage Temperature Range	T_s	-40 to +100	°C

Electrical Characteristics* (*50 Ohm System, V_D = 7V, T = 25°C)

Storage Temperature Range	•	T _S	-40 to +100	°C
<u>Parameter</u> Frequency Ranges	Min 869 935	<u>Typ</u>	<u>Max</u> 894 960	<u>Unit</u> MHz MHz
Gain (small signal) Over 869-894 MHz Over 935-960 MHz		32 30		dB dB
Gain variation: Over frequency range Over temperature range Noise Figure		+/-1 +/-1.5 6		dB dB dB
Linear output power: for CDMA (Note 2) Saturated output power(Note 3) OIP3(note 4) PAE (CDMA @2W note 2) Input VSWR (50Ω) Drain Voltage (V _D) Gate Voltages	33	38 43 30 2:1 7 (Note 3)		dBm dBm dBm % Volts
Quiescent current $(I_{DQ1,} I_{DQ2})^{(Note 5)}$ Thermal Resistance (Channel to Case) Rjc		150,400 11)	mA °C/W

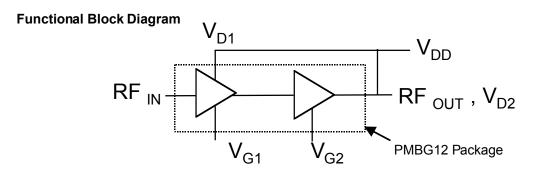
Notes:

- 1. Not with RF power simultaneously applied.
- 2. 9 Channel Forward Link QPSK Source; 1.23 Mbps modulation rate. ACPR1 measured at 885 kHz offset at a value ≥ 38 dBc. CDMA Waveform measured using the ratio of the average power within the 1.23 MHz channel and within a 30 kHz bandwidth at an 885 MHz offset.
- 3. Single tone at Bandcenter.
- 4. Two tones: 1.25 MHz apart at Bandcenter, bias optimized
- 5. Quiescent current can be adjusted to optimize the linearity of the amplifier for differing operation. Default biasing is optimized for CDMA (Ref. Note 2). Gate voltages are to be adjusted to achieve these quiescent currents.

This is advanced information which contains data on products in development. Characteristic performance data and specifications are subject to change without notice.

Advanced Information

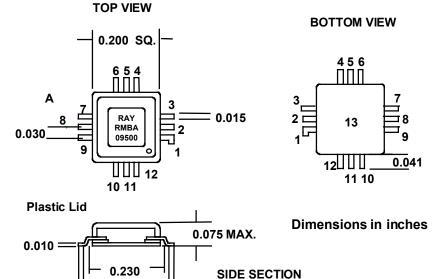
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Typical Performance Data

- 38 dBc ACPR1 at 885 KHz offset for 1.23 Mbps Forward Link at P_{OUT} = 33 dBm; PAE = 29% (9 Channel Forward Pilot, Paging, Traffic and Sync.)
- * Voltage Rail = 7.0 volts

Figure 1: 12 Lead Plastic Air Cavity Package with Integral Heat Sink



Pin#	Description
1 2 3 4 5 6 7 8 9	RF Out & Vd2 RF Out & Vd2 RF Out & Vd2 AC Ground (g2) GND AC Ground (g1) GND RF Input GND Vd1
11 12 13	Vg2 Vg1 GND (METAL BASE)

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following describes a procedure for evaluating the RMBA09500-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for Cellular/GSM base stations, or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. It should be noted that RMBA09500-58 requires external passive components for DC bias and RF output matching circuits. A recommended schematic circuit is shown in Figure 3. The gate biases for the two stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of figure 3. The following designations should be noted:

- (1) Pin designations are as shown in figure 2.
- (2) Vg1 and Vg2 are the Gate Voltages (negative) applied at the pins of the package
- (3) Vgg1 and Vgg2 are the negative supply voltages at the evaluation board terminals
- (4) Vd1 and Vd2 are the Drain Voltages (positive) applied at the pins of the package
- (5) Vdd is the positive supply voltage at the evaluation board terminal.

The base of the package must be soldered on to a heat sink for proper operation.

Test Procedure for the evaluation board (RMBA09500-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA09500.) Note: Vdd1, 2 are tied together.

- Step 1: Turn off RF input power.
- Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Set Vgg1 and Vgg2 to -3V (pinch-off).
- Step 3: Slowly apply drain supply voltages of +7V to the board terminal Vdd ensuring that there is no short
- Step4: Adjust Vgg1 down from -3V until the drain current (with no RF applied) increases to Idq1 as per supplied result sheet. Then adjust Vgg2 until the total drain current becomes equal to the sum of Idq1 and Idq2.
- Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.
- Step 6: Follow turn-off sequence of.
 - (i) Turn off RF Input Power (ii) Turn down and off drain voltage Vdd.
 - (iii) Turn down and off gate voltages Vgg1 and Vgg2.

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Application Information

Figure 2: Functional Block Diagram of Packaged Product

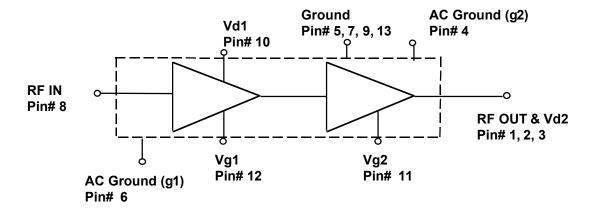
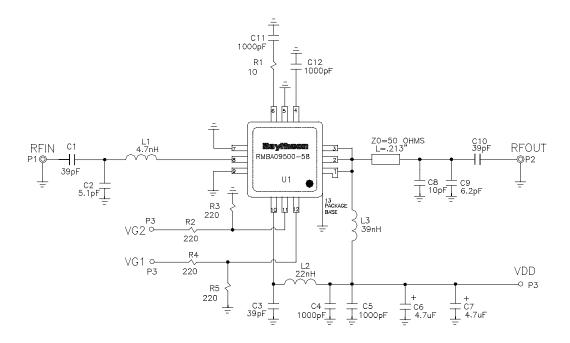


Figure 3: Schematic of Application Circuit showing external components



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Application Information

PARTS LIST for Test Evaluation Board (RMBA09500-58-TB, G654188/G654942)

PART	VALUE	EIA SIZE	Vendor(s)
C1,C3,C10	39 pF	0402	Murata, GRM36COG390J050
C2	5.1 pF	0402	Murata, GRM36COG5R1B050
C8	10 pF	0402	Murata, GRM36COG10RB050
C9	6.2 pF	0402	Murata, GRM36COG6R2B050
C4,C5,C11,C12	2 1000 pF	0402	Murata, GRM36X7R102K050
C6,C7	4.7 uF	3528	TDK, C3216X5R1A475KT
L1	4.7 nH	0603	Toko, LL1608-FH4N7S
L2	22 nH	0603	Toko, LL608-FH22NK
L3	39 nH	1008	Coilcraft, 1008HS-390TKBC
R1	10 Ohm	0402	IMS, RCI-0402-10R0J
W1	26AWG (0.015	" dia) Wire	Alpha, 2853/1
U1	RMBA09500-58		Raytheon, G655978
P3	Right angle Pir	n Header	3M (2340-5211TN)
P1,P2	SMA Connecto	ors	Johnson Components (142-0701-841)
Board	FR4		Raytheon Dwg# G655966, V1
R2, R3,R4,R5	220 ohm	0402	IMS RCI 0402 2200J

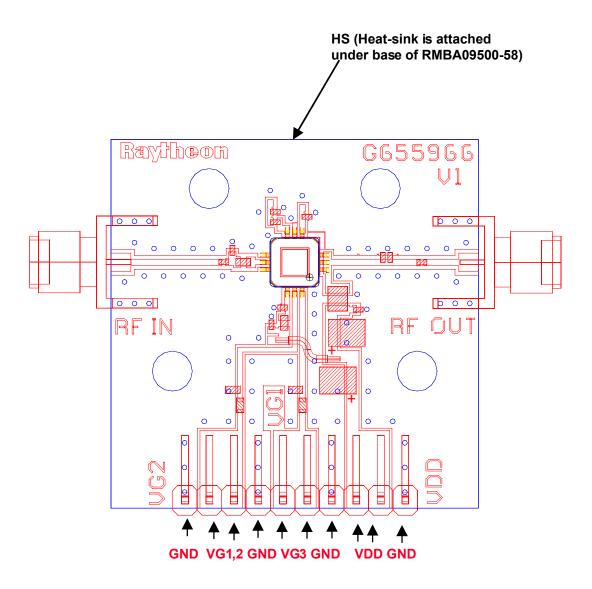
Recommendations for Heat-Sinking the RMBA09500-58

PWB must be prepared with a heat sink, made of a highly conductive (electrical and thermal) material such as copper or aluminum with necessary surface plating, attached to the backside of PWB where the package is to be mounted on the front side. A small pedestal in the heat sink should protrude through a hole in the PWB where the package bottom is directly soldered. Use Sn/Pb (67/37) solder (or Sn/Pn/Ag 62/36/2 solder) at 220°C for 20 seconds or less. The package bottom should be firmly soldered to the pedestal while the pins are soldered to the respective pads on the front side of PWR without causing any stress on the pins. To accomplish stress free mounting, the top surface of the pedestal should be made flush with the top surface of PWB. Remove flux completely if used for soldering.

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Application Information

Figure 4: Layout of Test Evaluation Board (RMBA09500-58-TB)



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