Raytheon

RMBA19500-58

PCS 2 Watt Linear GaAs MMIC Power Amplifier

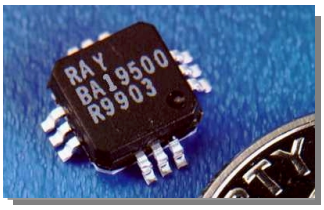
ADVANCED INFORMATION

Description

The RMBA19500 is a high power, highly linear Power Amplifier. The circuit uses Raytheon's pHEMT process. It has been designed for use as a driver stage for PCS base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for CDMA operation. The device is matched for 50 ohms input impedance.

Features

- 2 Watt Linear output power at 38 dBc ACPR1 for CDMA operation
- Small Signal Gain of 30 dB
- Small outline SMD package



Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Drain Supply Voltage [1]	V_D	+10	Volts
Gate Supply Voltage	V_G	-5	Volts
RF Input Power (from 50 Ω source)	P_{RF}	+5	dBm
Operating Case Temperature Range	T_C	-30 to +85	°C
Storage Temperature Range	T_S	-40 to +100	°C

Electrical Characteristics

(50 Ohm System, VD = 7V, T = 25°C)

Parameter	Min	Typ	Max	Unit
Frequency Range	1930		1990	MHz
Gain (small signal)				
Over 1930-1990 MHz		30		dB
Gain variation:				
Over frequency range		+/-1		dB
Over temperature range		+/- 1.5		dB
Noise Figure		6		dB
Linear output power:				
for CDMA [2]	33			dBm
Saturated output power [3]		38		dBm

Parameter	Min	Typ	Max	Unit
OIP3 [4]		40.5		dBm
PAE (CDMA modulation				
@2W) [2]		20		%
Input VSWR (50 Ω)		2:1		
Drain Voltage (VD)		7		Volts
Gate Voltages		-3		Volts
Quiescent current				
(I_{DQ1},2, I_{DQ3}) [5]		180, 445		mA
Thermal Resistance				
(Channel to Case) Rjc		11		°C/W

Typical Performance Data

- 38 dBc ACPR1 at 885 KHz offset for 1.23 Mbps Forward Link at POUT = 33 dBm; PAE = 20% (9 Channel Forward - Pilot, Paging, Traffic and Sync.)
- > 30 dBc ACPR1 and > 48 dBc ACPR2 at 30 KHz and 60 KHz offsets for 48.6 Kbps NADC TDMA at POUT = 34 dBm; PAE = 27%
- > 30 dBc and > 60 dBc emissions at 200 KHz and 400 KHz offsets for 270 Kbps GSM at POUT = 34 dBm; PAE = 27%

For above conditions refer to Note 3.

* Voltage Rail = 7 volts

Notes:

1. Only under quiescent conditions - no RF applied.
2. 9 Channel Forward Link QPSK Source; 1.23 Mbps modulation rate. ACPR1 measured at 885 KHz offset at a value ≥ 38 dBc. CDMA Waveform measured using the ratio of the average power within the 1.23 MHz channel and within a 30 kHz bandwidth at an 885 MHz offset.
3. Single tone at Band center.
4. Two tones: 1.25 MHz apart at Bandcenter: bias optimized.
5. Quiescent currents can be adjusted to optimize the linearity of the amplifier for differing operation. Default biasing is optimized for CDMA (Ref Note 2). Gate voltages are to be adjusted to achieve these quiescent currents.

Characteristic performance data and specifications are subject to change without notice.

Raytheon RF Components
362 Lowell Street
Andover, MA 01810

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

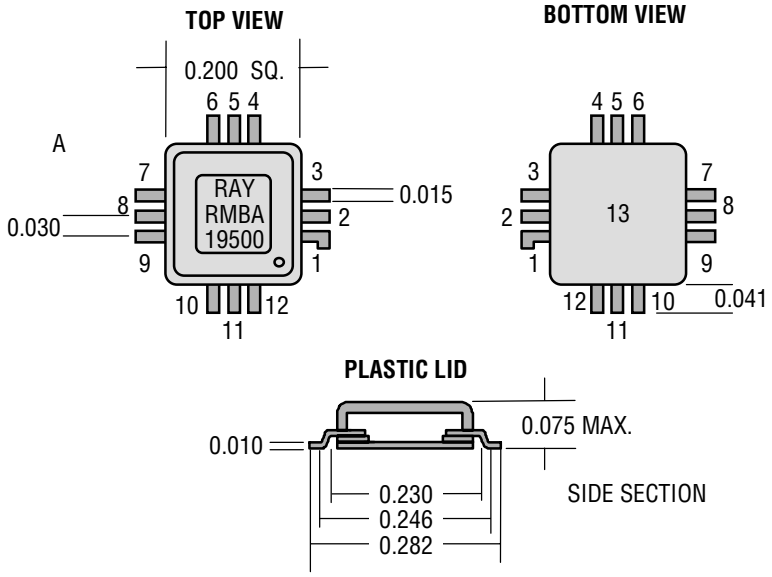
The following describes a procedure for evaluating the RMBA19500-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for PCS Base station or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. It should be noted that RMBA19500-58 requires external passive components for DC bias and RF output matching circuits. A recommended schematic circuit is shown in Figure 3. The gate biases for the three stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of figure 3. The following designations should be noted:

(1) Pin designations are as shown in figure 2.
(2) Vg1, Vg2 and Vg3 are the Gate Voltages (negative) applied at the pins of the package
(3) Vgg1, Vgg2 and Vgg3 are the negative supply voltages at the evaluation board terminals (Vg1and Vg2 are tied together)
(4) Vd1, Vd2 and Vd3 are the Drain Voltages (positive) applied at the pins of the package
(5) Vdd is the positive supply voltage at the evaluation board terminal (Vd1, Vd2 and Vd3 are tied together)

Note: The base of the package must be soldered on to a heat sink for proper operation.

Figure 1
12 Lead Plastic Air Cavity Package with Integral Heat Sink

Dimensions in inches



Pin #	Description
1	RF Out & Vd3
2	RF Out & Vd3
3	RF Out & Vd3
4	VD1
5	GND
6	VG1
7	RF In
8	GND
9	VG2
10	VD2
11	GND
12	VG3
13	GND

Figure 2
Functional Block Diagram of Packaged Product

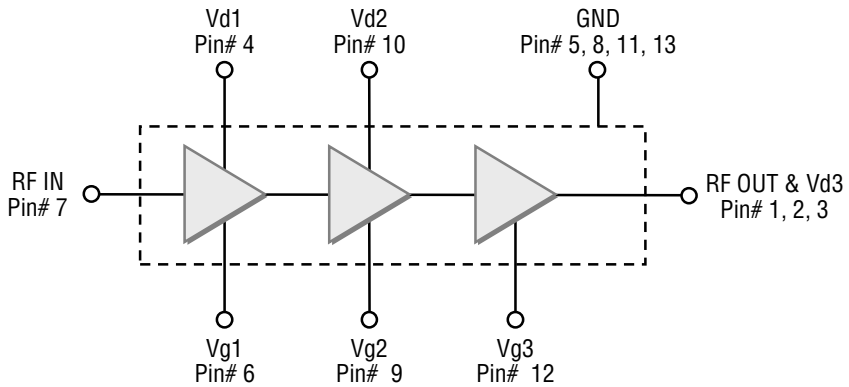


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Figure 3
Schematic of Application Circuit showing external components

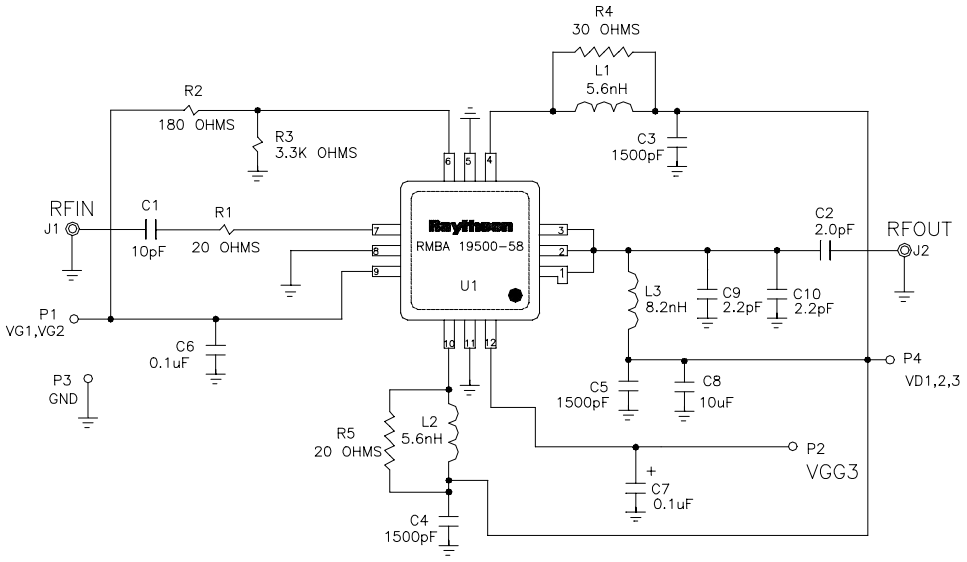
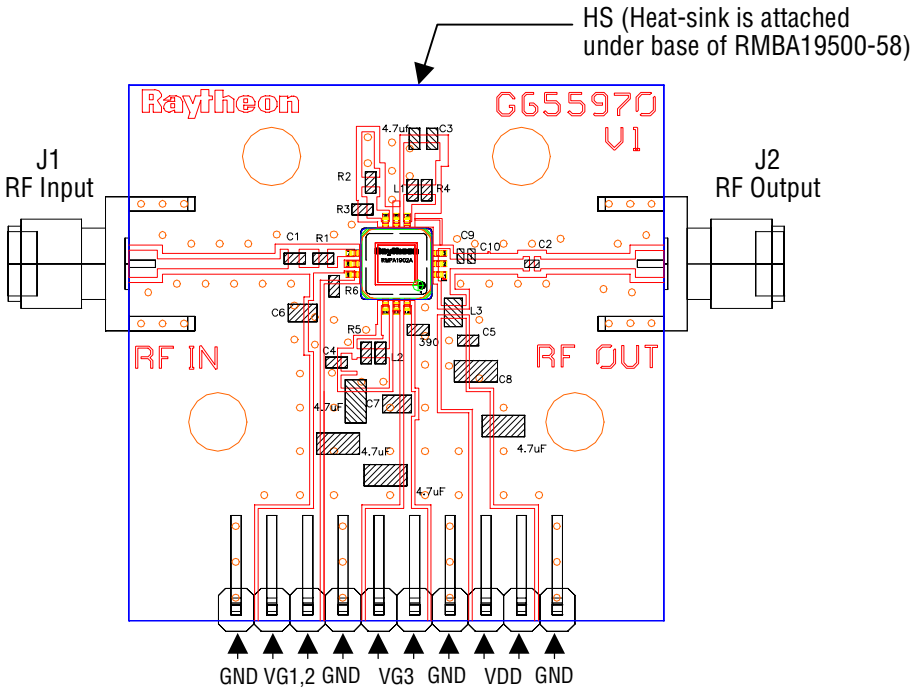


Figure 4
Layout of Test Evaluation Board (RMBA19500-58-TB)



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Test Procedure
for the evaluation board (RMBA19500-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2, VG3) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA19500.)

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Set Vgg1, Vgg2 and Vgg3 to -3V (pinch-off).

Step 3: Slowly apply drain supply voltages of +7 V to the board terminal Vdd ensuring that there is no short.

Step 4: Adjust Vgg12 down from -3V until the drain current (with no RF applied) increases to Idq12 as per supplied result sheet. Then adjust Vgg3 until the total drain current becomes equal to the sum of Idq12 and Idq3.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

Step 6: Follow turn-off sequence of:

(i) Turn off RF Input Power

(ii) Turn down and off drain voltage Vdd.

(iii) Turn down and off gate voltages Vgg1, Vgg2 and Vgg3.

Parts List
for Test Evaluation Board (RMBA19500-58-TB, G654188/G654942)

Part	Value	Size (EIA)	Vendor(s)
L1, L2	5.6 nH	.06" x .03"	Toko (LL1608-F5N6)
L3	8.2 nH	.08" x .05"	Coilcraft (0805HT-8N2TKBC)
C1	10 pF	.06" x .03"	Murata (GRM39COG100J050AD)
C2	2.2 pF	.06" x .03"	Murata (GRM39COG2R2J050BD)
C3, C4, C5	1500 pF	.06" x .03"	Murata (GRM39Y5V152Z50V)
C10, C9	2.2 pF	.06" x .03"	Murata (GRM39COG2R2J050BD)
C8	10.0 uF	.12"x.06"	TDK (CC1206JX5R106M)
C6,C7	0.1uF		Murata (GRM39Y5V104Z)
R1-R5	20 Ohms	.06"x .03"	IMS (RCI-0603-20R0J)
R2	180 Ohms	.06"x .03"	IMS (RCI-0603-1800J)
R3	3.3K Ohms	.06"x .03"	IMS (RCI-0603-3301J)
R4	30 Ohms	.06"x .03"	IMS (RCI-0603-30R0J)
U1	RMBA19500-58	.31" x .41	Raytheon, G654466/G653367
HS	Heatsink		Raytheon, G655548
P1-P5	Terminals		Samtec (TSW-102-09-T-S-RE)
J1, J2	SMA Connectors		E.F. Johnson (142-0701-841)
Board	FR4		Raytheon Dwg# G654187/G654941

Recommendations
for Heat-Sinking the RMBA19500-58

PWB must be prepared with a heat sink, made of a highly conductive (electrical and thermal) material such as copper or aluminum with necessary surface plating, attached to the backside of PWB where the package is to be mounted on the front side. A small pedestal in the heat sink should protrude through a hole in the PWB where the package bottom is directly soldered. Use Sn/Pb (67/37) solder (or Sn/Pn/Ag 62/36/2 solder) at 220°C for 20 seconds or less. The package bottom should be firmly soldered to the pedestal while the pins are soldered to the respective pads on the front side of PWR without causing any stress on the pins. To accomplish stress free mounting, the top surface of the pedestal should be made flush with the top surface of PWB. Remove flux completely if used for soldering.

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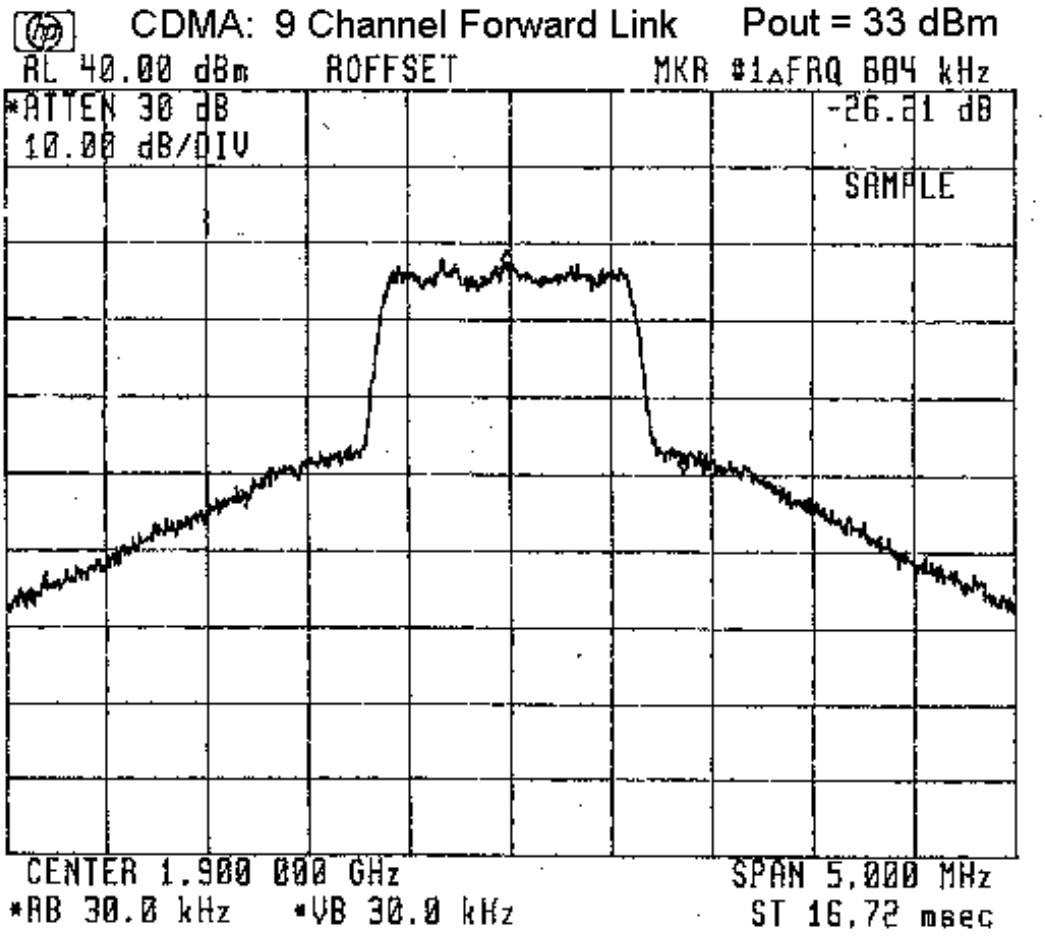
Performance Data



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