

RMBA19500A-58 PCS1900 2 Watt GaAs MMIC Power Amplifier

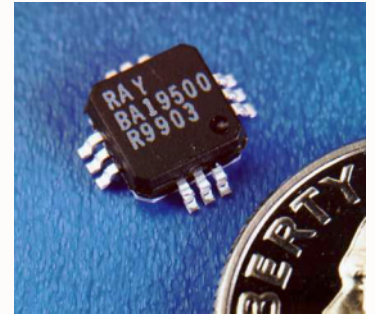
PRODUCT INFORMATION

Description

The RMBA19500A-58 is a highly linear Power Amplifier. The two stage circuit uses Raytheon RF Components' pHEMT process. It has been designed for use as a driver stage for PCS1900 base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for PCS operation.

Features

- ◆ 2 Watt linear output power at 36 dBc ACPR1 for CDMA operation
- ◆ OIP3 ≥43 dBm at 27 and 30 dBm output
- ◆ Small Signal Gain of >30 dB
- ◆ Small outline SMD package



Electrical Characteristics²

Parameter	Min	Typ	Max	Unit
Frequency Range	1930		1990	MHz
Gain (small signal) Over 1930-1990 MHz	30			dB
Gain variation:				
Over frequency range		+/- 1.0		dB
Over temperature range		+/- 1.5		dB
Noise Figure		6		dB
P1dB Output		30		dBm
Output Power @ CDMA ³	33			dBm

Parameter	Min	Typ	Max	Unit
PAE@33 dBm Pout		24		%
OIP3 ⁴	43	45		dBm
Drain Voltage (Vdd)		7.0		Volts
Gate Voltage (VG1,2 and VG3) ⁵	-2		-0.25	Volts
Quiescent currents (Idq1,2 and Idq3) ⁵		180, 445		mA
Thermal Resistance (Channel to Case)	Rjc	11		°C/W

Absolute Ratings

Parameter	Symbol	Value	Unit
Drain Supply Voltage ¹	Vd	+10	Volts
Gate Supply Voltage (max absolute value)	Vg	-5	Volts
RF Input Power (from 50Ω source)	Pin	+5	dBm
Operating Case Temperature Range	Tc	-30 to +85	°C
Storage Temperature Range	Tstg	-40 to +100	°C

Notes:

1. Only under quiescent conditions – no RF applied.
2. V_{DD} = 7.0V, T_c = 25°C. Part mounted on evaluation board with input and output matching to 50 Ohms.
3. 9 Channel Forward Link QPSK Source; 1.23 Mbps modulation rate. CDMA ACPR1 is measured using the ratio of the average power within the 1.23 MHz channel at band center to the average power within a 30 KHz bandwidth at an 885 KHz offset. Minimum CDMA output power is met with ACPR1 > 36 dBc.
4. OIP3 specifications are achieved for power output levels of 27 and 30 dBm per tone with tone spacing of 1.25 MHz at band-center with adjusted supply and bias conditions of V_{dd}=6.5V and Id_{qTotal}=625mA (see Note 5).
5. VG1,2 and VG3 must be individually adjusted to achieve IDQ1,2 and IDQ3. A single VGG bias supply adjusted to achieve IDQ_{TOTAL}=625mA can be used with nearly equivalent performance. Values for IDQ1,2 and IDQ3 shown have been optimized for CDMA operation. IDQ1,2 and IDQ3 (or IDQ_{TOTAL}) can be adjusted to optimize the linearity of the amplifier for other modulation systems.

The device requires external input and output matching to 50 Ohms as shown in Figure 3 and the Parts List.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

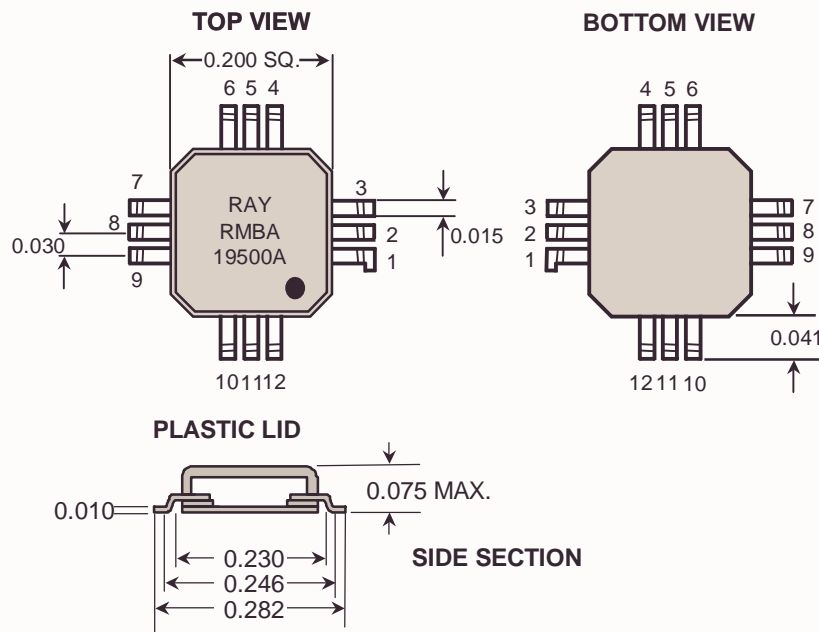
The following describes a procedure for evaluating the RMBA19500A-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for PCS1900 Base station or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. The RMBA19500A-58 requires external passive components for DC bias and RF input and output matching circuits as shown in Figure 3 and the Parts List. A recommended schematic circuit is shown in Figure 3. The gate biases for the three stages of the amplifier may be be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of figure 3. The following designations should be noted:

- (1) Pin designations are as shown in figure 2.
- (2) Vg1, Vg2, and Vg3 are the Gate Voltages (negative) applied at the pins of the package.
- (3) Vgg1, 2, and Vgg3 are the negative supply voltages at the evaluation board terminals (Vg1 and Vg2 are tied together).
- (4) Vd1, Vd2, and Vd3 are the Drain Voltages (positive) applied at the pins of the package.
- (5) Vdd is the positive supply voltage at the evaluation board terminal (Vd1, Vd2, and Vd3 are tied together).

Note: The base of the package must be soldered on to a heat sink for proper operation.

Figure 1
Package Outline
and Pin
Designations

Dimensions in inches



Pin#	Description
1	RF Out & Vd3
2	RF Out & Vd3
3	RF Out & Vd3
4	Vd1
5	GND
6	Vg1
7	RF In
8	GND
9	Vg2
10	Vd2
11	GND
12	Vg3
13	GND

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Figure 2
Functional Block Diagram

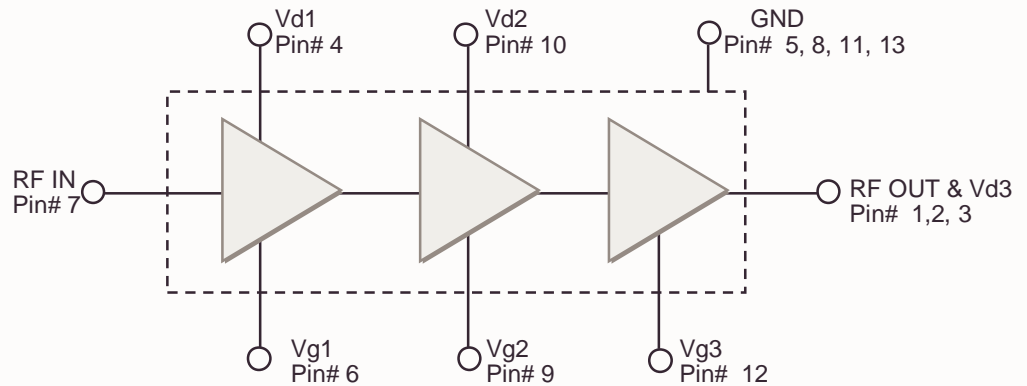
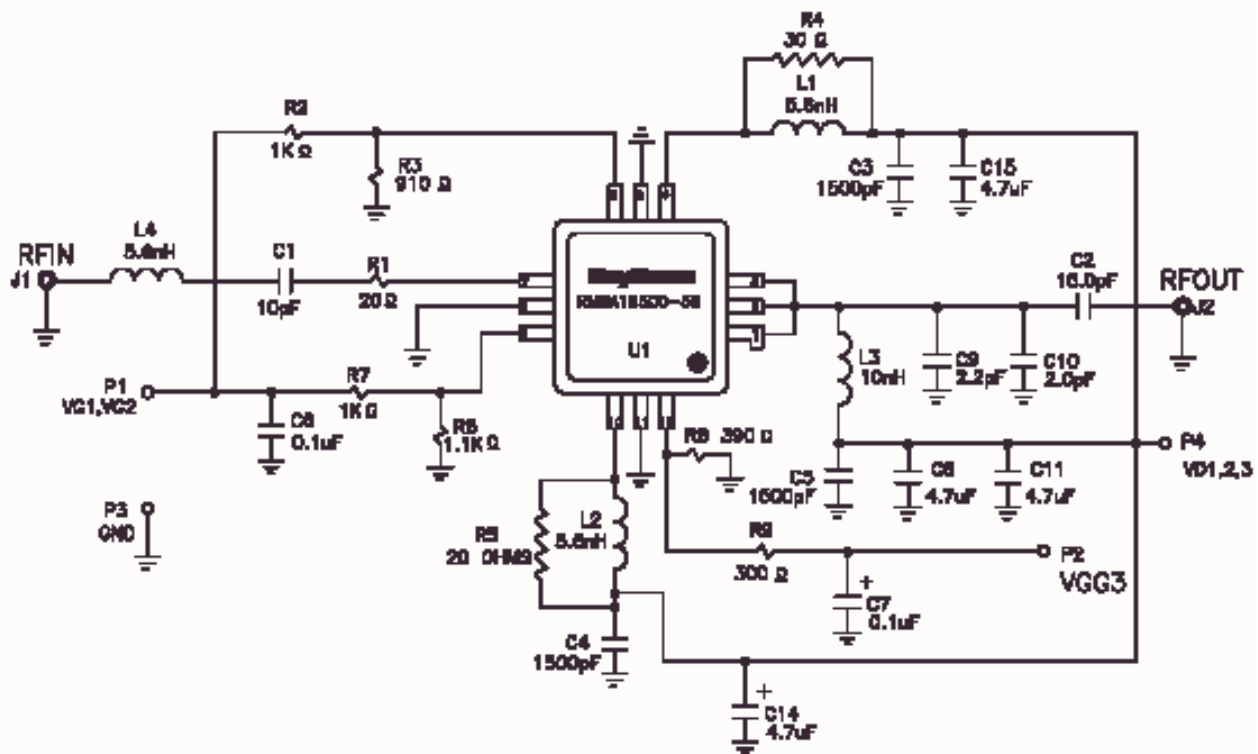


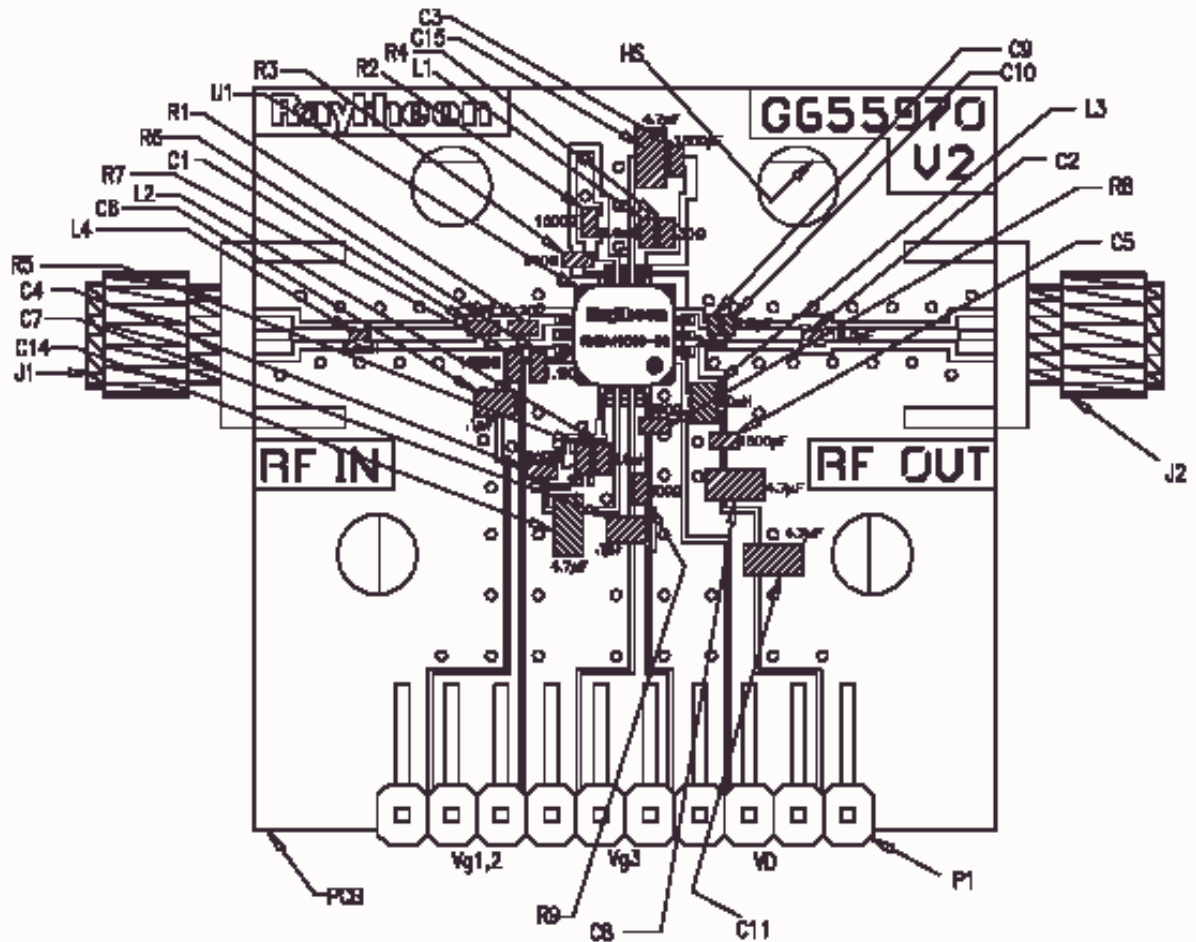
Figure 3
Schematic of Application Circuit showing external components



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Figure 4
Layout of Test
Evaluation Board
(RMBA19500A-58-TB,
G655971)



Test Procedure

for the evaluation board (RMBA19500A-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (Vg1, Vg2, Vg3) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA19500A.)

- Step 1:** Turn off RF input power.
- Step 2:** Use GND terminal of the evaluation board for the ground of the DC supplies. Set Vgg1, 2 and Vgg3 to -4V (pinch-off).
- Step 3:** Slowly apply drain supply voltages of +5 V to the board terminal Vdd ensuring that there is no short.
- Step 4:** Adjust Vgg3 up from -3V until the drain current (with no RF applied) increases to Idq3 as per supplied result sheet. Then adjust Vgg1, 2 until the total drain current becomes equal to the sum of Idq1, 2 and Idq3.
- Step 5:** After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.
- Step 6:** Follow turn-off sequence of:
 - (i) Turn off RF Input Power
 - (ii) Turn down and off drain voltage Vdd.
 - (iii) Turn down and off gate voltages Vgg1, 2 and Vgg3.

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PCS1900 2 Watt GaAs MMIC Power Amplifier

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Parts List
for Test Evaluation
Board (RMBA19500A-
58-TB,
G654188/G654942)

Part	Value	EIA Size	Vendor(s)
L1, L2,L4	5.6 nH	.06" x .03"	Toko (LL1608-F5N6)
L3	10 nH	.085" x .060"	Coilcraft (0805HT-10NTKBC)
C1	10 pF	.067" x .036"	Murata(GRM39COG100J050AD)
C9	2.2 pF	.042" x .022"	Murata(GRM36COG2R2J050BD)
C3, C4, C5	1500 pF	.067" x .036"	Murata (GRM39Y5V152Z50V)
C10	2.0 pF		Murata(GRM36COG2R20J050BD)
C2	15.0 pF	.042" x .022"	Murata(GRM36COG150J050)
C8,C11,C14,C15	4.7 uF	.134" x .071"	TDK (C3216XR1A475KT)
C6,C7	0.1uF	.183" x .054"	Murata (GRM39Y5V104Z50)
R1,R5	20 Ohms	.069" x .037"	IMS (RCI-0603-20R0J)
R2,R7	1000 Ohms	.069" x .037"	IMS (RCI-0603-1001J)
R3	910 Ohms	.069" x .037"	IMS (RCI-0603-9100J)
R4	30 Ohms	.069" x .037"	IMS (RCI-0603-30R0J)
R6	1.1K Ohms	.069" x .037"	IMS (RCI-0603-1101J)
R8	390 Ohms		IMS (RCI-0603-3900J)
R9	300 Ohms		IMS (RCI-0603-3000J)
U1	RMBA19500-58	.31" x .41"	Raytheon
HS	Heatsink		Raytheon, G655548
P1	Terminals		3M (2340-5211TN)
J1, J2	SMA Connectors		E.F. Johnson (142-0701-841)
Board	FR4		Raytheon Dwg# G654187/G654941

Thermal Considerations
for Heat Sinking the
RMBA19500A-58

The PWB must be prepared with either an embedded copper slug in the board where the package is to be mounted or a heat sink should be attached to the backside of the PWB where the package is to be mounted on the front side. The slug or the heat sink should be made of a highly electrically and thermally conductive material such as copper or aluminum. The slug should be at least the same thickness as the PWB. In the case of the heat sink, a small pedestal should protrude through a hole in the PWB where the package bottom is directly soldered. In either configuration, the top surface of the slug or the pedestal should be made coplanar with the package lead mounting plane i.e., the top surface of the PWB. Use Sn96 solder (96.5% Sn and 3.5% Ag) at 220°C for 20 seconds or less to attach the heat sink to the backside of the PWB. Then, using Sn63, the package bottom should be firmly soldered to the slug or the pedestal while the pins are soldered to the respective pads on the front side of the PWB without causing any stress on the pins. Remove flux completely if used for soldering.

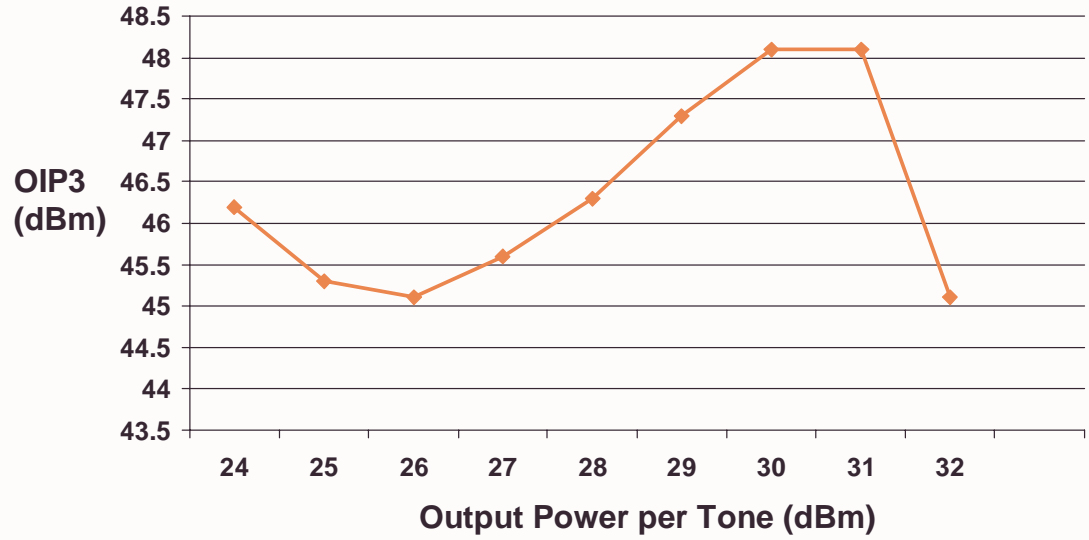
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Performance Data

RMBA19500A OIP3 vs Power Output per Tone
1.960 Ghz, 25°C, Vd=7.0V



Gain vs Power Output per Tone

1.960 Ghz, 25°C, Vd=7.0V

