Raytheon

# RMDA20420

## 20-42 GHz General Purpose MMIC Amplifier

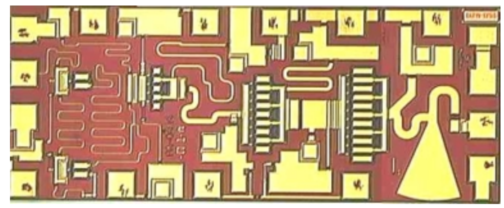
ADVANCED INFORMATION

### Description

The Raytheon RMDA20420 is a broadband general purpose driver amplifier designed for use in point to point radio, point to multi-point communications, LMDS, SatCom and other millimeter wave applications. The RMDA20420 is a fully matched GaAs MMIC utilizing Raytheon's advanced 0.15µm gate length PHEMT process.

### Features

- Wideband 20 - 42 GHz operation
- 22 dB small signal gain (typ.)
- 23 dBm saturated power output (typ.)
- Matched to 50 Ohms
- Optional bonding configuration for multiplier applications
- Chip Size 1.720 mm x 0.760 mm



### Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Positive DC Voltage (+3.5 V Typical) | Vd | + 5 | Volts |
| Negative DC Voltage | Vg | - 2 | Volts |
| Simultaneous (Vd - Vg) | Vdg | + 7 | Volts |
| Positive DC Current | Id | 600 | mA |
| RF Input Power (from 50 Ω source) | Pin | 15 | dBm |
| Operating Base Plate Temperature | Tc | -30 to +70 | °C |
| Storage Temperature Range | Tstg | -55 to +125 | °C |
| Thermal Resistance (Channel to Backside) | Rjc | 57 | °C/W |

### Electrical Characteristics[1]

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency Range | 20 | | 42 | GHz |
| Drain Supply Voltage (Vd) | 2 | 3.5 | 5 | V |
| Gate Supply Voltage (Vg)[2] | -2 | -0.2 | 0.5 | V |
| Gain Small Signal Gain | 20 | 22 | | dB |
| Gain Variation vs. Frequency | | +/-2.5 | | dB |
| Power Output at 1 dB Compression | | 21 | | dBm |

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Power Output Saturated | 22 | 23 | | dBm |
| Drain Current at P1 dB Compression | | 355 | | mA |
| Drain Current at Psat | | 362 | | mA |
| Input Return Loss (Pin=-20 dBm) | | 12 | | dB |
| Output Return Loss (Pin=-20 dBm) | | 10 | | dB |

**Notes:**
1. Operated at 25 °C, 50 Ohm system, Vd=+3.5 V, quiescent current (Idq)=350 mA.
2. Typical range of the negative gate voltage is -0.5 to 0.0V to set typical Idq of 350 mA.

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### Application Information

**CAUTION: THIS IS AN ESD SENSITIVE DEVICE**

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.

**Figure 1**
Functional Block Diagram

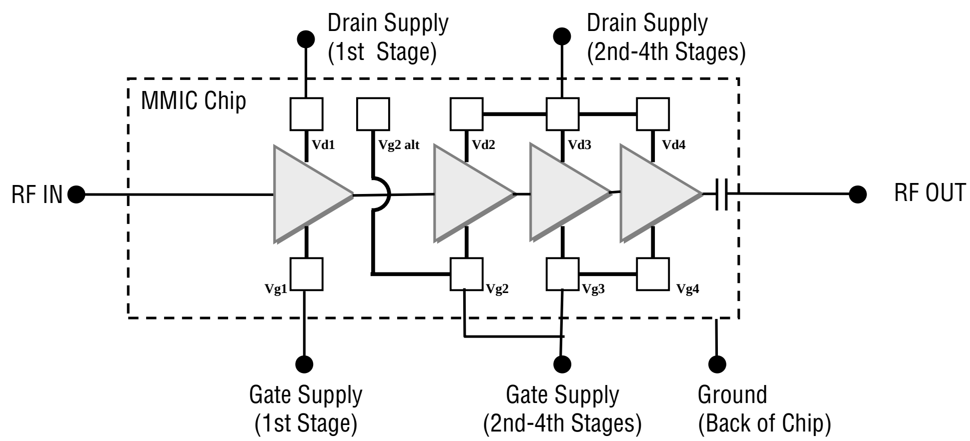
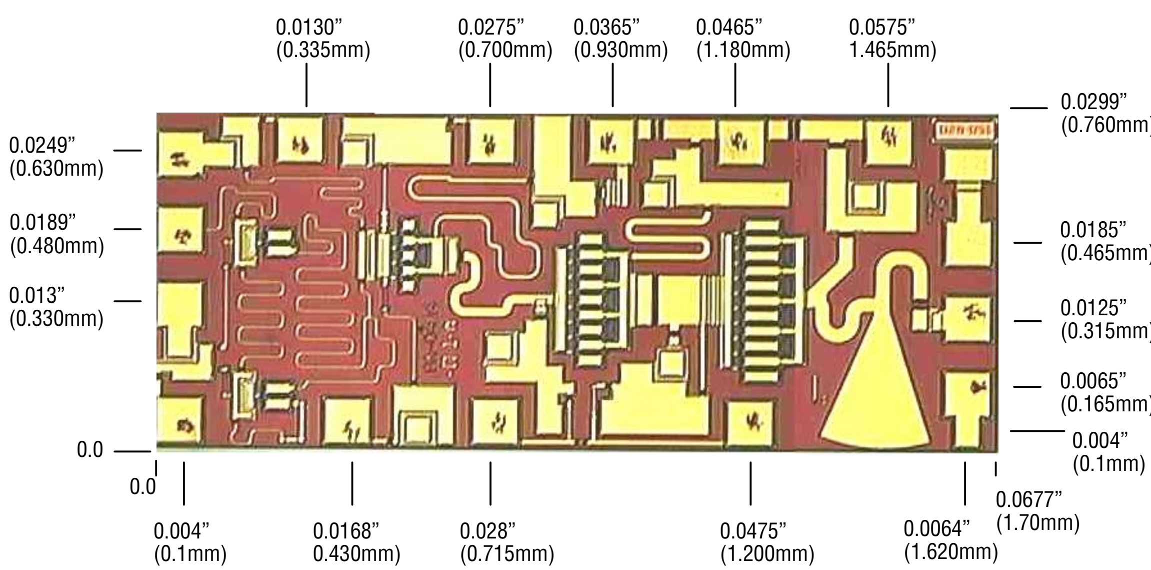



**Figure 2**
Chip Layout and Bond Pad Locations

Chip Size=0.0677" x 0.30" x 0.002" (1720 µm x 760 µm x 50 µm)




**Back of Chip is RF and DC Ground**

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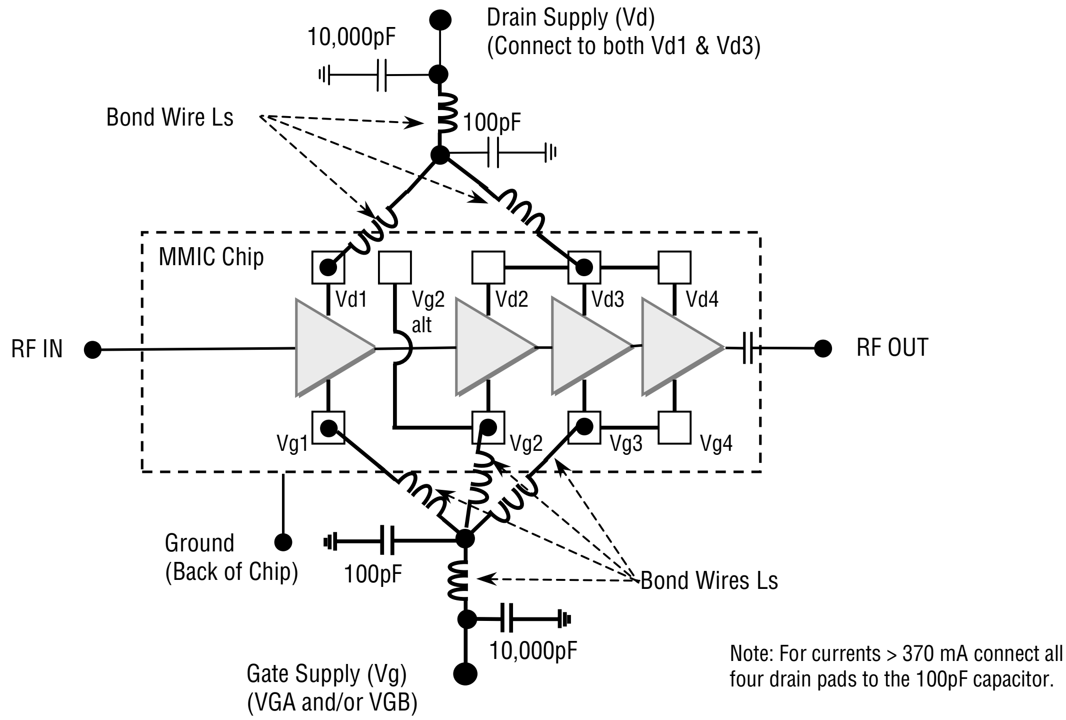


**Figure 3**
Schematic of Application Circuit

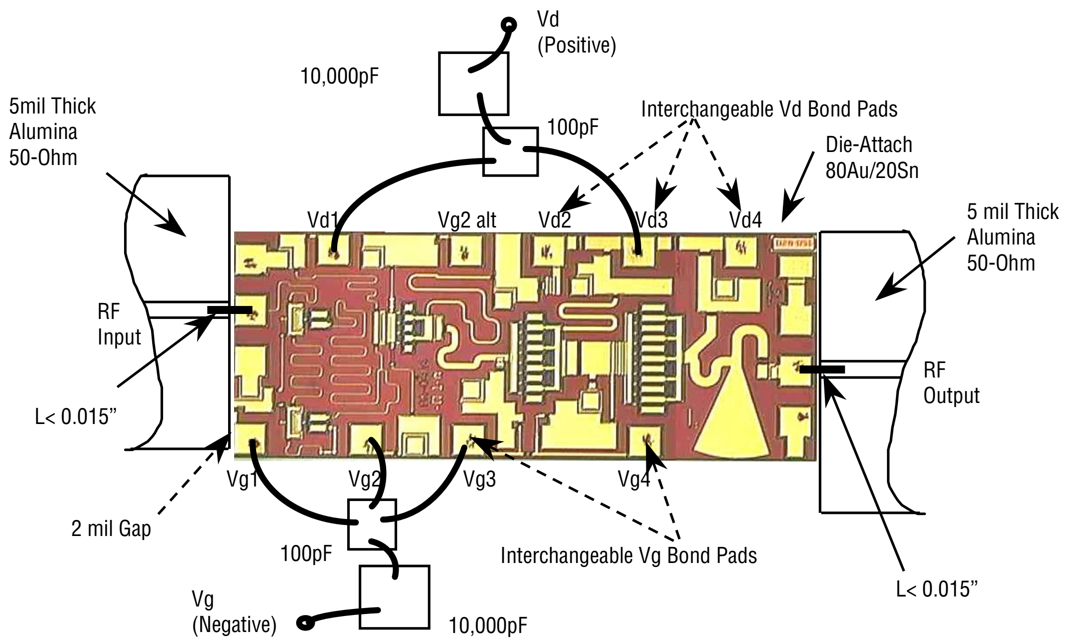


**Figure 4**
Recommended Assembly and Bonding Diagram

**Notes:**
1. Die-attach with 80Au/20Sn
2. Use 0.003" x 0.0005" gold ribbon for bonding.
3. RF input and output bonds should be less than 0.015" long with stress relief.
4. For currents > 370 mA connect all drain pads (Vd1, Vd2, Vd3, & Vd4) to the 100 pF capacitor.
5. Back of chip is DC and RF ground

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### Recommended Procedure
(for biasing and operation)

**CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT CAN DAMAGE THE AMPLIFIER.**

The following sequence must be followed to properly test the amplifier:

**Step 1:** Turn off RF input power.

**Step 2:** Connect the DC supply grounds to the ground of the chip carrier.
Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

**Step 3:** Slowly apply positive drain bias supply voltage of +3.5 V to Vd.

**Step 4:** Adjust gate bias voltage to set the quiescent current of Idq=350 mA.

**Step 5:** After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

**Step 6:** Follow turn-off sequence of:

(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

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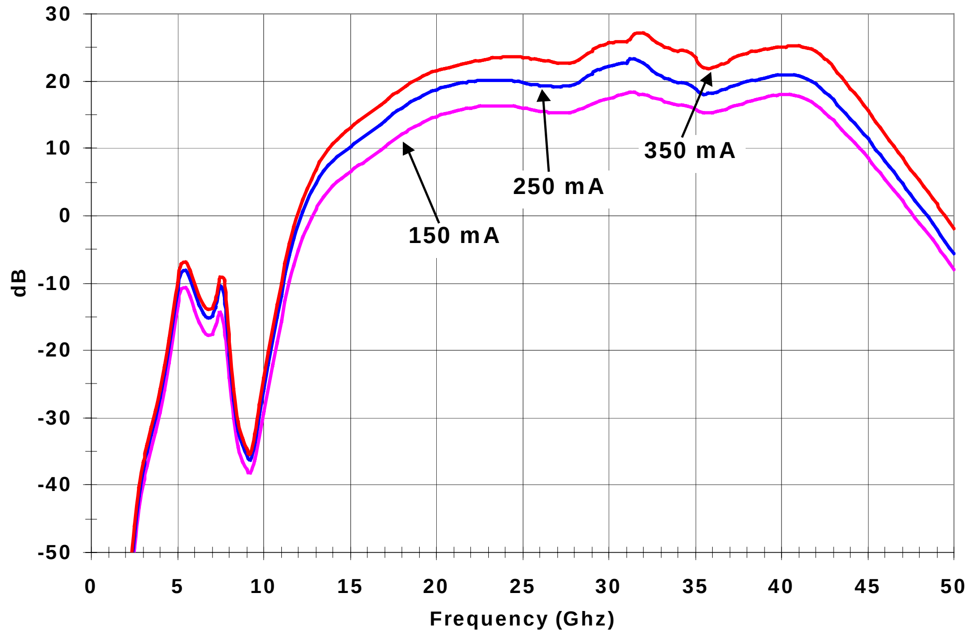
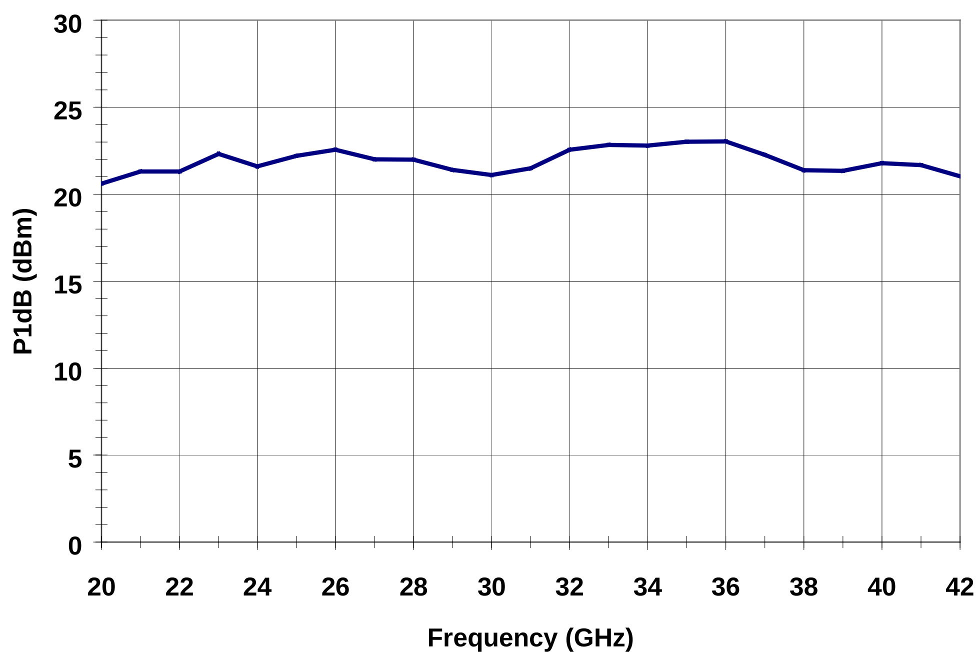
### Performance Data

**Typical SS Gain vs Frequency vs Supply Current**
**Bias Vd=3.5**




**Typical Output Power @ 1dB Compression**
**Bias Vd=3.5 V, Id=350 mA**

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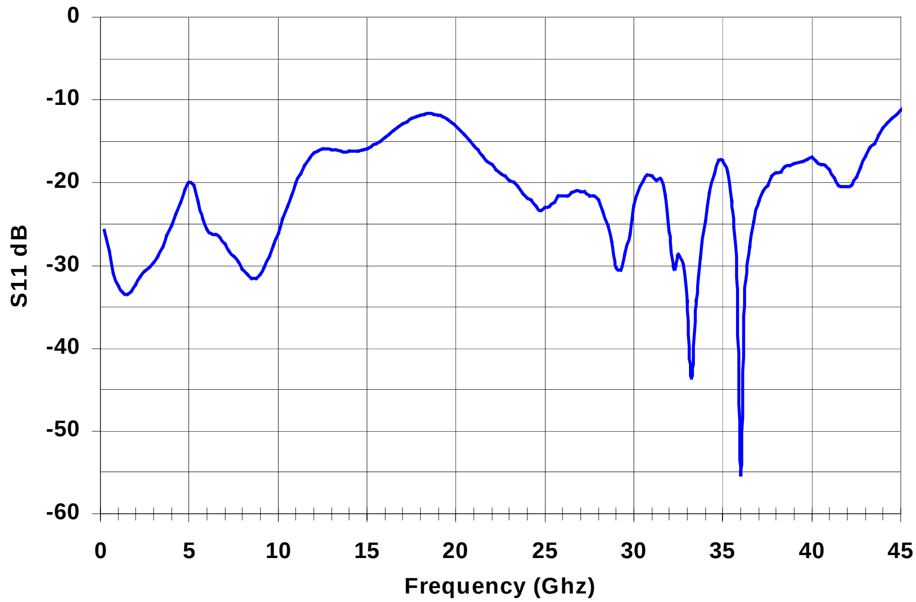
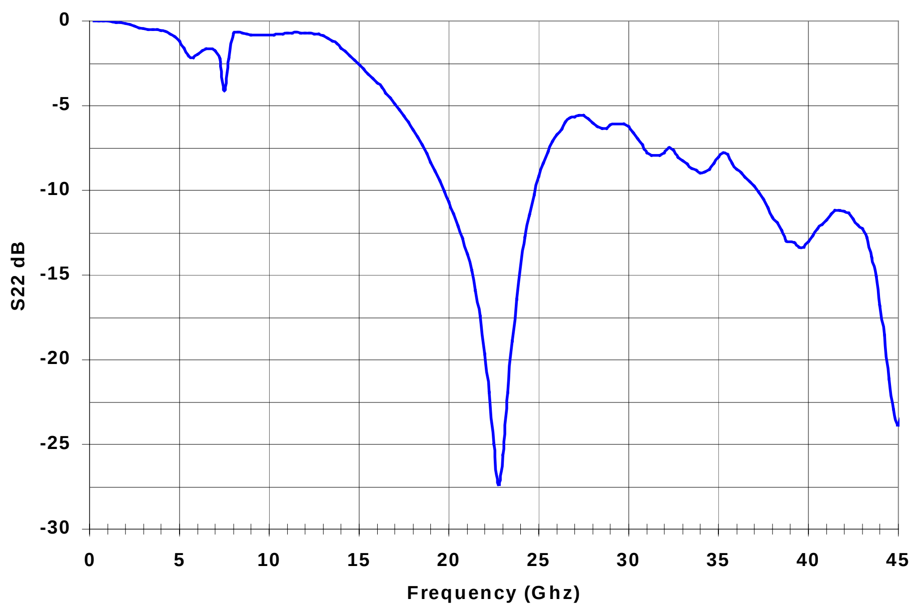
### Performance Data

**Typical Input Return Loss vs Frequency**
**Bias Vd=3.5 V, Id=350 mA**




**Typical Output Return Loss vs Frequency**
**Bias Vd=3.5 V, Id=350 mA**

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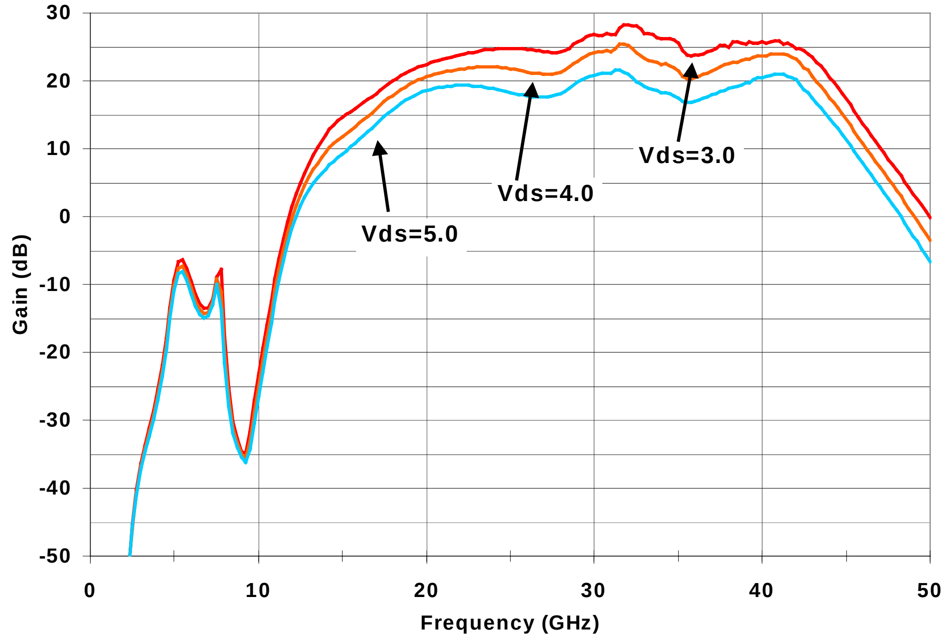
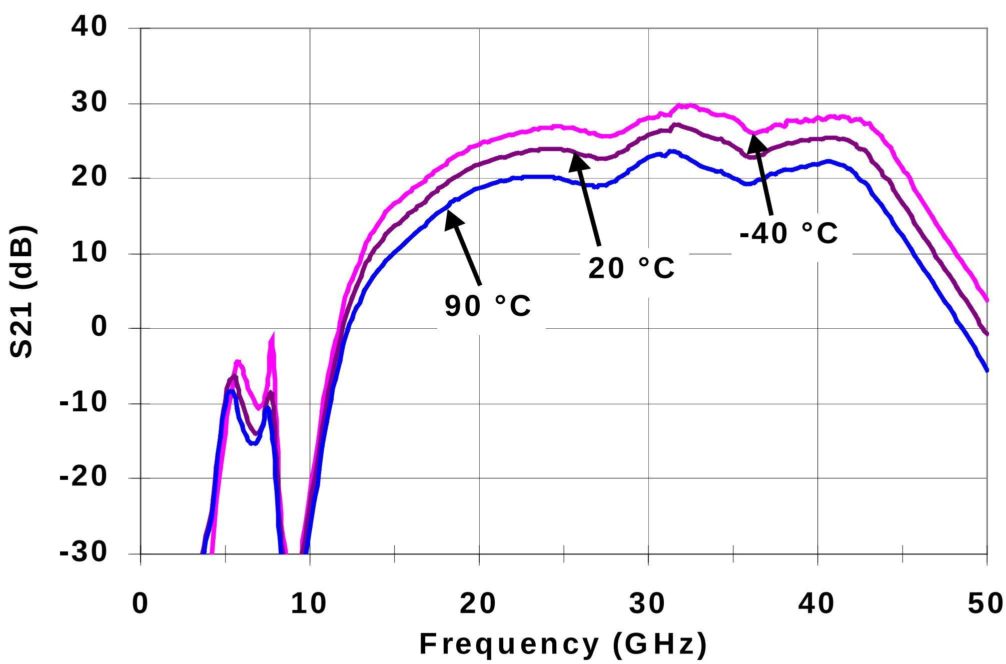
### Performance Data

**Typical SS Gain vs Frequency vs Supply Voltage**
**Supply Current=350 mA**




**Typical SS Gain vs Frequency vs Base Plate Temperature**
**Bias Vd=3.5 V, Id=350 mA**

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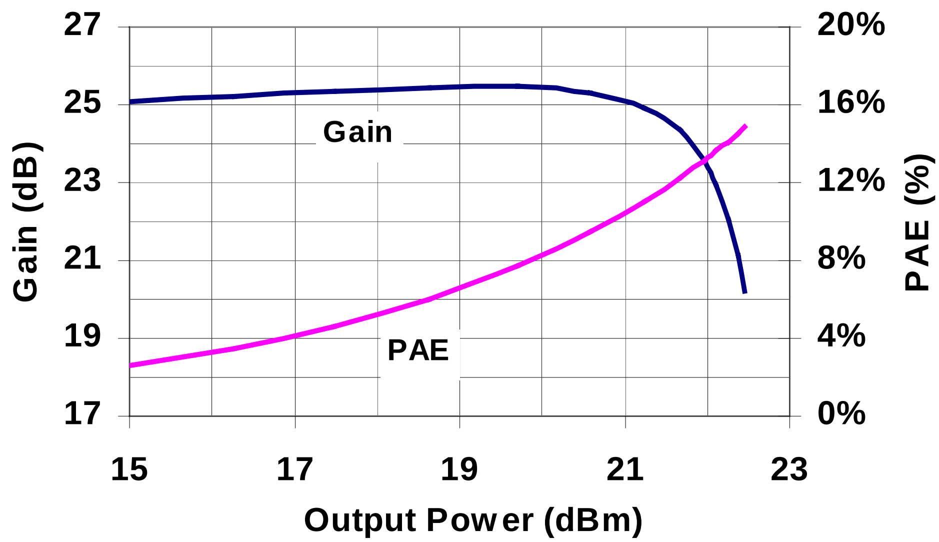
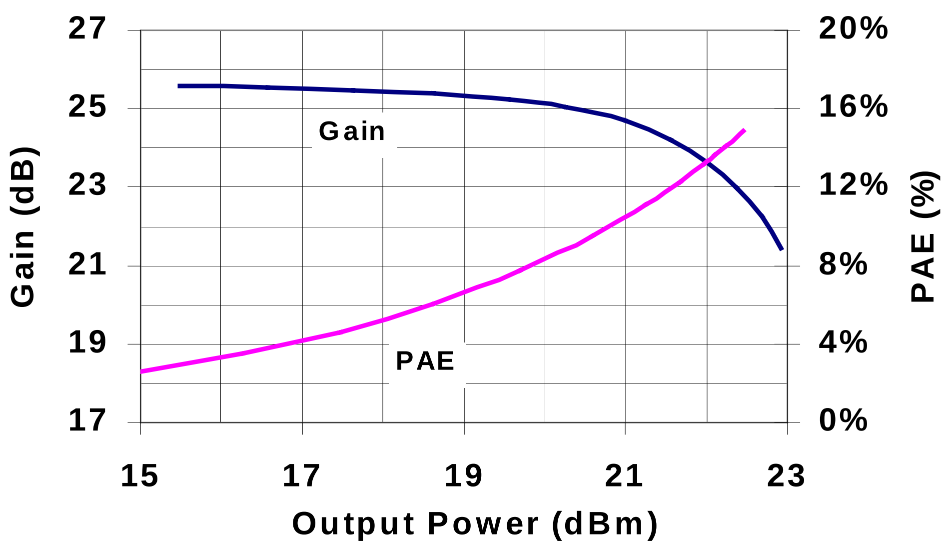
### Performance Data

Gain Compression and PAE vs Output Power
Frequency=40 GHz, Bias Vd=3.5 V, Id=350 mA




Gain Compression and PAE vs Output Power
Frequency=30 GHz, Bias Vd=3.5 V, Id=350 mA

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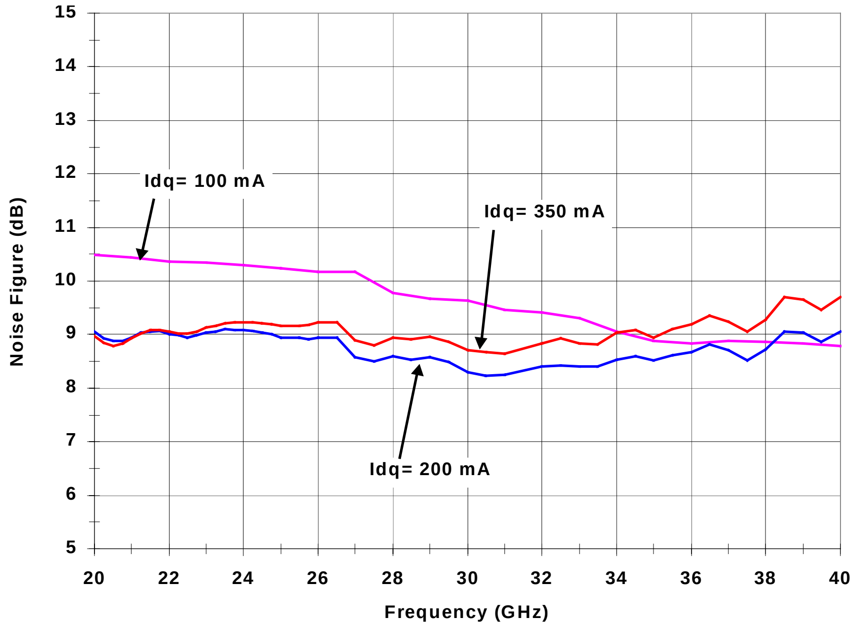
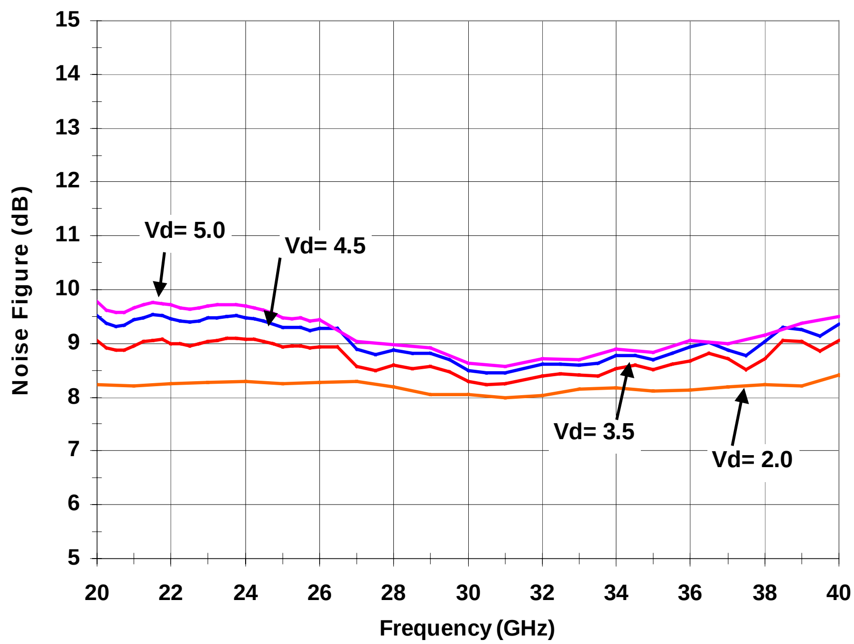
### Performance Data

Noise Figure vs Frequency vs Supply Current
Bias Vd=3.5 Volts




Noise Figure vs Frequency vs Supply Voltage
Supply Current=200mA

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