Raytheon

RMPA0953-103

3V Cellular AMPS and CDMA Power Amplifier Module with Digital Bias Control

ADVANCED INFORMATION

Description

The RMPA0953-103 power amplifier module (PAM) for AMPS, CDMA and **CDMA2000-1X** Cellular applications. The PAM is internally matched to 50 ohms to minimize the use of external components. Advanced DC power management reduces current consumption during peak phone usage at backed-off RF power levels. Advanced Digital Bias control reduces the number of interface components to baseband. High power-added efficiency and excellent linearity are achieved using Raytheon's InGaP Heterojunction Bipolar Transistor (HBT) process.

Features

- Single positive-supply operation and power-down mode
- Low Backed Off current consumption: 65 mA @ 12 dBm output power
- 34% power-added efficiency at +27.4 dBm CDMA average output power
- 48% AMPS power-added efficiency at +30.7 dBm AMPS output power
- Compact LCC package: 6.0 x 8.0 x 1.5 mm^3
- 50 ohm matched and DC blocked input/output
- Advanced Digital Bias Control

Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Units
Supply Voltages	Vcc1, Vcc2, and Vbias	5	V
Bias Voltage 1 and 2	Vba1, Vba2	2.5	V
Chip Enable	Venbl	3.0	V
RF Input Power	Pin	+5	dBm
Case Operating Temperature	Tc	-30 to+85	°C
Storage Temperature	Tstg	-55 to+150	°C

Electrical Characteristics[2]

Parameter	Min	Typ	Max	Unit
Operating Frequency	824		849	MHz
Gain				
(Po=12 dBm)	22		28	dB
(Po=27.4 dBm)	27	30	34	dB
CDMA Output Power		27.4		dBm
CDMA PAE				
(Po=27.4 dBm)		34		%
ACPR1[3]	-47	-52		dBc
ACPR2		-56		dBc
Input VSWR (50Ω)		2.0:1	2.5:1	

Parameter	Min	Typ	Max	Unit
Itotal @ 27.4 dBm Pout		425		mA
Itotal @ 12 dBm Pout		65		mA
Stability (All Spurious)[4]			-65	dBc
AMPS Power Output		30.7		dBm
AMPS PAE		48		%
Harmonics Po ≤ 27.4 dBm 2fo, 3fo, 4fo			-30	dBc
Shutdown Current[4]		<1		uA
Vcc	3.0	3.4	4.6	V

Notes:

1. No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.
2. All parameters met at Tc =+25°C, Vcc =+3.4V, Vref=+2.7V, f=836.5 MHz and load VSWR ≤ 1.2:1.
3. Po ≤ 27.4 dBm at Vcc=3.4V; CDMA Waveform measured using the ratio of average power within a 1.23 MHz channel to average power within a 30 kHz bandwidth at + 885 KHz offset.
4. No applied RF signal. Vcc=+3.4V nominal, Vref=+0.2V maximum.

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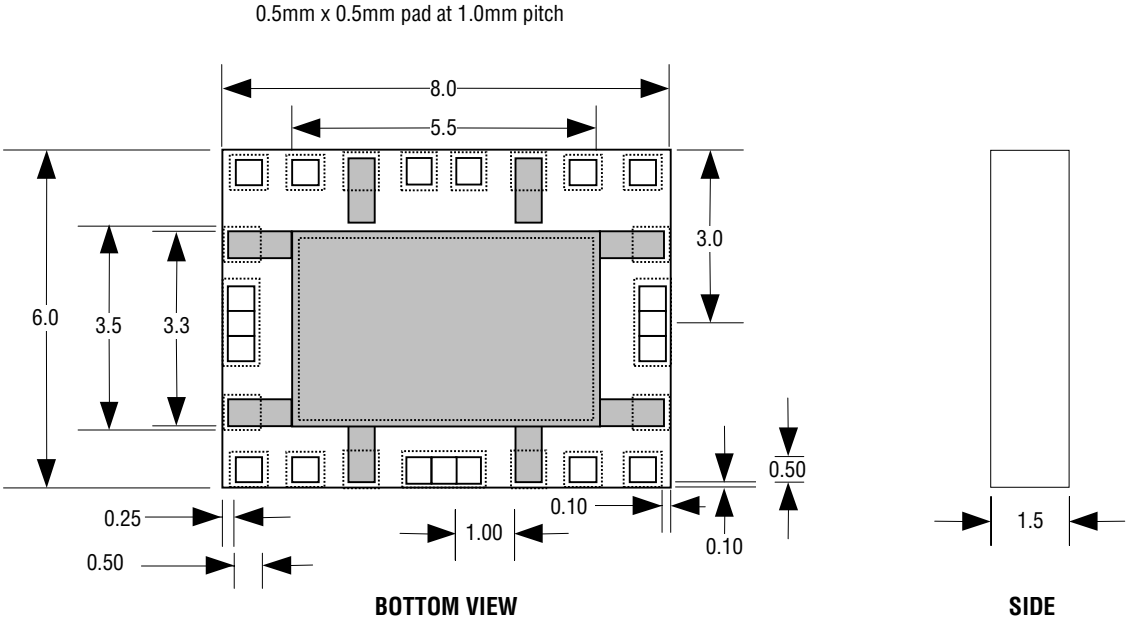
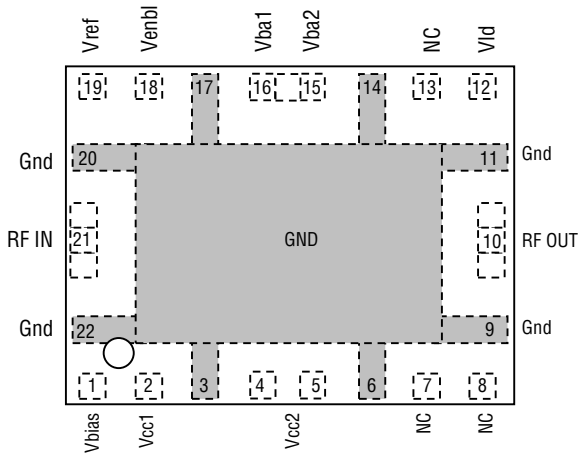
Figure 1
Package Outline and Pin Designations

Dimensions in mm





TOP VIEW
(Through Package)

Pin #	Description
1	Vbias
2	Vcc1
3	GND
4	Vcc1
5	Vcc2
6	GND
7	NC
8	NC
9	GND
10	RF Out
11	GND
12	Vld
13	NC
14	GND
15	Vba2
16	Vcc1
17	GND
18	Venbl
19	Vref
20	GND
21	RF In
22	GND

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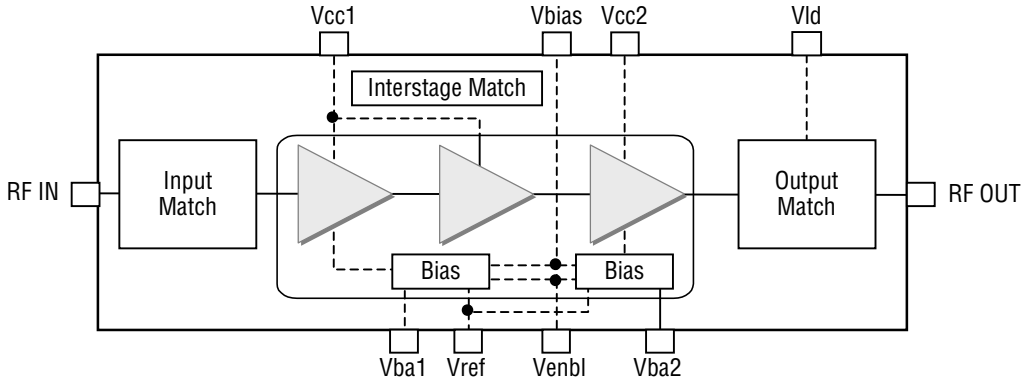
Figure 2
Functional Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply Voltage	Vcc	3.1	3.4	4.5	V
Power Shutdown Mode	$Vref_{off}$	0		0.2	V
RF Input Power[1]	Pin	-89	0	+3	dBm
CDMA Output Power Range	Pout	-55		+29	dBm
Vld High	Vld_Hi	2.5		2.9	V
Vld Low	Vld_Lo		float		V
Bias Control hi	Vba1,2_hi	2.38		2.83	V
Bias Control low	Vba1,2_lo	0.00		0.45	V
Enable Control Voltage high	Venbl_hi	2.38		2.83	V
Enable Contol Voltage low	Venbl_lo	0		0.45	V
Reference Voltage	Vref	2.30	2.9	3.50	V

Operational Control

	Vba1 and Vba2 Pins	Vld Pin (V)	Vcc1,2 and Vbias Pins Tied Together	Venbl Pin (V)	Pout (dBm)	PAE (%) typ.	Itotal (mA) typ.
High Power Operation	2.5V	Lo	3.4 V CDMA High Power	2.7	27.4	34	425
Threshold Power Operation	0V	Hi 2.7	3.4 V CDMA Threshold power for Vld HIGH Switch	2.7	19.0	15	150
Low Power Operation	0V	Hi 2.7	3.4 V CDMA Low Power	2.7	12.0	6	65

Notes:
1. Typical RF input power for CDMA Pout = +27.4 dBm.

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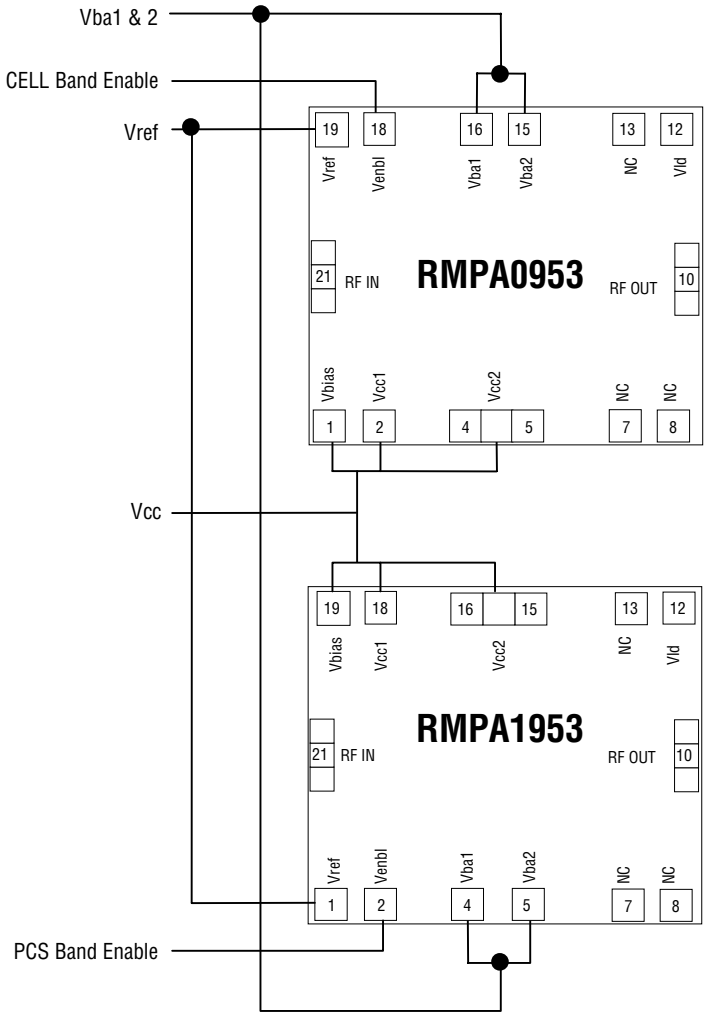
Figure 3
Common Control of Cellular and PCS Band PAs



Application Information

- **Precautions to Avoid Permanent Device Damage:**
  - Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
  - Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
  - Static Sensitivity: Follow ESD precautions to protect against ESD damage:
    - A properly grounded static-dissipative surface on which to place devices.
    - Static-dissipative floor or mat.
    - A properly grounded conductive wrist strap for each person to wear while handling devices.
  - General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
  - Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.
- **Device Usage:** Raytheon recommends the following procedures prior to assembly.
  - Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
  - Assemble the dry-baked devices within 7 days of removal from the oven.
  - During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
  - If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.
- **Solder Materials & Temperature Profile:** Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.
  - **Reflow Profile**
    - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
    - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
    - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
    - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. Figure 1 indicates the recommended soldering profile.
- **Solder Joint Characteristics:** Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.
- **Rework Considerations:** Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

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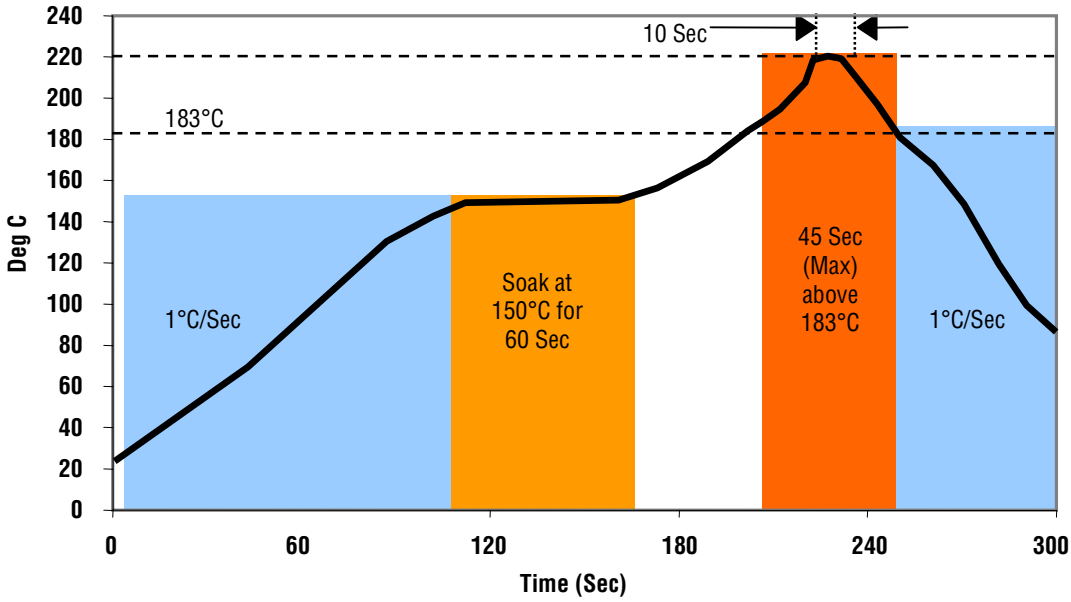
Figure 4
Recommended Solder Reflow Profile



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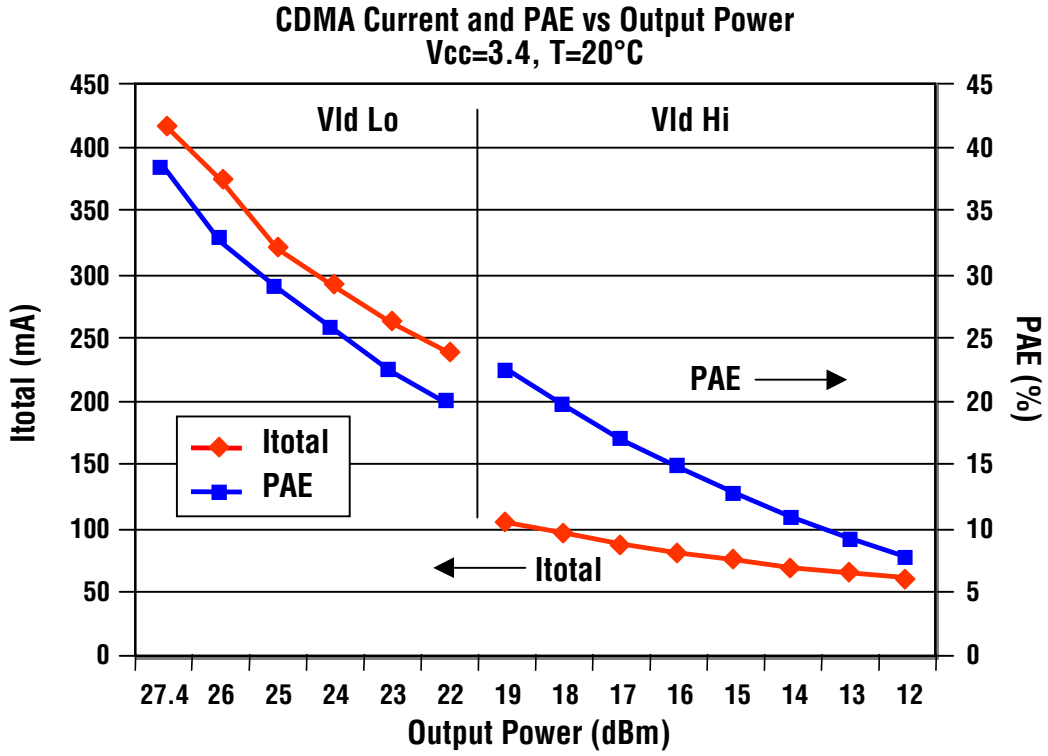
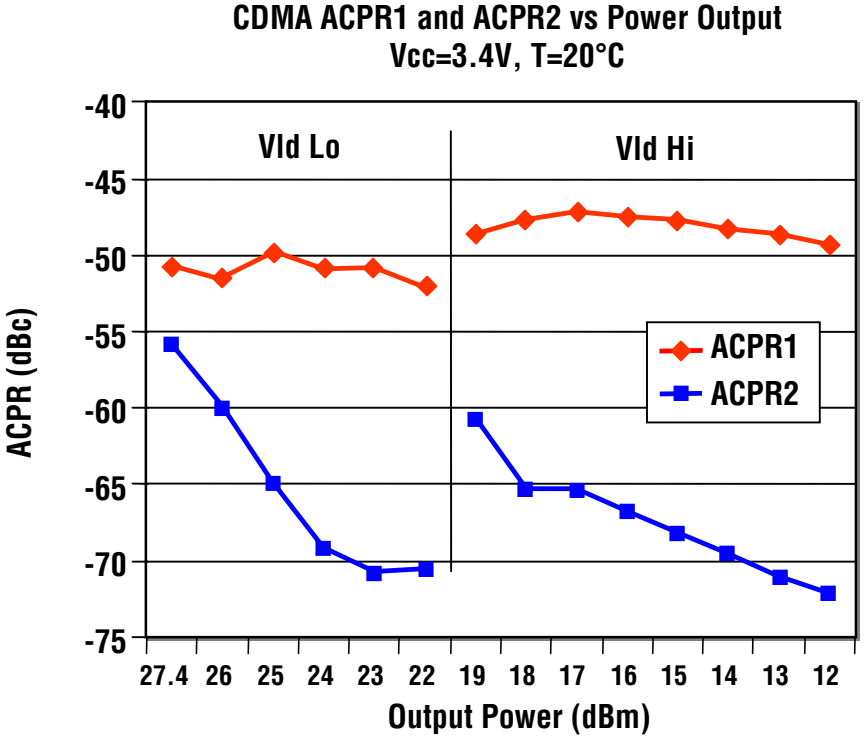
Performance Data





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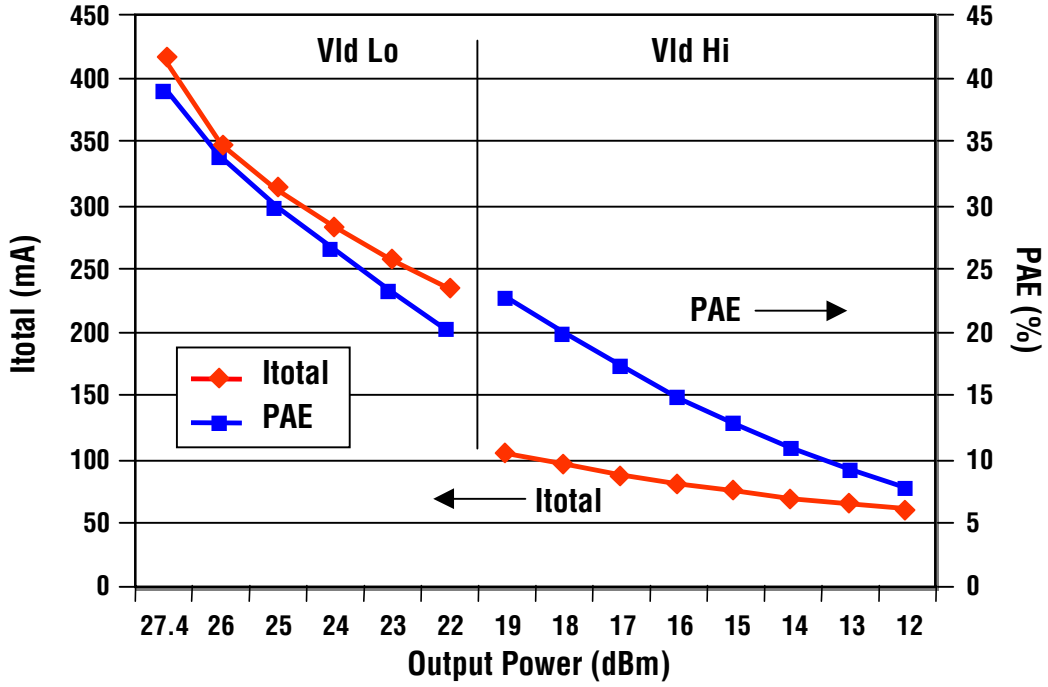
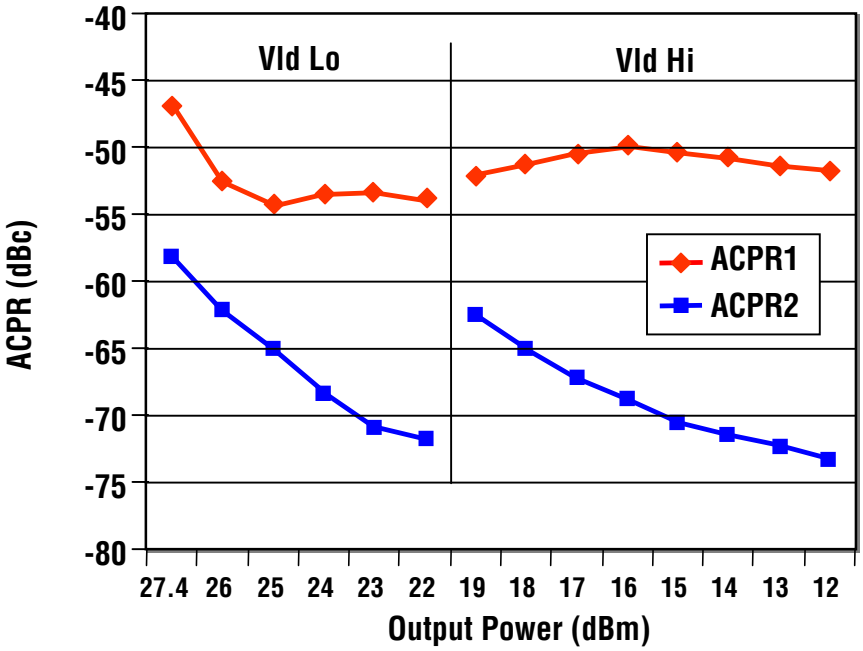
Performance Data

CDMA2000-1x Efficiency and Itotal vs Output Power
Vcc=3.4, T=20°C



CDMA2000-1x ACPR1 and ACPR2 vs Power Output
Vcc=3.4V, T=20°C



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