

RMPA1901-53

PCS CDMA GaAs MMIC Power Amplifier

Description The RMPA1901-53 is a monolithic high efficiency power amplifier for PCS CDMA applications. Performance parameters may be slightly adjusted by “tweaking” the off-chip matching components. The amplifier circuit design is a single ended configuration that utilizes harmonic tuning for increased power added efficiency and linearity. The device uses Raytheon’s Pseudomorphic High Electron Mobility Transistor (pHEMT) process.

- Features**
- Positive supply voltage of 5.8V, nominal
 - Efficiency of 34%, typical, for digital CDMA power out of 28.5 dBm
 - ACPR of 50 dBc, typical, for digital CDMA power out of 28.5 dBm
 - Small outline metal based quad plastic package

Electrical Characteristics	Parameter	Min	Typ	Max	Unit
(Specifications at 25°C unless otherwise stated)	Frequency Range	1850		1910	MHz
		1710		1785	MHz
	Gain (Small Signal)		29		dB
	Gain Variation vs Temp		-0.03		dB/°C
	Gain Linearity (0 dBm ≤ Pout ≤ 28.5 dBm)	-1.0		+1.0	dB
	Noise Power (1930-1990 MHz) (All Power Levels)			-135	dBm/Hz
	Input VSWR (50Ω)			2.0:1	---
	Stability (All spurious) ¹			-70	dBc
	Harmonics (Po ≤ 28.5 dBm) 2fo, 3fo, 4fo			-30	dBc
	Efficiency Po = 800 mW, Vdd=5.8V			34	%
	Po = 40 mW, Vdd=5.8V			5	%
	ACPR (Offset ≤ ± 1.25 MHz) ²			50	dBc
	Noise Figure (over temp.)			7.0	dB
	Quiescent Current			80	mA
	Vdd			5.8	Volts
	Vg1/Vg2, Vg3 (<5 mA) ³	-1.5		-0.3	Volts
Case Operating Temp	-30		+90	°C	

Product Information

Notes:

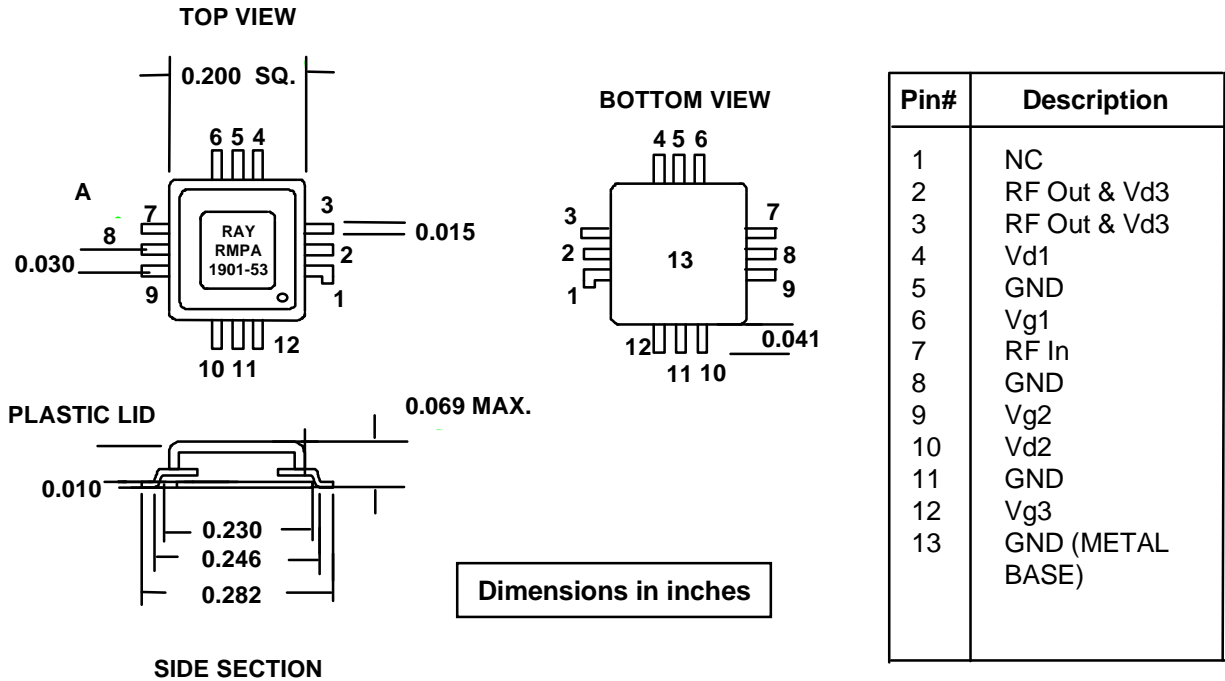
1. Source/Load VSWR ≤ 3:1 (All Angles, -50 dBm < Po < 28.5 dBm) or Load VSWR ≥ 20:1 (Out of Band, All Angles, Tc = -40 to +110°C)
2. Po ≤ 28.5 dBm at Vdd = 5.8V; CDMA Waveform measured using the ratio of the average power within the 1.23 MHz channel and within a 30 kHz bandwidth at a 1.25 MHz offset.
3. Vg1 = Vg2 and Vg3 adjusted for Quiescent Current of Idq1 & Idq2 = 35 mA, and Idq3 = 45 mA.

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Figure 1. Package Data



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CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following describes a procedure for evaluating the RMPA1901-53, a monolithic high efficiency power amplifier, in a surface mount package, designed for use in Personal Communication Systems (PCS) utilizing Code Division Multiple Access (CDMA). Figure 2 shows the functional block diagram of the packaged product. Figure 1 shows the package outline and the pin designations. It should be noted that RMPA1901-53 requires external passive components for DC bias and RF output matching circuits. A recommended schematic of circuits is shown in Figure 3. The gate biases for the three stages of the amplifier are set by simple resistive voltage dividers. Potentiometers R1 to R3 are used to set the required quiescent currents of the amplifier stages. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of figure 3. The following should be noted:

- (1) Pin designations are as shown in figure 2.
- (2) Vg1, Vg2 and Vg3 are the Gate Voltages (negative) applied at the pins of the package
- (3) Vgg1, Vgg2 and Vgg3 are the negative supply voltages at the evaluation board terminals
- (4) Vd1, Vd2 and Vd3 are the Drain Voltages (positive) applied at the pins of the package
- (5) Vdd1, Vdd2 and Vdd3 are the positive supply voltages at the evaluation board terminals

Test Procedure for the evaluation board (RMPA1901-53-TB)**CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2, VG3) WHILE CORRESPONDING DRAIN VOLTAGES (VD1,VD2,VD3) ARE PRESENT MAY DAMAGE THE AMPLIFIER.**

The following sequence must be followed to properly test the amplifier:

- Step 1: Turn off RF input power.
- Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies.
Slowly apply gate supply voltages of typical -2.0 V to the board terminals Vgg1, Vgg2, Vgg3
- Step 3: Slowly apply drain supply voltages of +5.8 V to the board terminals Vdd1, Vdd2, Vdd3
[Gate supply voltages (Vgg1, Vgg2, Vgg3) may be adjusted, only if quiescent current (Idq1 to Idq3) values desired are different from those noted on the data summary supplied with the samples]
- Step 4: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.
- Step 5: Follow turn-off sequence of:
 - (i) Turn off RF Input Power
 - (ii) Turn down and off drain voltages Vdd1, Vdd2 and Vdd3
 - (iii) Turn down and off gate voltages Vgg1, Vgg2 and Vgg3

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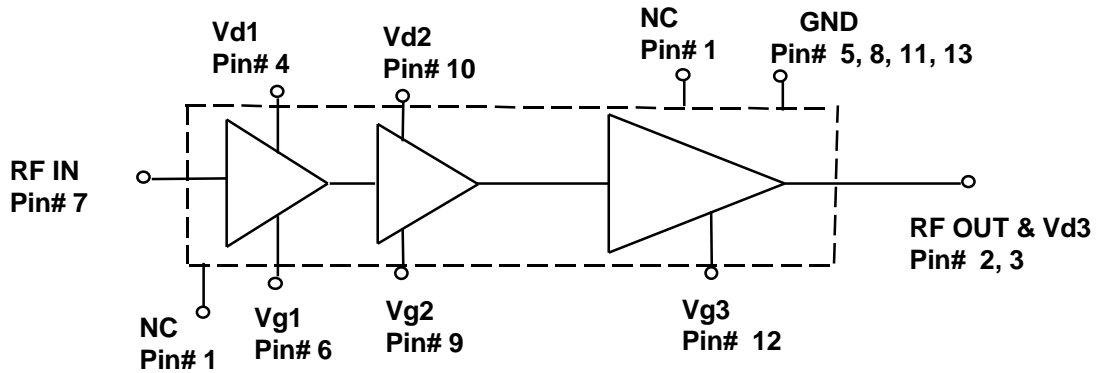
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Maximum Ratings

<u>Parameter</u>	<u>Symbol</u>	<u>Value</u>	<u>Unit</u>
Positive DC Voltage	Vd1, Vd2	+ 9	Volts
Negative DC Voltage	Vg1, Vg2	- 6	Volts
Simultaneous (Vd-Vg)	Vdg	+12	Volts
RF Input Power (from 50-Ohm source)	P _{IN}	+10	dBm
Operating Case Temperature	T _C	-30 to +90	°C
Storage Temperature Range	T _{Stg}	-35 to +110	°C
Thermal Resistance (Channel to case)	R _{Jc}	+18	°C/W

Figure 2: Functional Block Diagram of Packaged Product (RMPA1901-53)

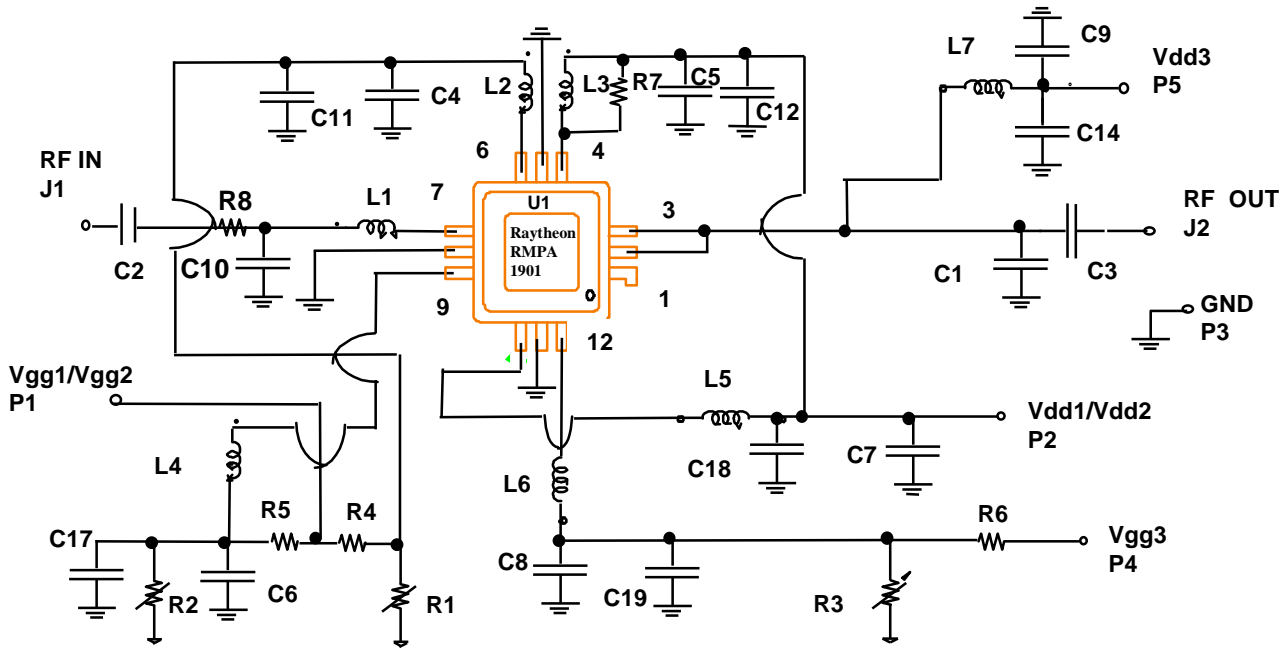


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Figure 3: Schematic for a Typical Test Evaluation Board



PARTS LIST for Test Evaluation Board (RMPA1901-53-TB, G653702)

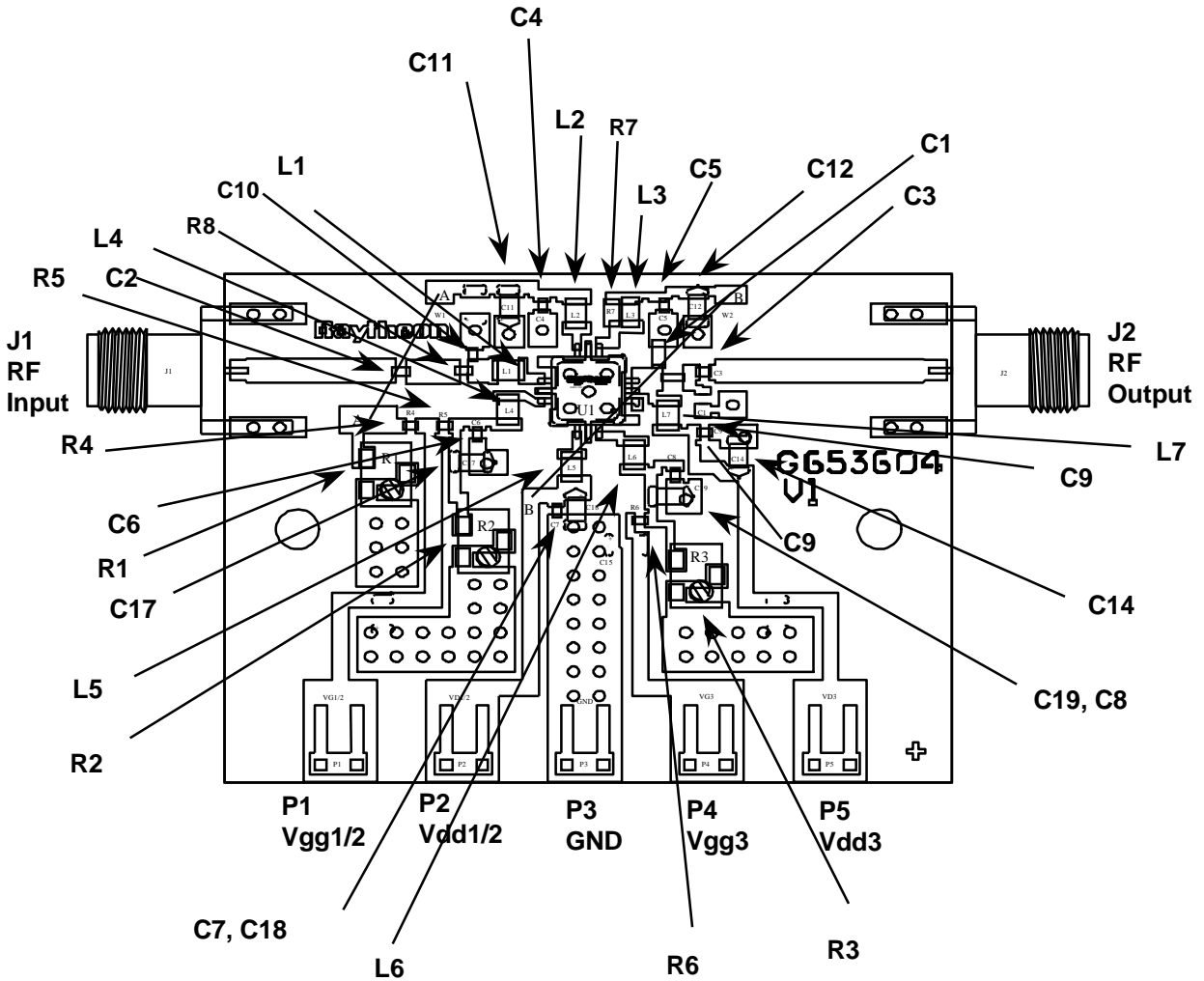
PART	VALUE	SIZE(L"xW")	Vendors
L1	5.6 nH	.08" x .05"	Taiyo Yuden, Toko, KOA
L2, L3	15 nH	.08" x .05"	Taiyo Yuden, Toko, KOA
L4-L7	12 nH	.08" x .05"	Taiyo Yuden, Toko, KOA
C1	2.2 pF	.06" x .03"	AVX, Murata, Novacap, Johanson
C2, C3	10 pF	.06" x .03"	AVX, Murata, Novacap, Johanson
C4-C9	1000 pF	.04" x .02"	AVX, Murata, Novacap, Johanson
C10	1.0 pF	.06" x .03"	AVX, Murata, Novacap, Johanson
C14	4.7 uF	.125"x.06	TDK, ATC, AVX, Murata, Novacap, Johanson
C11,C12,C17-C19	4.7 uF or 0.1 uF optional	.125"x.06 .08" x .05"	TDK, ATC, AVX, Murata, Novacap, Johanson AVX, Murata, Novacap, Johanson
R1-R3	0-5K Ohms		IMS, Venkel, Amitron
R4-R6	510 Ohms	.04" x .02"	IMS, Venkel, Amitron
R7, R8	10 Ohms	.04" x .02"	IMS, Venkel, Amitron
U1	RMPA1901-53	.31" x .41	Raytheon, G652367
P1-P5	Terminals		Samtec
W1, W2	26 AWG wire		
J1, J2	SMA Connectors		E.F. Johnson
Board	FR4		Raytheon Dwg# G653604

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Figure 4 : Layout of Test Evaluation Board (RMPA1901-53-TB)



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