Raytheon

RMPA39000

37-40 GHz GaAs MMIC Power Amplifier

ADVANCED INFORMATION

Description

The Raytheon RMPA39000 is a high efficiency power amplifier designed for use in point to point radio, point to multi point communications, LMDS and other millimeter-wave applications. The RMPA39000 is a 3-stage GaAs MMIC amplifier chip utilizing Raytheon's advanced 0.15 µm gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.

Features

- 15 dB Gain at Pin (-10 dBm)
- 15% Power Added Efficiency
- 28 dBm Saturated Power Output (typ)

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Positive DC Voltage (5V Typical)	Vd	+ 6	Volts
Negative DC Voltage	Vg	- 2	Volts
Simultaneous (Vd-Vg)	Vdg	+ 8	Volts
RF Input Power (from 50 ohm source)	P_{IN}	+20	dBm
Operating Base plate Temperature	T_C	-30 to +90	°C
Storage Temperature Range	T_{Stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R_{jc}	15	°C/W

Electrical Characteristics

50 ohm system, Vd = +5V, Quiescent current = Idq = 700 mA

Parameter	Typ	Unit
Frequency Range	37 - 40	GHz
Gate Supply Voltage (Vg)[1]	- 0.15	V
Drain Supply Voltage (Vd)	+ 5	V
Quiescent Gate Current (Ig)	< 0.1	mA
Quiescent Drain Supply Current (Idq)[2]	700	mA
Gain at Pin = -10 dBm	15	dB
Gain Variation vs Frequency	+/-1	dB
Power Output at Pin = 0 dBm	15	dBm
Power Output at 1 dB Compression	27	dBm

Parameter	Typ	Unit
Power Output (Saturated)	28	dBm
Drain Current at Pin = -10 dBm	700	mA
Drain Current at Pin = 0 dBm	700	mA
Drain Current at P1 dB Compression	750	mA
Drain Current at Saturated Pout	750	mA
Power Added Efficiency (PAE): at P1 dB	15	%
Input Return Loss (Pin = -10 dBm)	8	dB
Output Return Loss (Pin = -10 dBm)	7	dB

Notes:
1. Typical range of the negative gate voltages is -0.3 to 0.0V to set typical Idq of 700 mA.
2. Typical range of Idq is 500 to 900 mA to achieve the desired P1 dB.

Characteristic performance data and specifications are subject to change without notice.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012” long corresponding to a typically 2 mils gap between the chip and the substrate material.

Figure 1
Functional Block Diagram

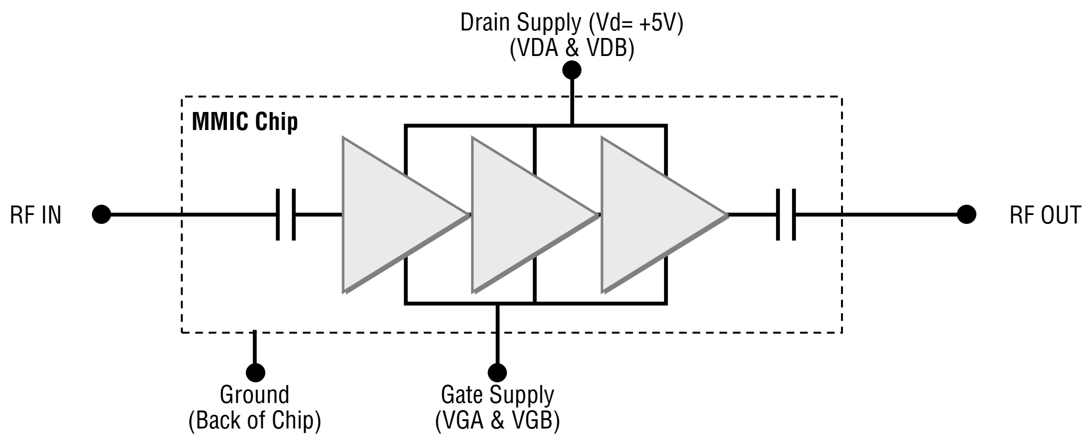

Figure 2
Chip Layout and Bond Pad Locations

(Chip Thickness=0.002”. Back of Chip is RF and DC Ground)

Dimensions in inches

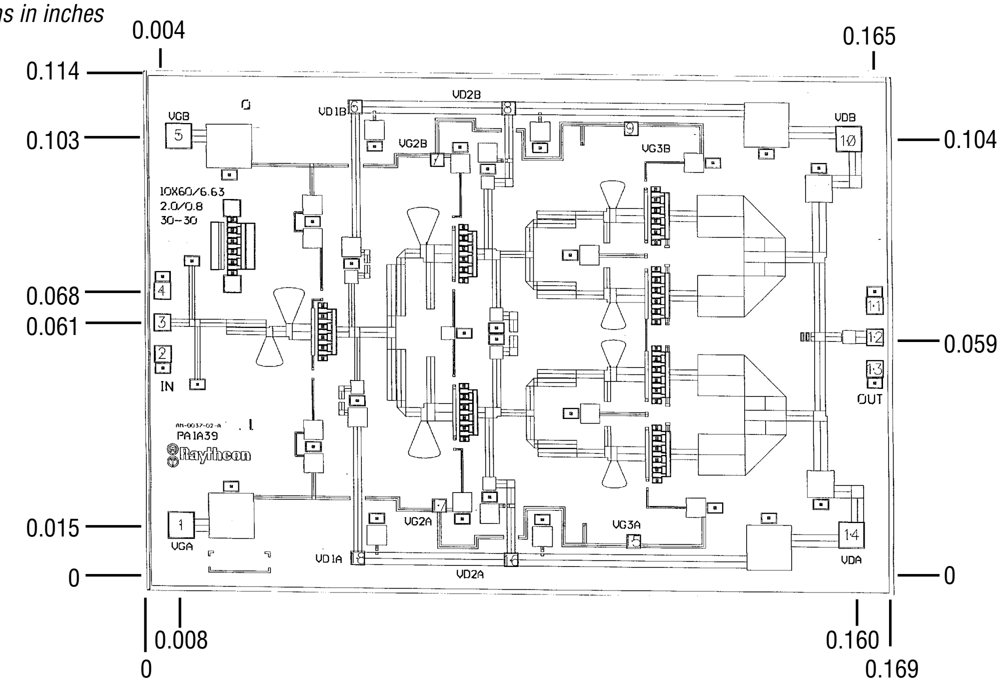

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Figure 3
Recommended Application Schematic Circuit Diagram

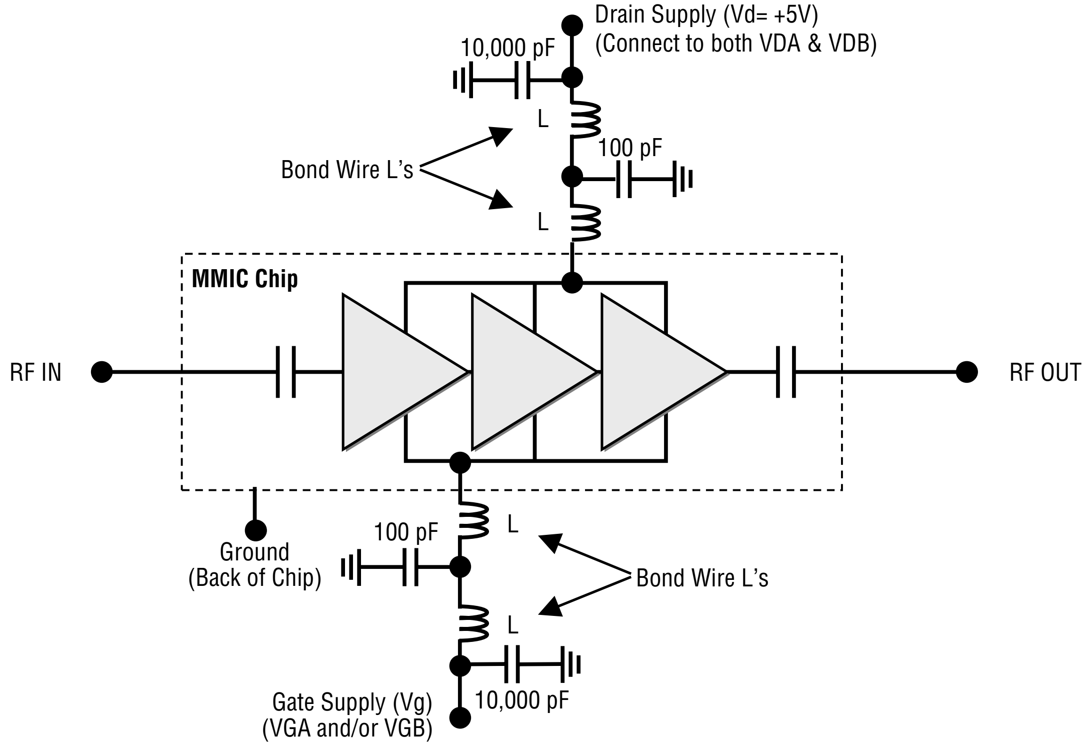
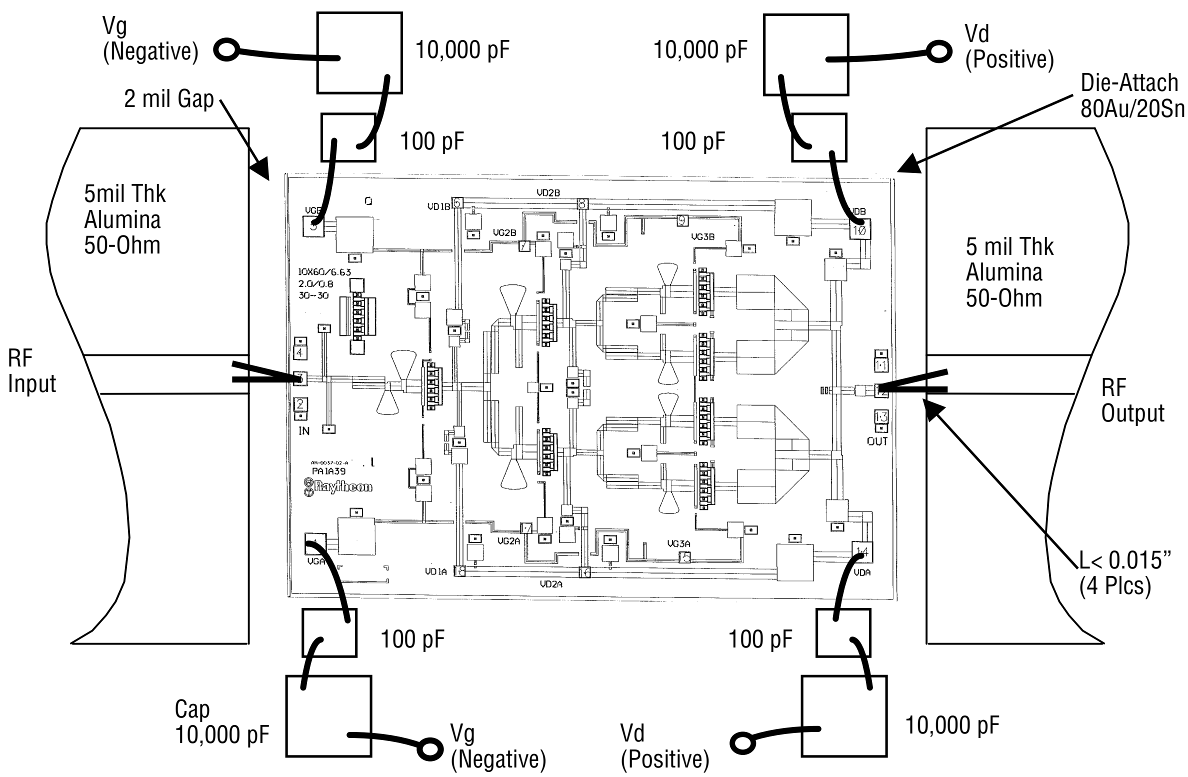


Figure 4
Recommended Assembly and Bonding Diagram



Note:
Use 0.003" x 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

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Recommended Procedure
for biasing and operation

CAUTION: LOSS OF GATE VOLTAGES (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power

Step 2: Connect the DC Supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vg

Step 3: Slowly apply positive drain bias supply voltage of +5 V to Vd

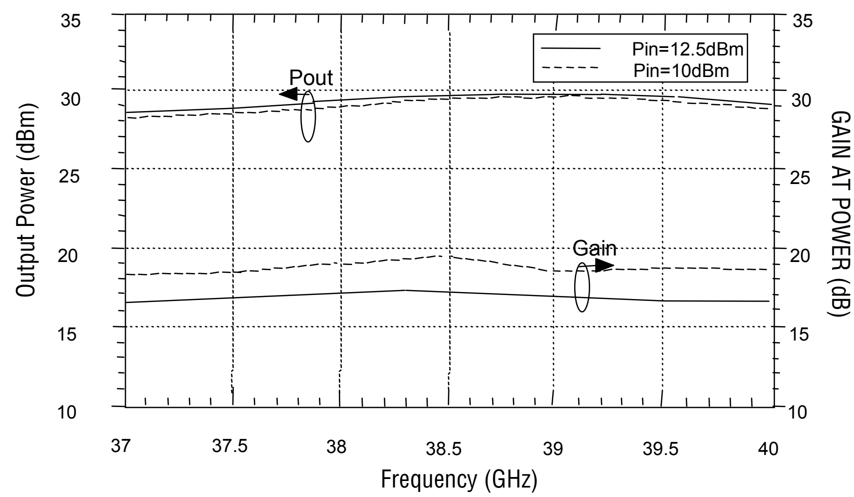
Step 4: Adjust gate bias voltage to set the quiescent current of Idq=700 mA

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

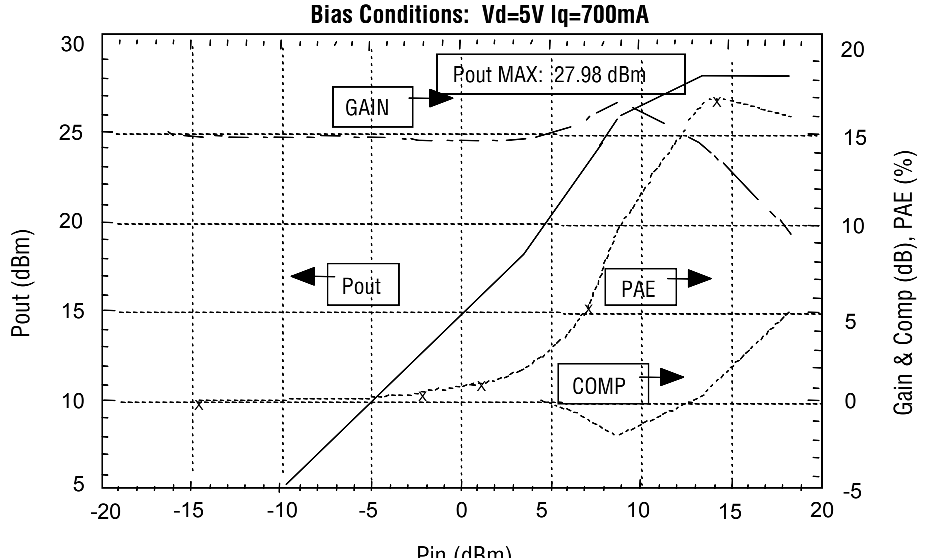
Step 6: Follow turn-off sequence of:
(i) Turn off RF input power
(ii) Turn down and off drain voltage (Vd)
(iii) Turn down and off gate bias voltage (Vg)

Performance Data

Output Power and Gain Measurements
f=39 GHz. Vd:5.0V. Vg:-0.17V. Iq: 700mA.



Output Power, Power Added Efficiency, Gain and Compression
Bias Conditions: Vd=5V Iq=700mA



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