

RMPA61800

Dual-Channel 6-18 GHz 2 Watt Power Amplifier MMIC

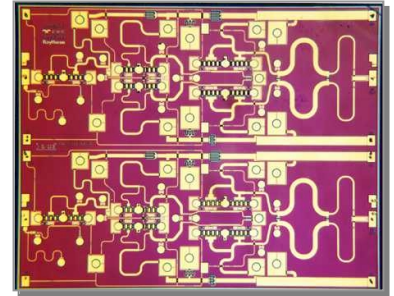
PRELIMINARY INFORMATION

Description

The Raytheon RMPA61800 is a fully monolithic dual channel power amplifier operating over the 6.0 to 18.0 GHz frequency band. The amplifier uses a .25 micron Pseudomorphic High Electron Mobility Transistor (PHEMT) process to maximize efficiency and output power. The chip configuration incorporates two stages of reactively combined amplifiers at the output preceded by an input amplifier stage. Two identical amplifier channels are provided to achieve a typical total combined (using an off-chip combiner) output power of 33 dBm at 3 dB gain compression. A single channel provides typically, 18 dB small signal gain and 31 dBm output power at 1 dB gain compression.

Features

- ◆ Two Identical Channels
- ◆ 21.0 dB Typical Small Signal Gain, Single Channel
- ◆ 2.0:1 Typical Input SWR, 2.5:1 Typical Output SWR, Single Channel
- ◆ 31 dBm Output Power at 1 dB Gain Compression, Single Channel
- ◆ 32 dBm Output Power at 3 dB Gain Compression, Single Channel
- ◆ 34 dBm Output Power at 1 dB Gain Compression, Dual Channel
- ◆ 22% Typical Power Added Efficiency at 1 dB Gain Compression
- ◆ Chip size: 6.55 mm x 5.15 mm x 0.1 mm



Absolute Maximum Ratings

(Single Channel)

Parameter	Symbol	Value	Unit
Positive Drain DC Voltage	V _d	8.5	V
RF CW Input Power	P _{in}	27	dBm
Drain Current	I _d	1.2	A
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{storage}	-40 to 110	°C

Electrical Characteristics

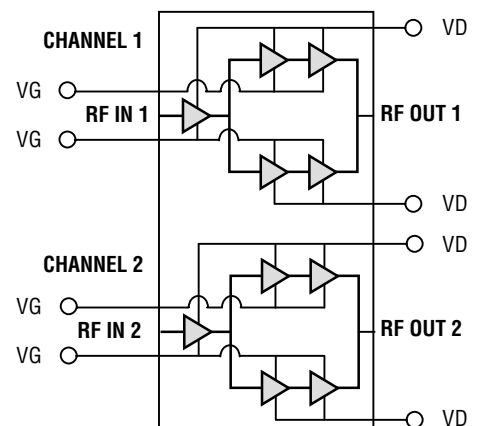
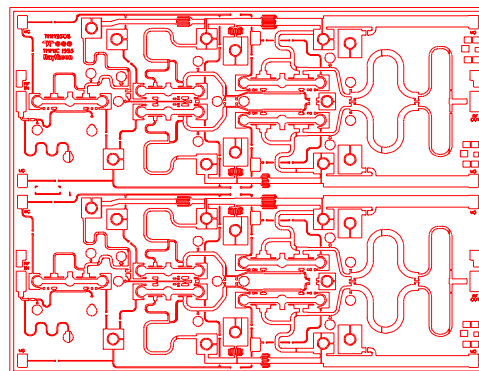
(Single Channel)

Parameter	Min	Typ	Max	Unit
Frequency Range	6.0		18.0	GHz
Small Signal Gain	15	21		dB
P1dB Compression	28	31		dBm
P3dB Compression	30	32		dBm
PAE at 1 dB Gain Comp.	12	22		%
Input Return Loss		9.5		dB
Output Return Loss		7.4		dB

Parameter	Min	Typ	Max	Unit
Gate Voltage (VG)		-0.4		VDC
Gain vs. Temp. 0~85°C		-0.025		dB/°C
Thermal Resistance @ T _{bc} =80°C (T _{bc} =Temp. @ back of chip)		6.2/2 channels		°C/W
Maximum Safe Operating Channel Temp.		150		°C

Note: Quiescent Bias V_D = +8V, I_D = 600mA/channel, T_C = +25°C.

Layout and Schematic



Characteristic performance data and specifications are subject to change without notice.

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Application Note

Scope:

This application note briefly describes the procedure for evaluating the Raytheon RMPA-61800, high efficiency .25um PHEMT Dual-Channel Amplifier. The chip configuration incorporates two stages of reactively combined amplifiers at the output preceded by an input amplifier stage.

Carrier Assembly:

The attached drawing shows a recommended off chip bias scheme for the RMPA-61800. The MMIC is mounted on a Cu shim or ridge, which in turn blazed to Cu-Mo-Cu, or Cu-W, or Mo carrier with alumina Lange coupler for divider and combiner RF circuit and off-chip DC bias components. The drawing shows the placement of components and bond wire connections. The following should be noted:

- (1) 1 mil gold bond wires are used on the carrier assembly.
- (2) Use 3-1 mil gold wires about 25 mils in length for optimum RF performance.
- (3) VG: Gate Voltage (negative) input terminal for amplifier stages. For best results, the gate supply should have a source resistance less than 100 ohms.
- (4) VD: Drain Voltage (positive) input terminal for amplifier stages.
- (5) VG and VD on both sides of the MMIC must be biased to insure proper operation.
- (6) Bias decoupling capacitors of 0.01 uF (multilayer) and 100 pF (single layer) are used on the carrier.
- (7) Close placement of external components is essential to stability.
- (8) The test fixture should incorporate a pair of 25 uF capacitor on the drain and gate(optional) bias terminals to prevent oscillations caused by the test fixture.
- (9) For Laboratory testing uses good power supplies, set current limits on supplies to RF drive-up current level, keep supply wire/leads as short as possible and if required use additional bypass capacitors at the fixture terminals:
 - (i) RF input power=off,
 - (ii) VD=off,
 - (iii) VG=off.

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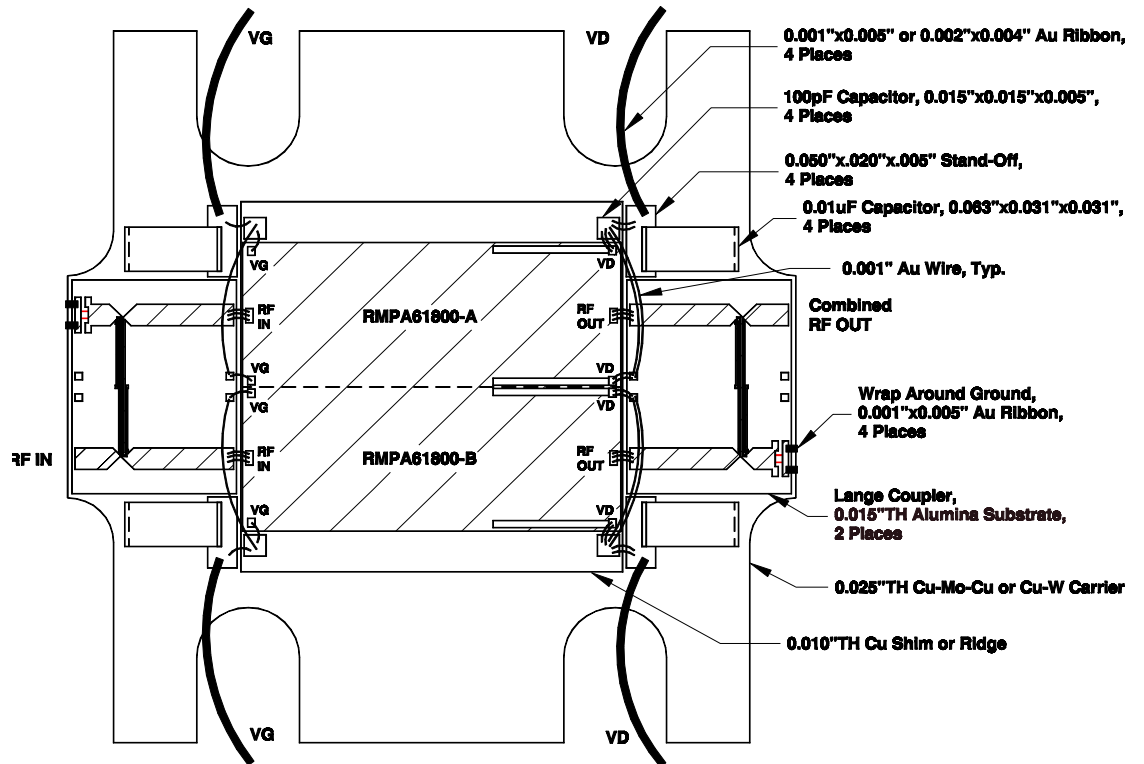
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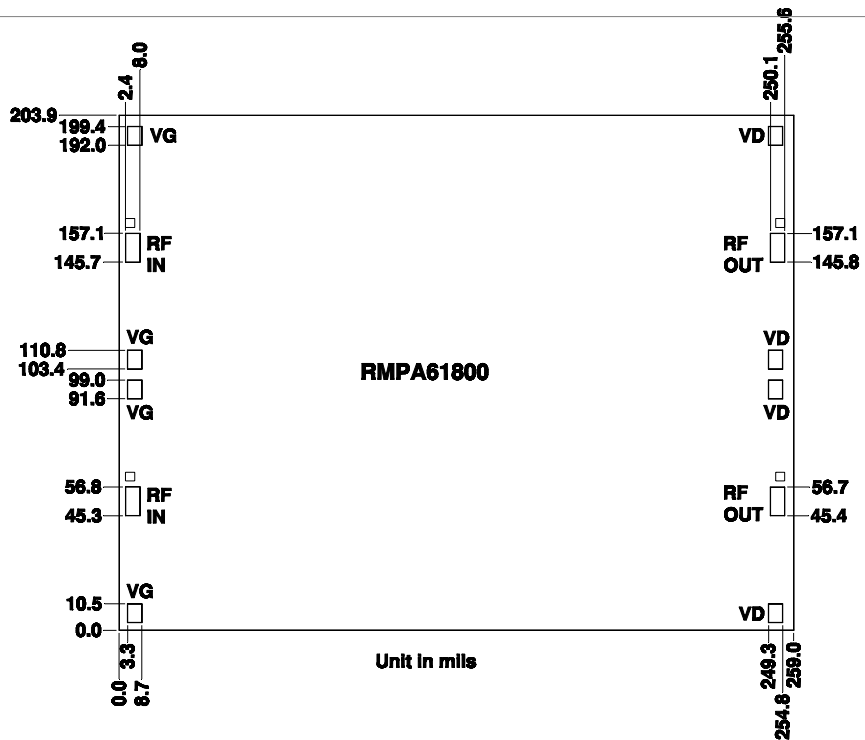
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Example of Assembled Combiner Module



Bonding Pads



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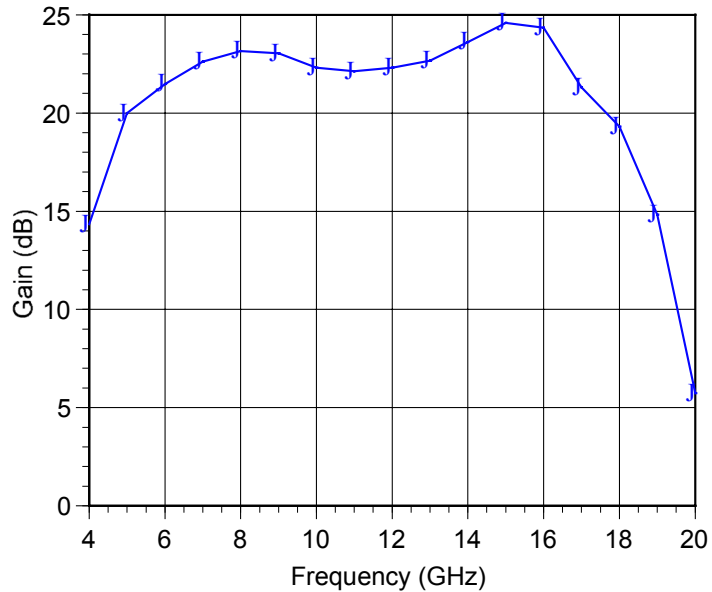
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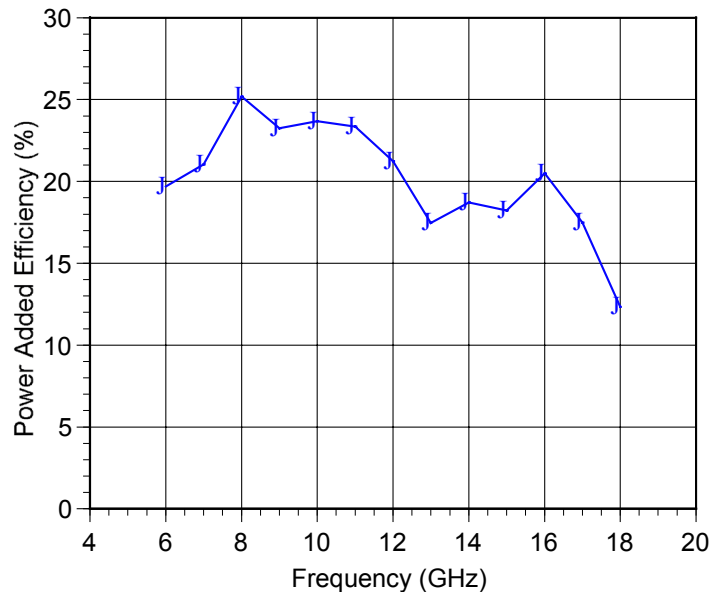
PRELIMINARY INFORMATION

Typical Two Channels Combined Characteristics

Small Signal Gain
Vd=8.0V, Idq=1.2A



Power Added Efficiency @ P1
Vd=8.0V, Idq=1.2A



The above data is derived from fixtured measurements which includes 3 parallel, 1 mil diameter, 15 mil long, gold bond wires connected to the RF input and output.

The Id @ 1 dB compression increases to 2 A or thereabouts. The dc supply should be able to support the required current to achieve the above performance.

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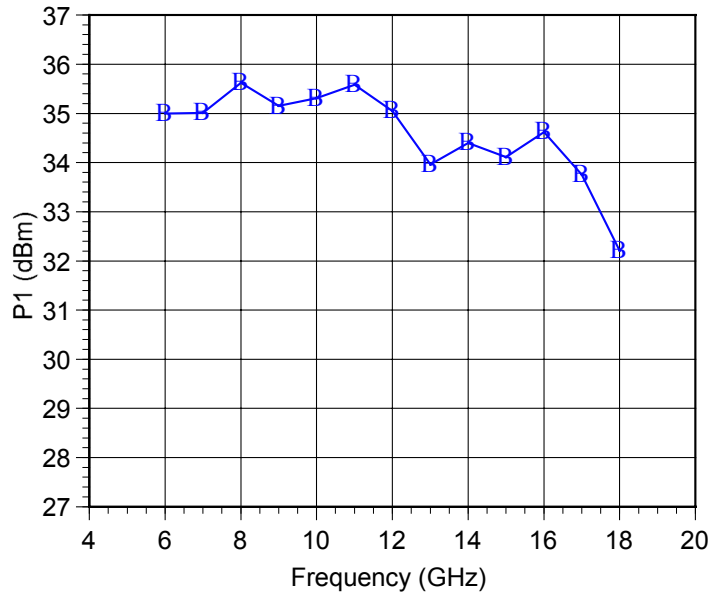
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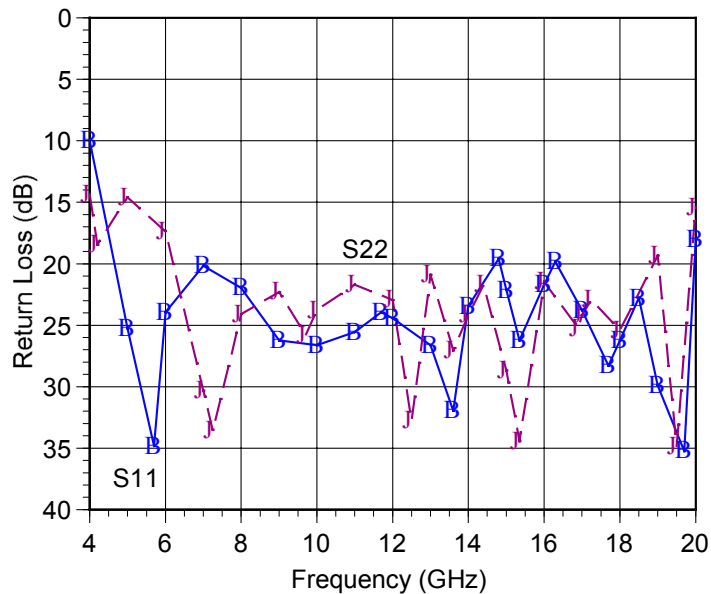
PRELIMINARY INFORMATION

Typical Two Channels Combined Characteristics

Output Power @ 1dB Compression
Vd=8.0V, Idq=1.2A



Input and output Return Loss
Vd=8.0V, Idq=1.2A



The above data is derived from fixtured measurements which includes 3 parallel, 1 mil diameter, 15 mil long, gold bond wires connected to the RF input and output.

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Test Procedure

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER. THIS AMPLIFIER IS AN ESD SENSITIVE DEVICE.

The following procedure must be followed to properly test the amplifier:

- Step 1** Slowly apply Gate Voltage (typical $V_{\text{pinch-off}} = -1.5\text{V}$) to terminal VG.
- Step 2** Slowly apply Drain Voltage at VD (<+5 volts) and monitor drain current I_{ds} . Adjust negative voltage VG to set the drain current (I_{ds}) to approximately 1.2 A. Adjust the drain voltage VD to nominal +8 volts (adjust Gate Voltage VG, if needed, to maintain the drain current at I_{ds}).
- Step 3** After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.
- Step 4** Follow Turn-off sequence:
(i) RF input power=off,
(ii) VD=off,
(iii) VG=off.

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