

RMTR13390

13-39 GHz Tripler MMIC

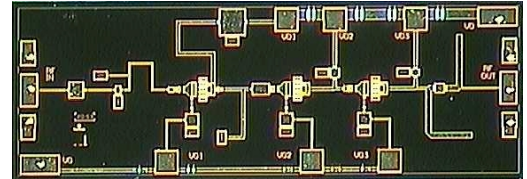
ADVANCED INFORMATION

Description

The RMTR13390 is a 13 to 39 GHz Tripler designed to be used in the LO chain of point to point radios, point to multi-point communications, LMDS, and other millimeter wave applications. The RMTR13390 is a three stage amplifier in which the first stage acts as a harmonic generator followed by two stages of amplification at 3Fo. The RMTR13390 utilizes Raytheon's advanced 0.15 μm gate length PHEMT process and is sufficiently versatile to serve in a variety of multiplier applications.

Features

- ◆ 2 mil substrate
- ◆ Conversion Loss 5 dBm (typ.)
- ◆ Wide operating bandwidth
- ◆ Chip size 3.224 mm x 1.134 mm



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Positive DC Voltage (+5 V Typical)	Vd	+ 6	Volts
Negative DC Voltage	Vg	- 2	Volts
Simultaneous (Vd - Vg)	Vdg	+ 8	Volts
Positive DC Current	Id	187	mA
RF Input Power (from 50 Ω source)	P _{IN}	+22	dBm
Operating Baseplate Temperature	T _C	-30 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T _{stg}	-55 to +125	$^{\circ}\text{C}$
Thermal Resistance (Channel to Backside)	R _j	117	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics

(At 25 $^{\circ}\text{C}$), 50 Ω system, Vd = +5 V, Quiescent current (Idq) = 100 mA, Pin = +17 dBm

Parameter	Min	Typ	Max	Unit
Input Frequency Range	12		13.5	GHz
Output Frequency Range	36		40.5	GHz
Gate Supply Voltage (Vg) ¹		- 0.2		V
Input Drive Power @ Fo	+15	+17		dBm
Output Power @ 3Fo		+12		dBm

Parameter	Min	Typ	Max	Unit
Conversion Loss		5		dBm
Fundamental Rejection		-15		dBc
2nd Harmonic Rejection		-25		dBc
4th Harmonic Rejection		-25		dBc
Input Return Loss		8		dB
Output Return Loss		7		dB

Note: 1. Typical range of the negative gate voltage is -0.5 to 0.0V to set typical Idq of 100 mA.

Characteristic performance data and specifications are subject to change without notice.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typically 2 mil between the chip and the substrate material.

Figure 1
Functional Block Diagram

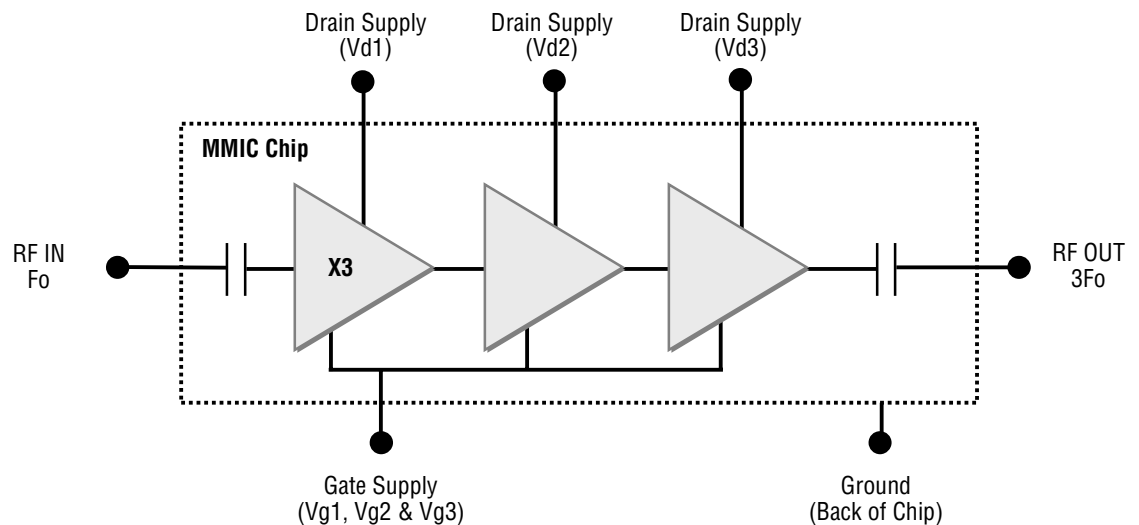
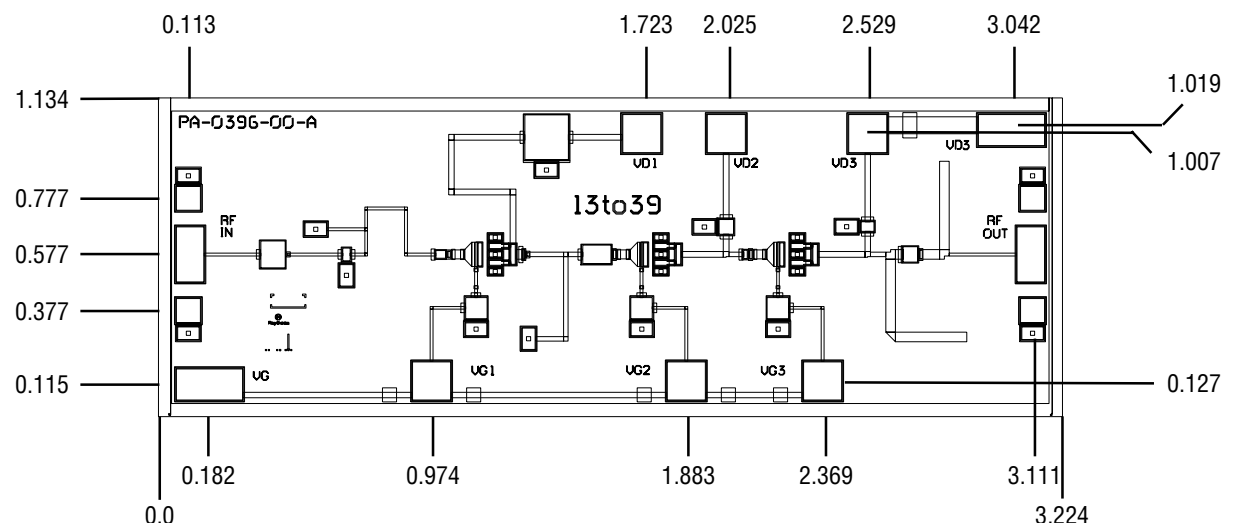


Figure 2
Chip Layout and Bond Pad Locations

Chip Size is 3.224 mm x 1.134 mm. Back of chip is RF ground.

Dimensions in mm

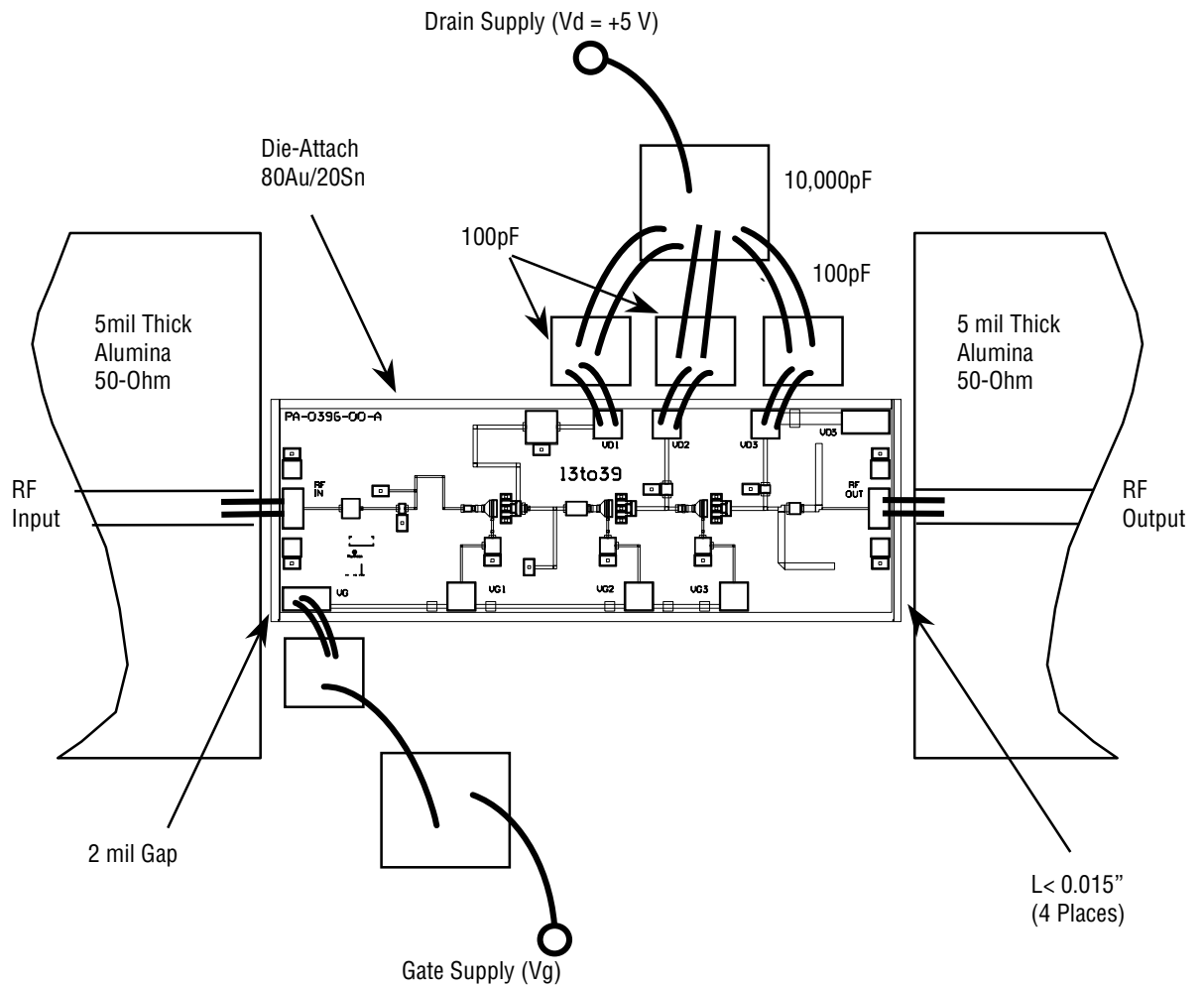


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Figure 4
Recommended
Assembly Diagram



Note: Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

Recommended Procedure
for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

- Step 1:** Turn off RF input power.
- Step 2:** Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vg.
- Step 3:** Slowly apply positive drain bias supply voltage of +5 V to Vd.
- Step 4:** Adjust gate bias voltage to set the quiescent current of Idq=100 mA.

- Step 5:** After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.
- Step 6:** Follow turn-off sequence of:
 - (i) Turn off RF input power.
 - (ii) Turn down and off drain voltage (Vd).
 - (iii) Turn down and off gate bias voltage (Vg).

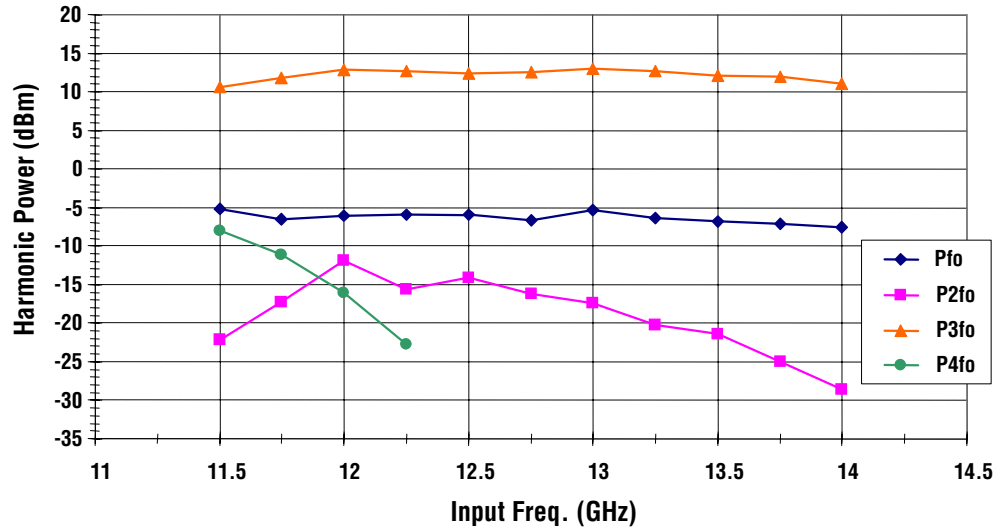
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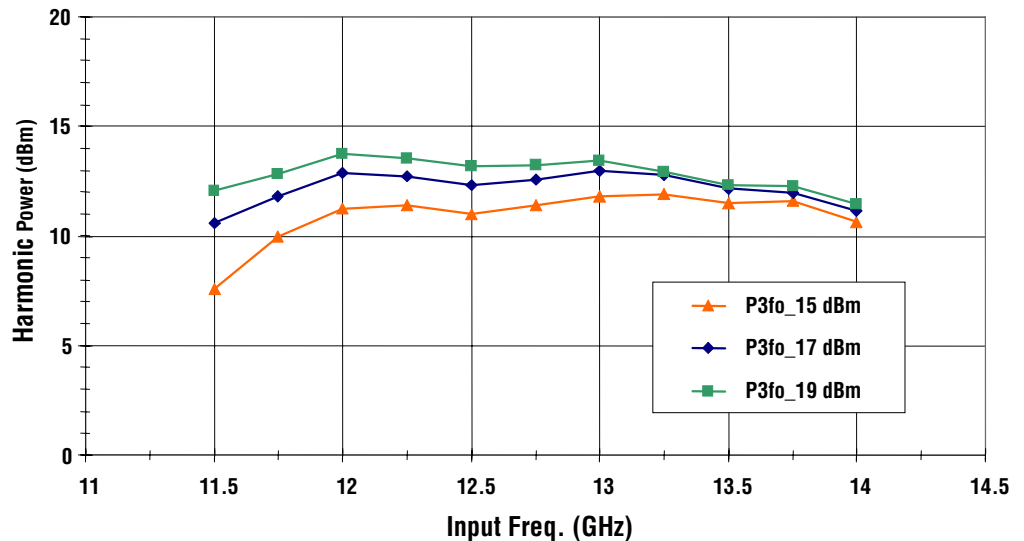
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Performance Data

RMTR13390 Fixtured Data
 Vd = 5V Vg = -0.25V Id = 98 mA w/o RF
 All Gates and Drains Separated on chip
 Pin = 17 dBm



RMTR13390 Fixtured Data
 Vd = 5V Vg = -0.25V Id = 98 mA w/o RF
 All Gates and Drains Separated on chip
 Pin = 15, 17 & 19 dBm



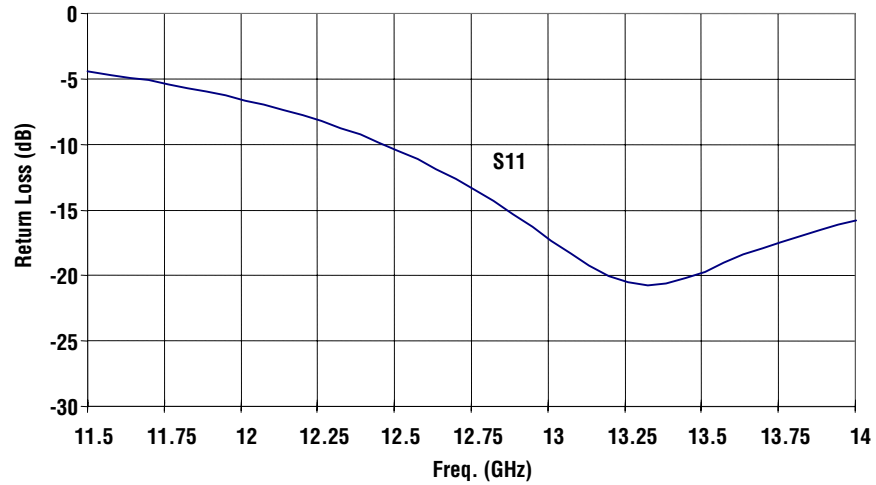
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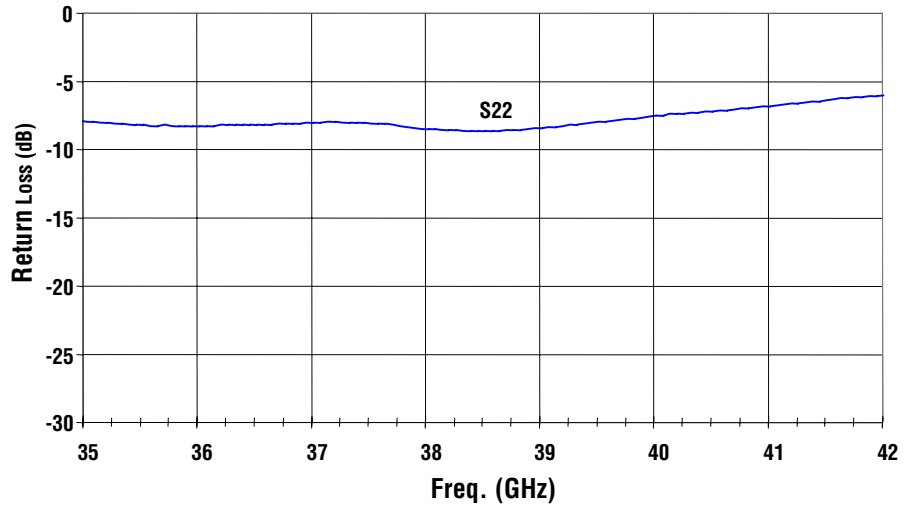
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Performance
Data

RMTR13390 Fixtured Data
 $V_d = 5V$ $V_g = -0.25V$ $I_d = 100\text{ mA}$ w/o RF
 All Gates and Drains Separated on chip (S)



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 $V_d = 5V$ $V_g = -0.25V$ $I_d = 100\text{ mA}$ w/o RF
 All Gates and Drains Separated on chip (S)



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