

## PRODUCT INFORMATION

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Description	The RMWD38001 is a 4-stage GaAs MMIC amplifier designed as a 37 to 40 GHz Driver Amplifier for use in point to point radios, point to multi-point communications, LMDS, and other millimeter wave applications. In conjunction with other Fairchild Semiconductor amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWD38001 utilizes Fairchild Semiconductor's 0.25µm power PHEMT proceoss and is sufficiently versatile to serve in a variety of driver amplifier applications.											
Features	<ul> <li>1dB comp</li> <li>Voltage de</li> </ul>	trate nal gain 25 c ressed Pout tector inclu 3.0 mm x 1.	: 18 dE ded to	Sm (typ.)	out						۰ ۲	
Absolute		Parameter				Syml	hol	Value		Units		
Raings	Ratings							+6		Volts		
		Positive DC voltage (+4 V Typical) Negative DC voltage				Vd Vg Vdg		-2	Volts			
	Simultaneous (Vd - Vg)				8							
		Positive DC Current RF Input Power (from 50 $\Omega$ source)				I <sub>D</sub> 173 P <sub>IN</sub> +8			mA			
								dBm				
		Operating	Basepla	ate Temperat	ture	T <sub>c</sub>		-30 to +85		°C		
		Storage Te	mperat	ure Range		T <sub>ste</sub>	9	-55 to +125		°C		
		Thermal Resistance (Channel to Backside)			R <sub>jc</sub>	:	126		°C/W			
Electrical							_					
Characteristics	Parameter		Min	Тур	Max	Unit	Par	rameter	Min	Тур	Max	Unit
(At 25 °C 50Ω	Frequency Rar	nge	37		40	GHz		in Current at Saturated:		100		
system, Vd=+4 V,	Gate Supply Voltage (Vg) <sup>1</sup>			-0.4		V		Pin = -5.5 dBm		120		mA
Quiescent Current	Gain Small Sig			0.5				wer Added Efficiency (PAE): at P1 dB		13		%
(Idq)= 105 mA	Pin = -10 dI		21	25		dB		ut Return Loss		10		,,,
	Gain Variation vs Frequency		;y	2		dB		(Pin = -10 dBm)		15		dB
	Gain at 1dB Compression Power Output at 1 dB			24		dB		tput Return Loss				
	Compressic			18		dBm		(Pin = -10 dBm)		9		dB
	Power Output Saturated:					OIP			28		dBm	
	Pin = -5.5 d	Bm	15.5	19		dBm		ise Figure		6		dB
	Drain Current Pin = -10 dl			105		mA		tector Voltage (Pout = +17 dBm)		0.1		v
		Drain Current at 1 dB Compression										

#### Note:

1. Typical range of gate voltage is -0.7 to -0.1 V to set Idq of 105 mA.

Characteristic performance data and specifications are subject to change without notice.

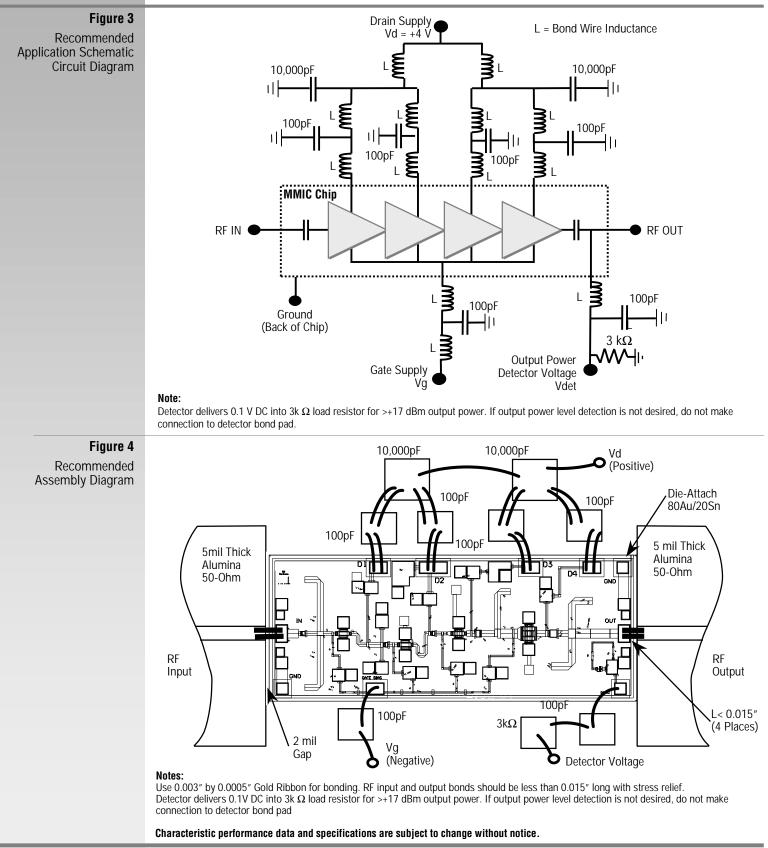


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Application Information	<ul> <li>CAUTION: THIS IS AN ESD SENSITIVE DEVICE.</li> <li>Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.</li> <li>Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.</li> <li>These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.</li> <li>Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.</li> </ul>
Figure 1 Functional Block Diagram	Drain Supply       Drain Supply       Drain Supply       Drain Supply         Vd1       Vd2       Vd3       Vd4         FIN       Output Four       RF OUT       MMIC Chip         Ground       Gate Supply       Output Power       Detector Voltage Vdet         Note:       Detector delivers 0.1 V DC into 3k Ω load resistor for >+17 dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.
<b>Figure 2</b> Chip Layout and Bond Pad Locations Chip Size is 3.0 mm x 1.2 mm. Back of chip is RF and DC ground	Dimensions in mm



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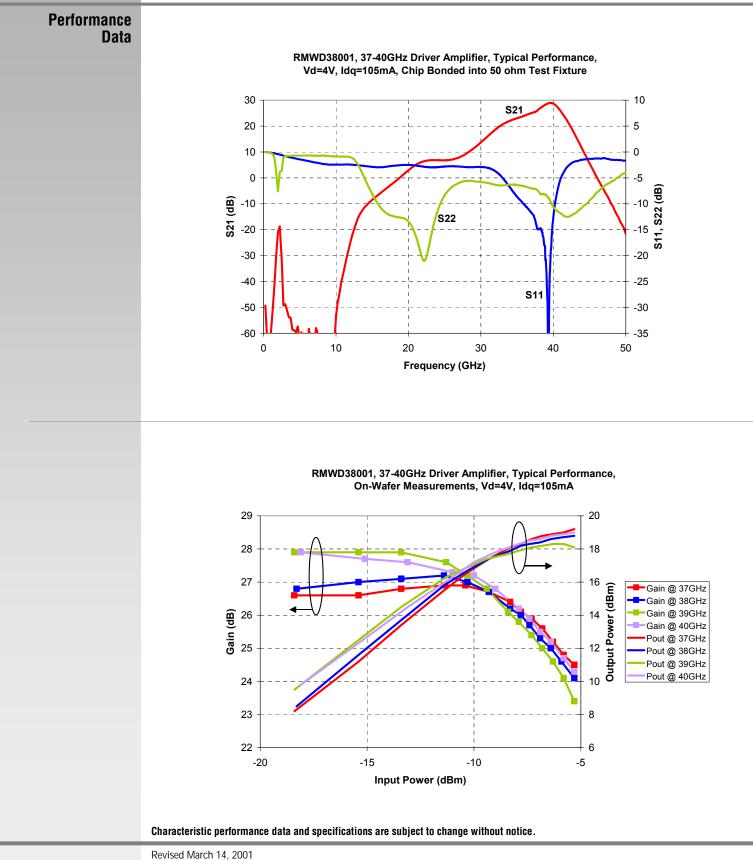


Recommended Procedure	CAUTIO	N: LOSS OF GATE VOLTAGES (Vg) WHILE DRAI AMPLIFIER CHIP.	N VOLTA	GES (Vd) IS PRESENT MAY DAMAGE THE
for Biasing and	The follo	owing sequence of steps must be followed to prop	erly test	the amplifier:
Operation	Step 1:	Turn off RF input power.	Step 4:	Adjust gate bias voltage to set the quiescent
	Step 2:	Connect the DC supply grounds to the grounds		current of Idq=105 mÅ.
		of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vgs.	Step 5:	After the bias condition is established, RF input signal may now be applied at the
	Step 3:	Slowly apply positive drain bias supply		appropriate frequency band.
		voltages of +4 V to Vd.	Step 6:	Follow turn-off sequence of:
				(i) Turn off RF Input Power
				(ii) Turn down and off drain voltage (Vd).
				(iii) Turn down and off gate voltage (Vg).

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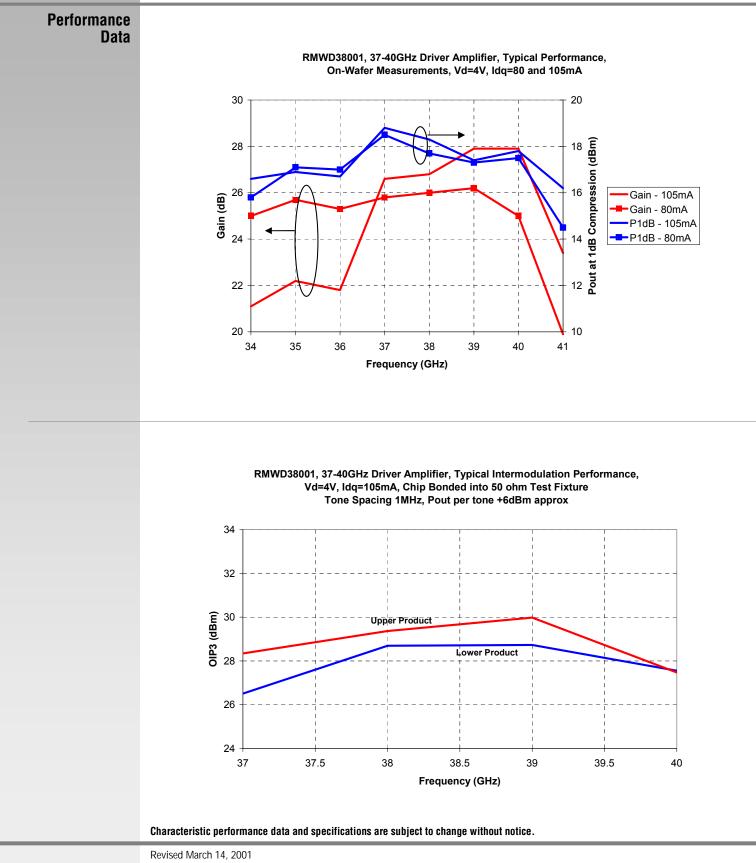


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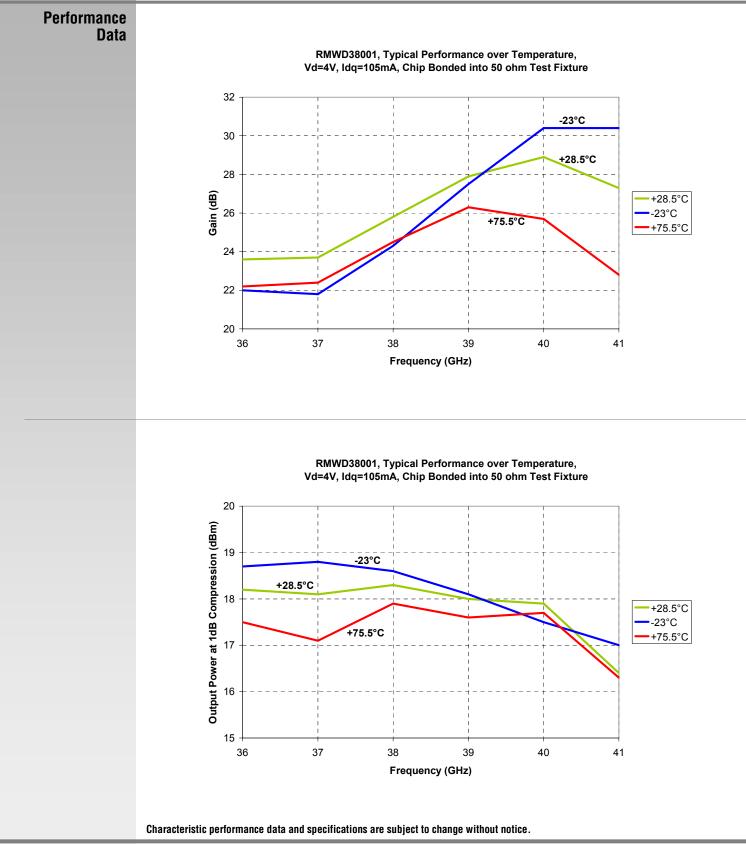




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