DDR VDDQ and Termination Voltage Regulator

General Description

The RT9005A/B is a dual-output linear regulator for DDR-SDRAM VDDQ supply and termination voltage VTT supply.

The Regulator is capable of actively sinking or sourcing up to 2A. The output termination voltage can be tightly regulated to track 1/2 VDDQ by two external voltage divider resistors.

Ordering Information

RT9005□□□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)
- VOUT1 Output Voltage
  A : 2.5V
  B : 1.8V

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

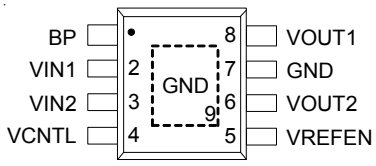
- **Ideal for DDR-I and DDR-II VDDQ, VTT Applications**
- **Integrated Power MOSFETs**
- **Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces**
- **High Accuracy Output Voltage at Full-Load**
- **VOUT2 Sink and Source 2A Continuous Current**
- **VOUT2 Adjustment by Two External Resistors**
- **Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output**
- **Current Limiting Protection**
- **On-Chip Thermal Protection**
- **Available in SOP-8 (Exposed Pad) Packages**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I and DDR-II Memory Systems

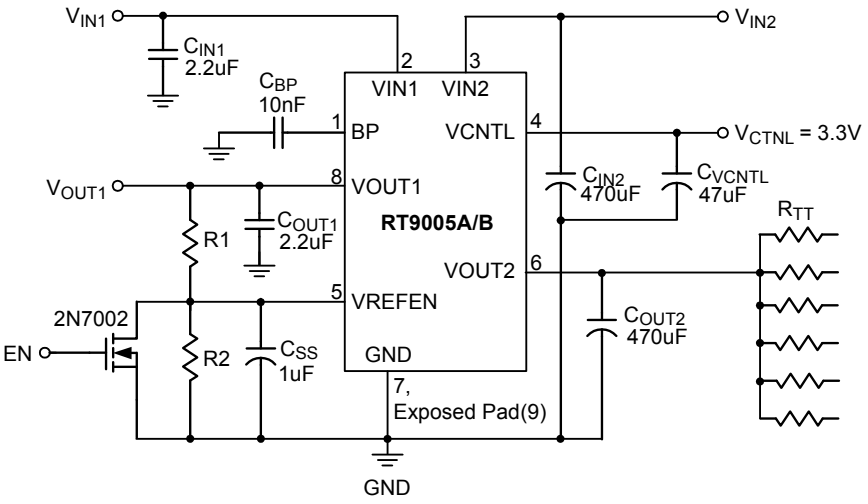
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

Typical Application Circuit

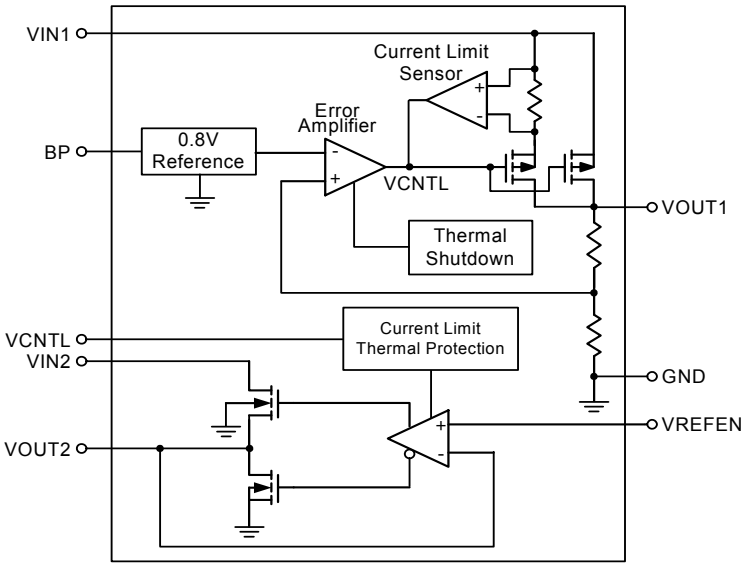


Note : If there is any application need to use 10μF ceramic capacitor in front of R_{TT}, please shut one 1000μF (Aluminum eletrolytic capacitor).

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BP	Noise Reduction. Connecting a 10nF capacitor to GND to reduce output noise.
7, Exposed Pad (9)	GND	Common Ground (The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation). The GND pad are a should be as large as possible and using many vias to conduct the heat into the buried GND plate of PCB layer.
2	VIN1	Linear Regulator Power Input Voltage.
3	VIN2	Input voltage which supplies current to the output pin. Connect this pin to a well-decoupled supply voltage. To prevent the input rail from dropping during large load transient, a large, low ESR capacitor is recommended to use. The capacitor should be placed as close as possible to the VIN2 pin.
4	VCNTL	VCNTL supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the VCNTL. Connect this pin to 3.3V bias supply to handle large output current with at least 10uF capacitor from this pin to GND.
5	VREFEN	Reference voltage input and active low VOUT2 shutdown control pin. Two resistors dividing down the VIN voltage on the pin to create the regulated output voltage. Pulling the pin to ground turns off the device by an open-drain, such as 2N7002, signal N-MOSFET.
6	VOUT2	Regulator Output. VOUT2 is regulated to REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 1000μF AL electrolytic capacitor with 10μF ceramic capacitors are recommended to reduce the effects of current transients on V_{OUT}.
8	VOUT1	Regulator 2.5V/1.8/1.5V Output.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed) ---------- 1.33W
- Package Thermal Resistance (Note 4)
  SOP-8 (Exposed), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed), θ_{JC} ---------- 28°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, V_{IN1} ---------- 5V to 2.5V
- Supply Input Voltage, V_{IN2} ---------- 3.6V to 1.5V
- Control Voltage, V_{CNTL} ---------- 5V to 3.1V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN1} =3.3V , V_{IN1} = V_{OUT} + 1V, C_{IN1} = C_{OUT1} = 2.2µF (Ceramic) & C_{BP} = 10nF; V_{IN2} = 2.5V/1.8/1.5V, V_{CNTL} = 3.3V, V_{REFEN} = 1.25V/0.9/0.75V, C_{IN2} = 470µF, C_{VCNTL}= 47µF, C_{OUT2} = 1000µF(Electrolytic), T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Operation Current	I_{VCNTL}	I_{OUT} = 0A	--	1.5	3.0	mA
Standby Current (Note 5)	I_{STBY2}	V_{REFEN} < 0.2V (Shutdown), R_{LOAD} = 180Ω	--	50	90	µA
VOUT1 (VDDQ)						
VOUT1 Accuracy	ΔV_{OUT}	I_{OUT} = 10mA	–2	--	+2	V
VOUT1 Current Limit	I_{LIM1}	R_{LOAD} = 0.5Ω, V_{IN1} = 3.3V	2	2.8	3	A
VOUT1 Dropout Voltage (Note 6)	V_{DROP}	I_{OUT} = 0.5A	--	120	180	mV
		I_{OUT} = 1.0A	--	240	360	
Line Regulation	ΔV_{LINE}	V_{IN1} = (V_{OUT1} + 0.5V) to 5.5V, I_{OUT1} = 1mA	--	--	0.3	%
Load Regulation (Note 7)	ΔV_{LOAD}	V_{IN1} = (V_{OUT1} + 0.5V), 10mA < I_{OUT1} < 1A	--	0.4	--	%/A
VOUT2 (VTT)						
Output Offset Voltage (Note 8)	V_{OS}	I_{OUT} = 0A	–20	--	+20	mV

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Load Regulation (Note 7)	ΔV_{LOAD}	I_{OUT} = +2A	−20	--	+20	mV
		I_{OUT} = −2A				
VOUT2 Current Limit	I_{LIM2}		2.2	--	--	A
Protection						
Thermal Shutdown Temperature	T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	35	--	°C
REFEN Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.6	--	--	V
	V_{IL}	Shutdown	--	--	0.2	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for SOP-8 (Exposed Pad) package.

Note 5. V_{OUT2} Standby current is the input current drawn by a regulator when the output voltage is disabled by a shutdown signal on REFEN pin (V_{IL} < 0.2V). It is measured with V_{IN2} = V_{CNTL} = 5V.

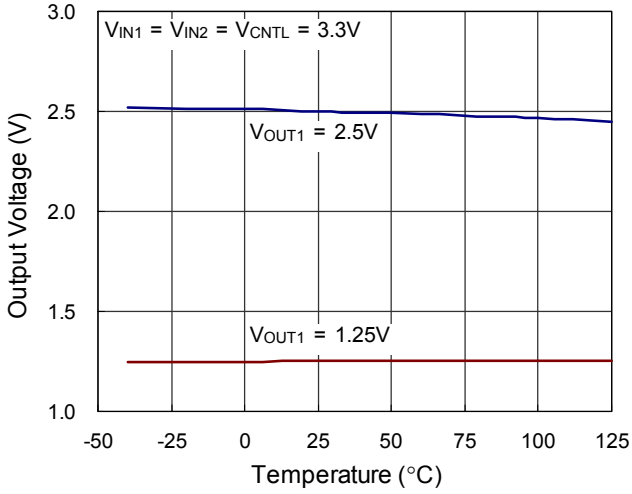
Note 6. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ − 100mV.

Note 7. Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

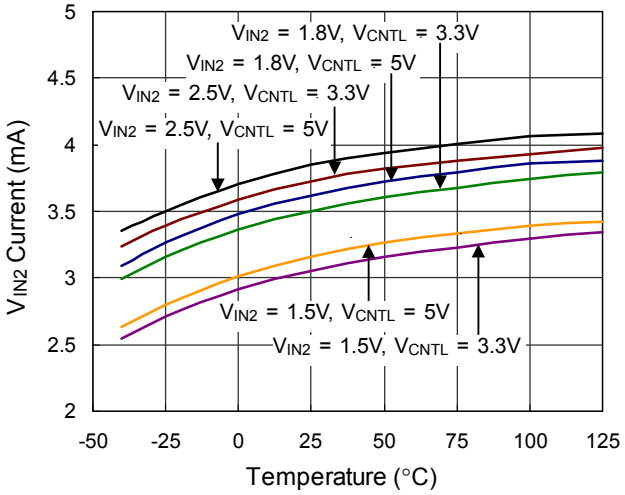
Note 8. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

Typical Operating Characteristics

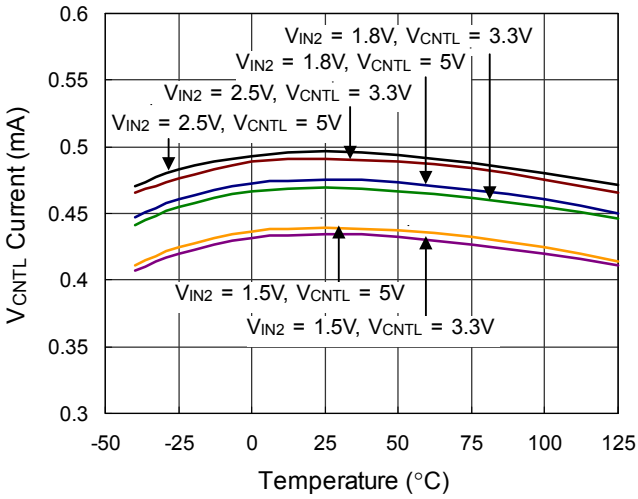
Output Voltage vs. Temperature



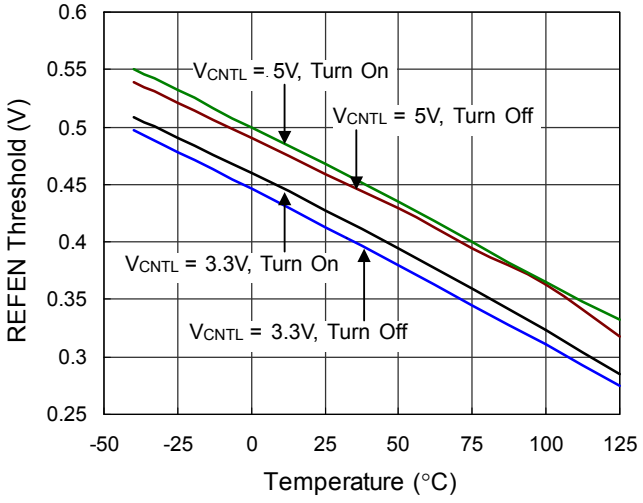
V_{IN2} Current vs. Temperature



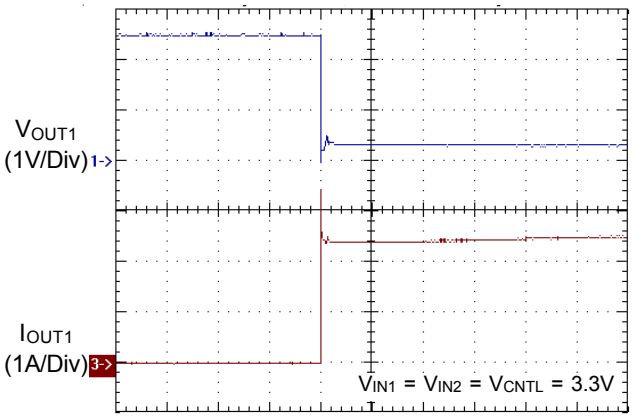
V_{CNTL} Current vs. Temperature



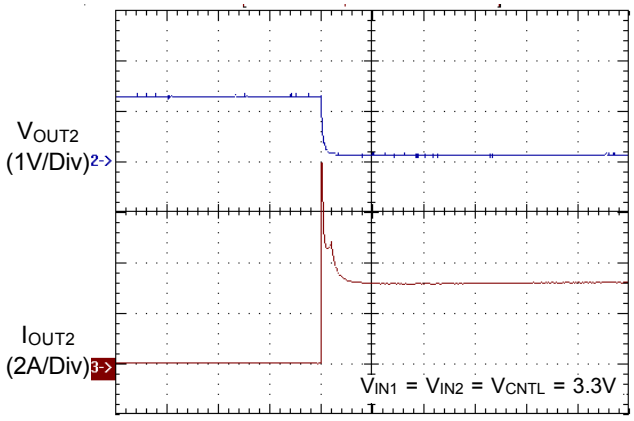
REFEN Threshold vs. Temperature



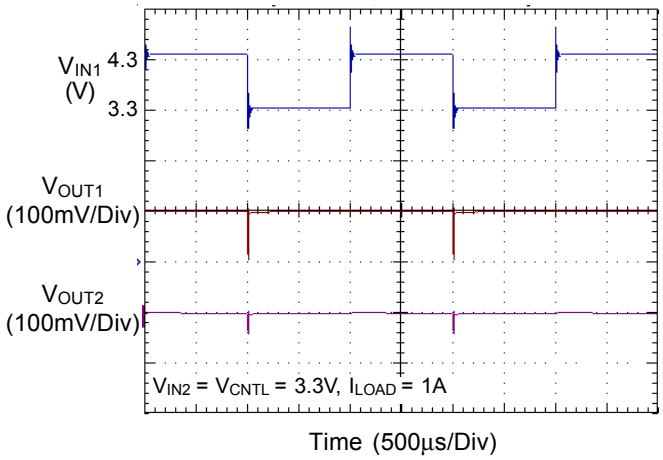
V_{OUT1} Short Circuit



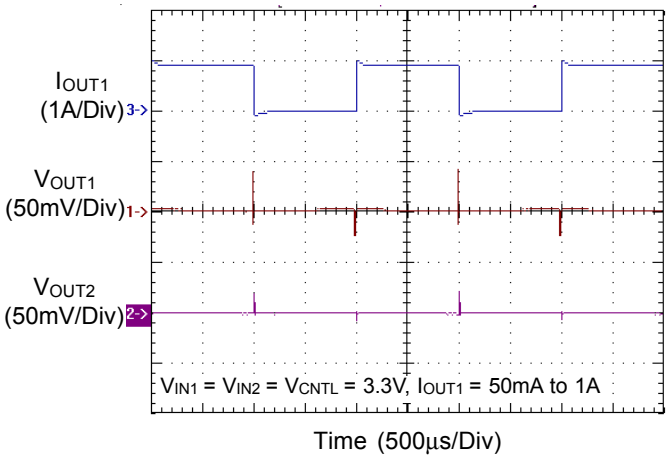
V_{OUT2} Short Circuit



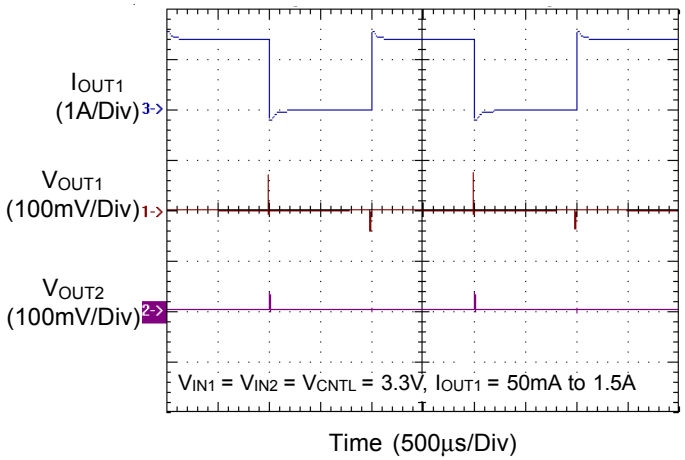
Line Transient Response



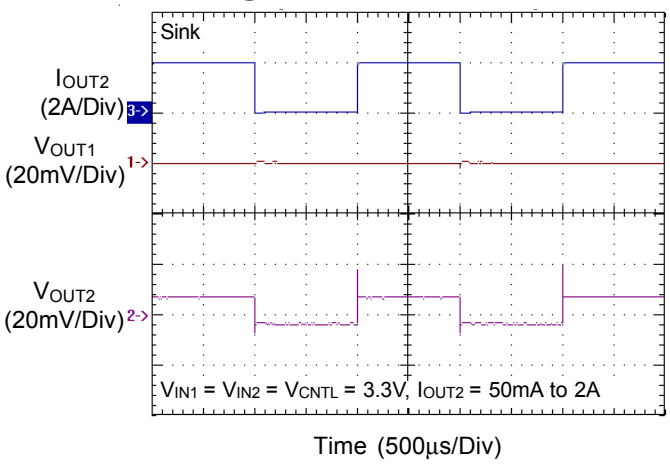
VOUT1 @ 1A Load Transient Response



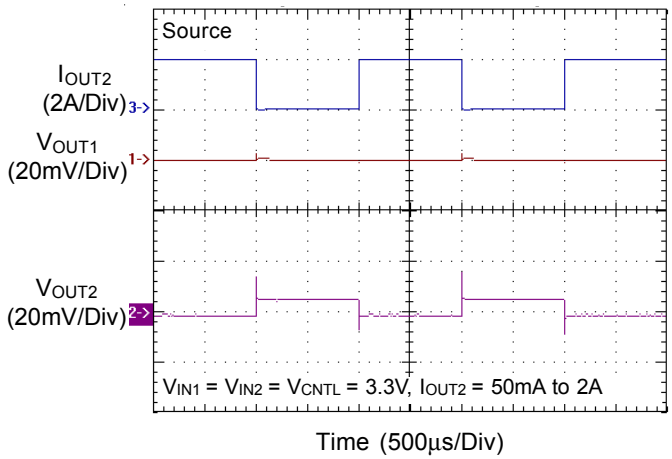
VOUT1 @ 1.5A Load Transient Response



VOUT2 @ 2A Load Transient Response



VOUT2 @ 2A Load Transient Response



Application Information

Thermal Consideration

RT9005A/B regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125°C. The power dissipation definition in device is :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOP-8 package (Exposed Pad) is 75°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)} = (125°C - 25°C) / 75°C/W = 1.33W$

Figure 2 show the package sectional drawing of SOP-8 (Exposed Pad). Every package has several thermal dissipation paths. As show in Figure 2, the thermal resistance equivalent circuit of SOP-8 (Exposed Pad). The path 2 is the main path due to these materials thermal conductivity. We define the exposed pad is the case point of the path 2.

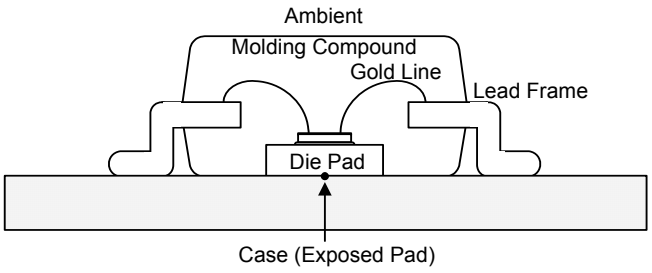


Figure 1. SOP-8 (Exposed Pad) Package Sectional Drawing

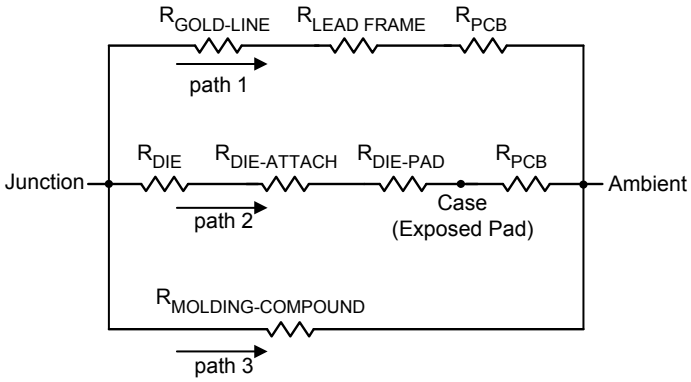


Figure 2. Thermal Resistance Equivalent Circuit

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of SOP-8 package.

About PCB layout, the Figure 3 show the relation between thermal resistance θ_{JA} and copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at T_A = 25°C.We have to consider the copper couldn't stretch infinitely and avoid the tin overflow. We use the "dog-bone" copper patterns on the top layer as Figure 4.

As shown in Figure 5, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad of 2 oz. copper (Figure 5.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 5.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 5.e) reduces the θ_{JA} to 49°C/W.

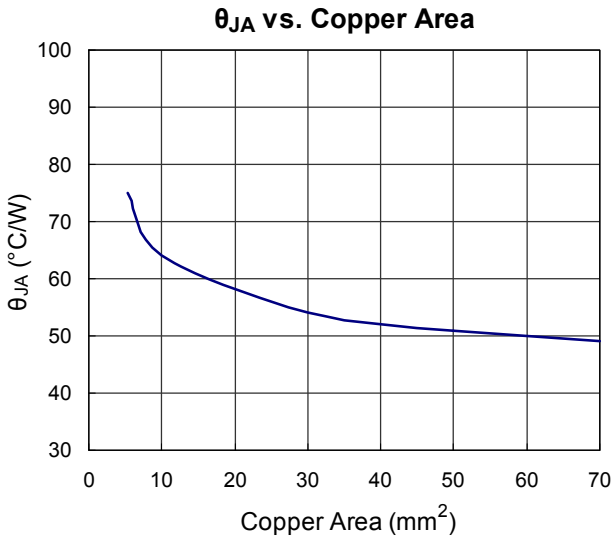


Figure 3

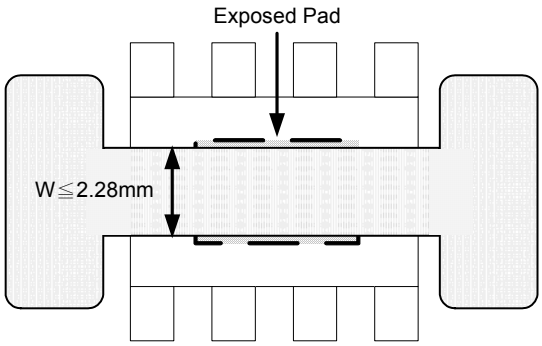


Figure 4. Dog-Bone layout

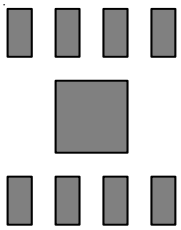


Figure 5 (a). Minimum Footprint, θ_{JA} = 75°C/W

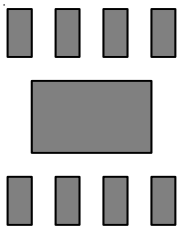


Figure 5 (b). Copper Area = 10mm², θ_{JA} = 64°C/W

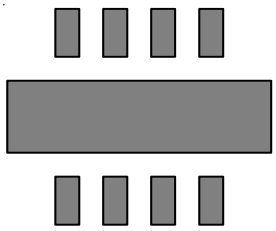


Figure 5 (c). Copper Area = 30mm², θ_{JA} = 54°C/W

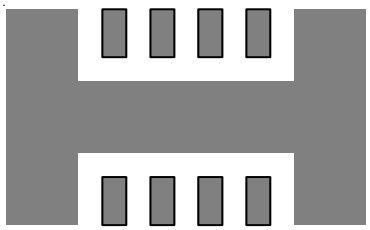


Figure 5 (d). Copper Area = 50mm², θ_{JA} = 51°C/W

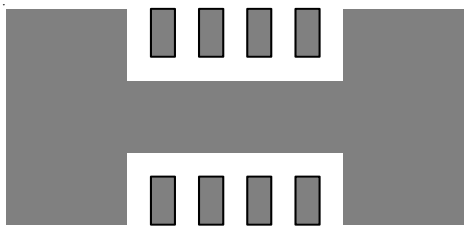
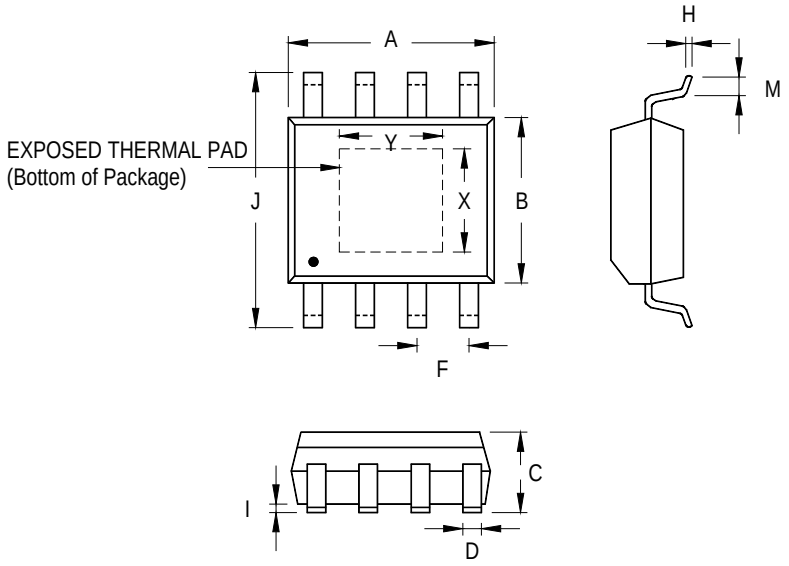


Figure 5 (e). Copper Area = 70mm², θ_{JA} = 49°C/W

Figure 5. Thermal Resistance vs. Different Cooper Area Layout Design

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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