RTD2011
Flat Panel Display Controller

Confidential

Revision 1.01

January 2, 2004

Content

Figure

Table

1 Features

General

- Integrated Spread-Spectrum DCLK PLL.
- Integrated 8-bit triple-channel 140MHz ADC/PLL
- Integrated programmable timing controller
- Embedded fully functional OSD support multi-language
- Embedded DDC support DDC1, DDC2B, DDC/CI
- Embedded 3 programmable PWM
- Zoom scaling up and down
- Embedded Pattern Generator
- No external memory required.
- Require only one crystal to generate all timing

Analog RGB Input Interface

- Support up to 140MHz (SXGA@ 75Hz)
- Support Sync On Green (SOG) and de-composite sync modes
- On-chip high-performance PLLs

Digital Input Interface

- Support 8-bit video (ITU 656) format input
- Built-in YUV to RGB color space converter & de-interlace

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase and Image position calibration

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement

Color Processor

- Digital brightness and contrast adjustments
- sRGB compliance
- Gamma correction
- Dithering logic for 18-bit panel color depth enhancement

Output Interface

- Built-in display timing generator and fully programmable
- 1 and 2-pixel/clock panel support and up to 140MHz
- Pin swap, odd/even swap and red/blue group swap.
- Programmable TCON function support
- RSDS (Reduced Swing Differential Signaling) data bus
- Reduced EMI and Power saving feature

Host Interface

- Support 3 pins MCU serial bus interface

Embedded OSD

- 12*18 dot font per character.
- Embedded 256 characters and symbols including 16 multi-color symbols.
- User's font ram, which make customer can program 128 special symbols.
- 32 programmable color font
- 7 background color and 8 character color.
- Programmable width and height control.
- 4 background window.
- Selectable shadow color for windows and characters.
- Intensity, blinking effect.
- Fade-in/out effect.
- Frame shadowing and independent row shadowing.
- Frame bordering and independent row bordering.
- 3 channels 8 bits PWM output, and selectable PWM clock frequency.
- Row-to-Row spacing to maintain constant display height.
- Window alpha-blending effect.

Power & Technology

- 2.5V/3.3V power supplier
- 0.25um CMOS process; 128-pinPQFP package

2 RTD2011 Pin-Out Diagram

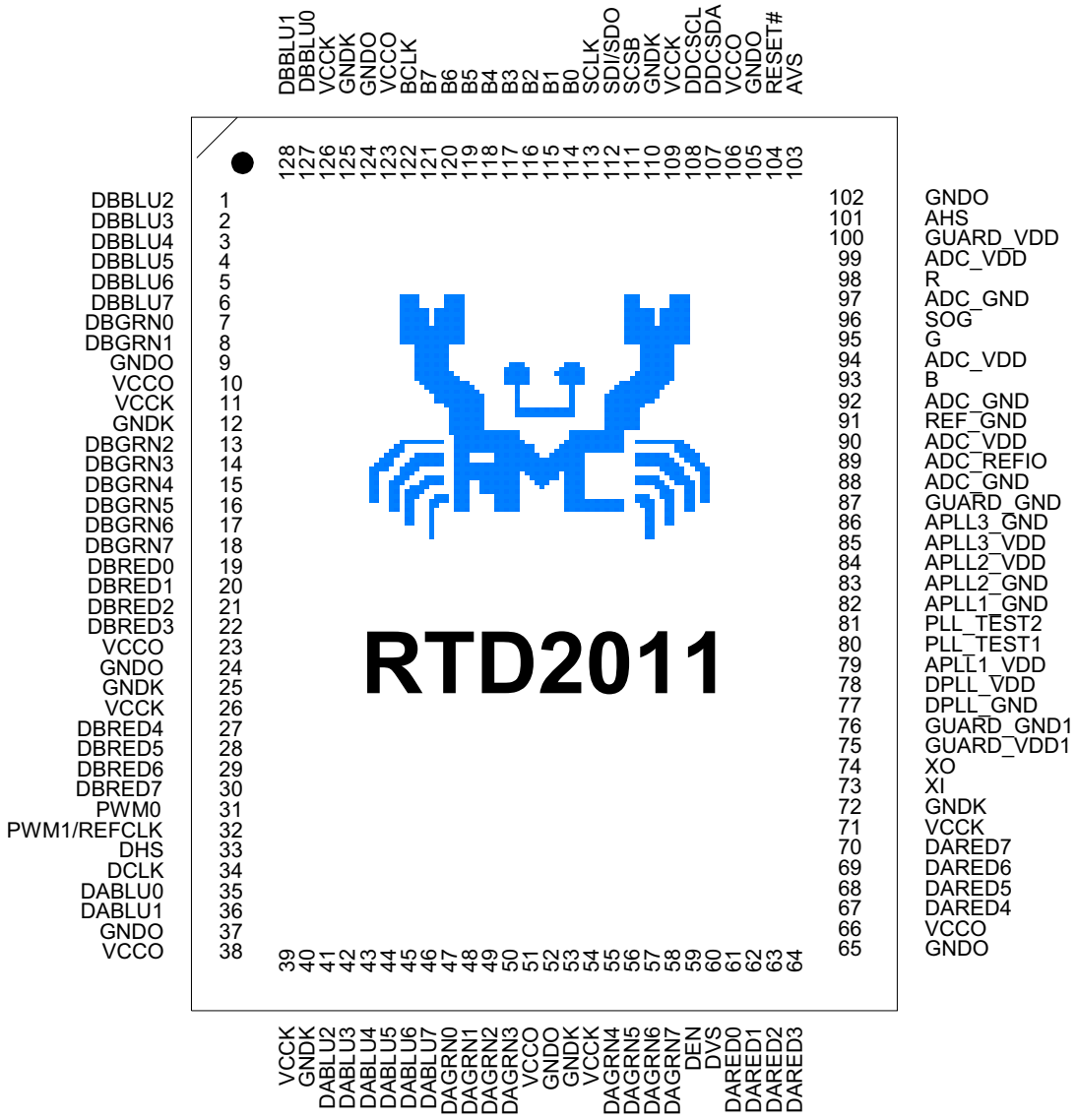


Figure 1 RTD2011 Pin-Out Diagram

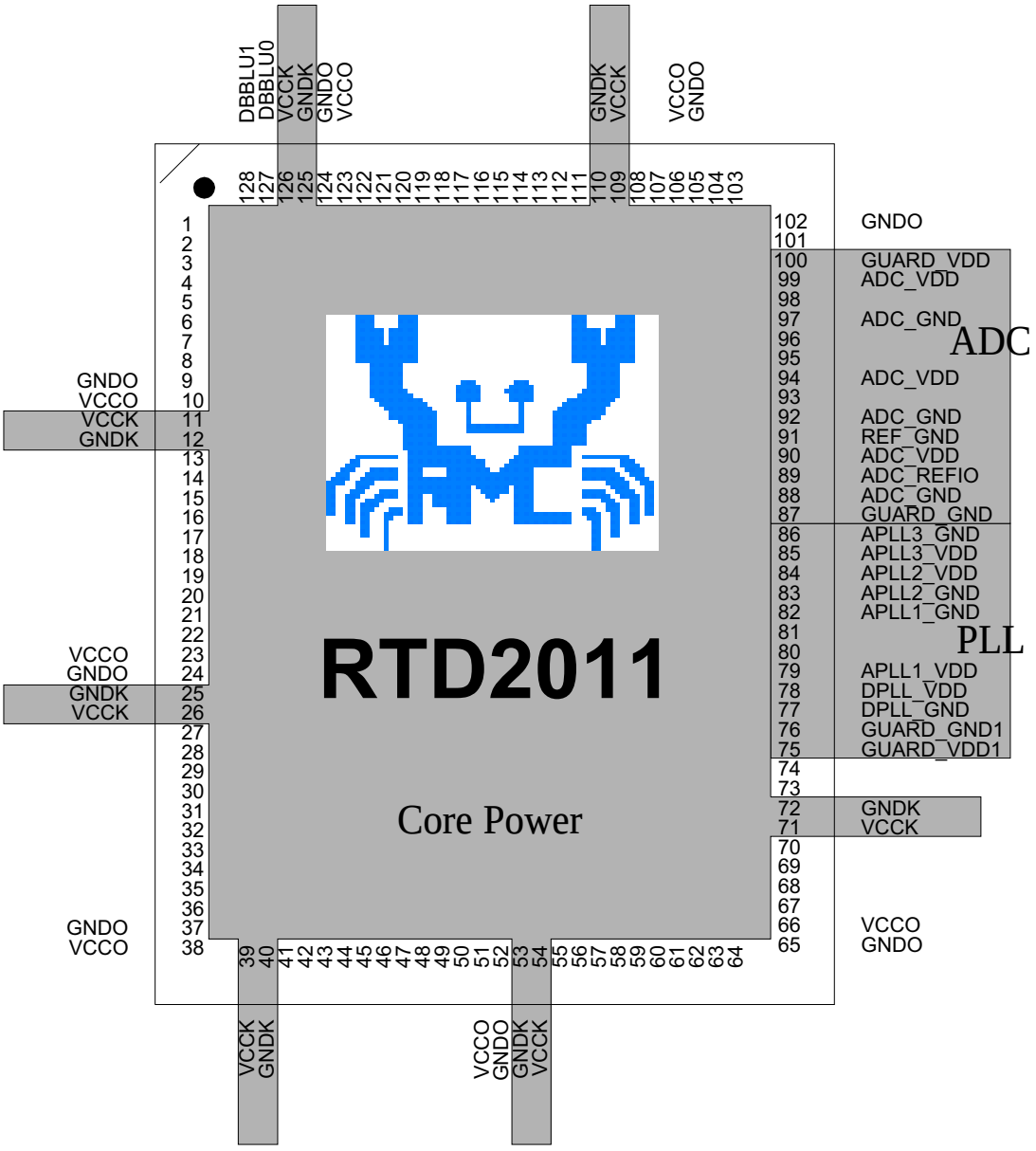


Figure 2 Board Power Plane Design

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

ADC: 14 pins

Name	I/O	Pin No	Description	Note
ADC_GUARD_GND	AG	87	ADC guard-ring ground	
ADC_GND	AG	88	ADC ground	
ADC_REFIO	AI	89	ADC reference pad	
ADC_VDD	AP	90	ADC power	(3.3V)
REF_GND	AG	91	Analog RGB ground	
ADC_GND	AG	92	ADC ground	
B	AI	93	Analog input from BLUE channel	
ADC_VDD	AP	94	ADC power	(3.3V)
G	AI	95	Analog input from GREEN channel	
SOG/ADC_TEST	AIO	96	SOG in / ADC test pin	
ADC_GND	AG	97	ADC ground	
R	AI	98	Analog input from RED channel	
ADC_VDD	AP	99	ADC power	(3.3V)
ADC_GUARD_VDD	AP	100	ADC guard-ring power	(3.3V)

PLL: 14 pins

Name	I/O	Pin No	Description	Note
PLL_GUARD_VDD	AP	75	PLL guard-ring power	(3.3V)
PLL_GUARD_GND	AG	76	PLL guard-ring ground	
DPLL_GND	AG	77	Ground for digital PLL	
XI	AI	73	Reference clock input	
XO	AO	74	Reference clock output	
DPLL_VDD	AP	78	Power for digital PLL	(3.3V)
APLL1_VDD	AP	79	Power for multi-phase PLL	(3.3V)
PLL_TEST1	AIO	80	Test Pin 1 / IRQ#	
PLL_TEST2	AIO	81	Test Pin 2 / pi(RSDS)	
APLL1_GND	AG	82	Ground for multi-phase PLL	
APLL2_GND	AG	83	Ground for analog PLL	
APLL2_VDD	AP	84	Power for analog PLL	(3.3V)
APLL3_VDD	AP	85	Power for hvmti PLL, hvana PLL	(3.3V)
APLL3_GND	AG	86	Ground for hvmti PLL, hvana PLL	

Control Interface: 4 pins

Name	I/O	Pin No	Description	Note
SCSB	I	111	Serial control I/F chip select	(2), (3), (5) (2), (3), (6)
SCLK	I	113	Serial control I/F clock	(2), (3), (5) (2), (3), (6)
SDI/SDO	I/O	112	Serial control I/F data in	(1), (2), (3) /, 2mA
RESET#	I	104	RESET# for Controller;	(2), (3), (5)

Digital Input: 11 pins

Name	I/O	Pin No	Description	Note
AHS	I	101	VGA-port Horizontal Sync;	(2), (4), (5)
AVS	I	103	VGA-port Vertical Sync;	(2), (4), (5)
BCLK/	I O	122	1. VGB-port input clock 2. ADC_TEST_CLK 3. TCON_2	(1), (2), (8)
B7~B0	I O	121 ~ 114	1. Video8[7:0] 2. ADC test data output, ADC_OUT [7:0] 3. TCON_10 ~3(a)	(1), (2), (3) (8)

Display Port: 52 pins

Name	I/O	Pin No	Description	Note
DCLK	O	34	Display clock; / TCON_ECLK/ TCON_0	(8)
DHS	O	33	Display Horizontal Sync; / TCON_OCLK/ TCON_1	(8)
DVS	O	60	Display Vertical Sync; /TCON_0/ RSDS clkp	(8)
DEN	O	59	Display Data Enable; / TCON_1/ RSDS clkn	(8)
DARED [7:0]	O	70, 69, 68, 67, 64, 63, 62, 61	Display A-port RED data; / RSDS R3p,R3n, R2p,R2n, R1p,R1n, R0p,R0n /TCON8 - bit0; TCON9 – bit1	(8)
DAGRN [7:0]	O	58, 57, 56, 55, 50, 49, 48, 47	Display A-port GREEN data; / RSDS G3p,G3n, G2p,G2n, G1p,G1n, G0p,G0n /TCON10 – bit0	(8)
DABLU [7:0]	O	46, 45, 44 ,43, 42, 41, 36, 35	Display A-port BLUE data; / RSDS B3p,B3n, B2p,B2n, B1p,B1n, B0p,B0n	(8)
DBRED [7:0]	O	30, 29, 28, 27, 22, 21, 20, 19	Display B-port RED data; / TCON2 -bit0; TCON3 -bit1 /TCON8~10 – bit2~4 /pi bit5	(8)
DBGRN [7:0]	O	18, 17, 16, 15, 14, 13, 8, 7	Display B-port GREEN data; / TCON4- bit0; TCON5- bit1(b),(c)	(8)
DBBLU [7:0]	O	6, 5, 4, 3, 2, 1, 128, 127	Display B-port BLUE data; / TCON6- bit0; TCON7- bit1(a)	(8)

Miscellaneous Interface: 2 pins

Name	I/O	Pin No	Description	Note
PWM1/REFCLK	IO	32	PWM1 / In/out testpin for DCLK / ITU656 (video8) even-odd signal	(2), (8)
PWM_0	O	31	PWM_0 output;	2mA, skew

DDC Channel: 2 pins

Name	I/O	Pin No	Description	Note
DDCSDA	I O	107	DDC serial control I/F data input DDC serial control I/F data output	(2), (3), (5), (6) 8mA, skew
DDCSCL	I	108	DDC serial control I/F clock	(2), (3), (5)

Power & Ground: 29 pins

Name	I/O	Pin No	Description
3.3V Power	P	10, 23, 38, 51, 66, 106, 123	VCC3IO: 7
3.3V Ground	G	9, 24, 37, 52, 65, 105, 124, 102	GNDO: 8
2.5V Power	P	11, 26, 39, 54, 71, 109, 126	VCCK: 7
2.5V Ground	G	12, 25, 40, 53, 72, 110, 125	GNDIK: 7

Note: (1) TTL compatible CMOS Input (Vt=1.7V); VCC=3.3V;
(2) 5V tolerance pad;
(3) Internal 75K Ohms pull high resistor.
(4) Internal 75K Ohms pull low resistor.
(5) Schmitt trigger CMOS Input (Vt=1.4-~2.2V);
(6) Open-Drain, Output Drive low & Pull-high.
(7) Bi-directional input/output
(8) Programmable driving current (2~16mA)

3 General Description

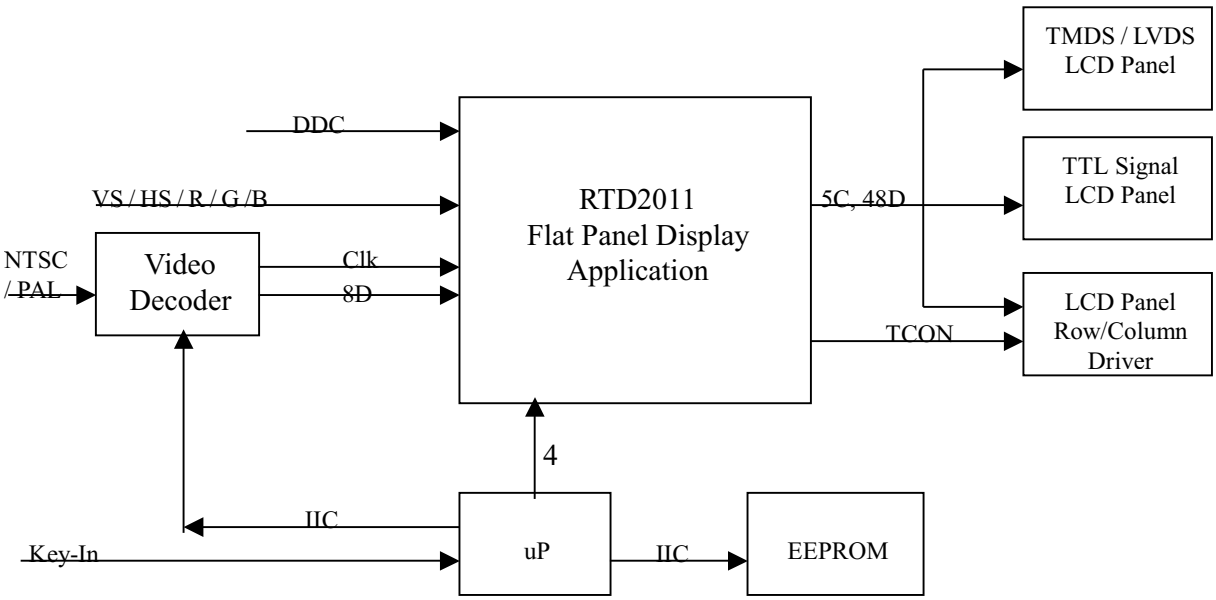


Figure 3 Application System Block Diagram

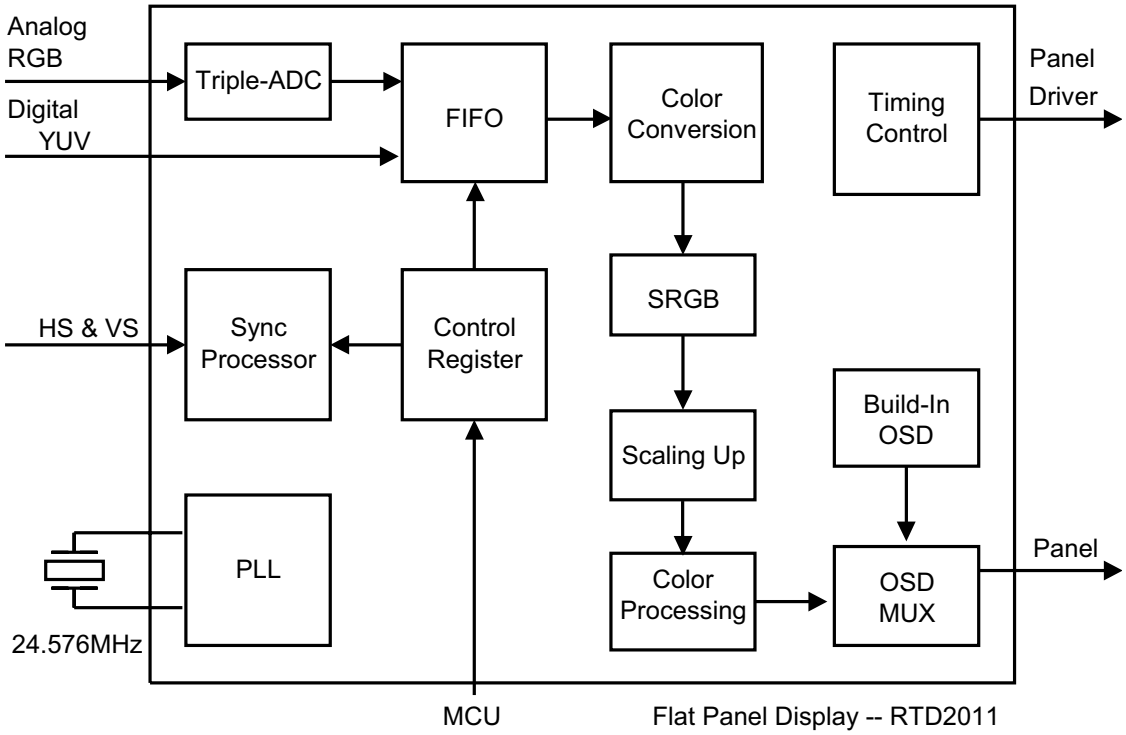


Figure 4 Chip Functional Block Diagram

4 Functional Description

4.1 Input

Digital Input (ITU 656)

RTD2011 is designed to connect the interface of digital signal from video decoder. Input data is latched within a capture window defined in registers. The timing scheme designed for input devices are showed in the following diagram.

There are not H sync、V sync signals provided by the video decoder with ITU BT.656, these synchronal signals have to be generated by decoding the EAV & SAV timing reference signals.

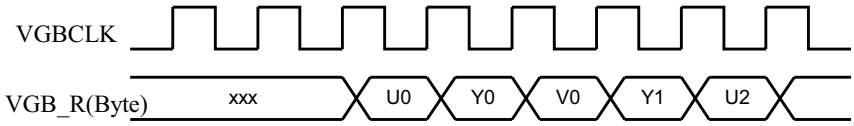


Figure 5 Input YUV 4:2:2(8-bits) Timing

Only 254 of possible 256 8-bit words may be used to express a signal value, 0 and 255 are reserved for data identification purposes. Video 8 data stream is as below:

Blanking period			Timing reference code				720 pixels YUV 422 DATA									Timing reference code				Blanking period		
…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	Cb2	Y2	…	Cr718	Y719	FF	00	00	EAV	80	10	…

Cbn: U(B-Y) colour difference component
Yn : luminance component
Crn: V(R-Y) colour difference component

SAV/EAV format

Bit 7	Bit 6(F)	Bit 5(V)	Bit 4(H)	Bit 3(P3)	Bit 2(P2)	Bit 1(P1)	Bit 0(P0)
1	Field bit 1st field F=0 2nd field F=1	Vertical blanking bit V=1 Active video V=0	H=0 in SAV H=1 in EAV	Protection bits			

Hardware can recognize the occurrence of EAV & SAV by detecting the 0xff , 0x00 , 0x00 data sequence, and then generate the Hsync、Vsync、Field signals internally by decoding the fourth word of the timing reference signal(EAV、SAV). F & V change state synchronously with the EAV(End of active video) reference code at the beginning of the digital line.

Bits P0, P1, P2, P3, have states dependent on the states of the bits F, V and H as shown below. At the receiver this permits one-bit errors to be corrected and two-bits errors to be detected.

Protection bits

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

Analog Input

RTD2011 integrates three ADC's (analog-to-digital converters), one for each color (red, green, and blue). The sync-processor can deal with Separate-Sync, Composite-Sync, and Sync-On-Green. And the PLL can generate very low jitter clock from HS to sample the analog signal to digital data. Input data is latched within a capture window defined in registers refer to VS and HS leading edge.

Input Capture Window

Inside RTD2011, there are four registers IPH_ACT_STA, IPH_ACT_WID, IPV_ACT_STA & IPV_ACT_LEN to define input capture window for the selected input video on either A or B input port while programmed analog input mode. The horizontal sync (IHS) & vertical sync (IVS) signals are used from the selected port to determine the capture window region.

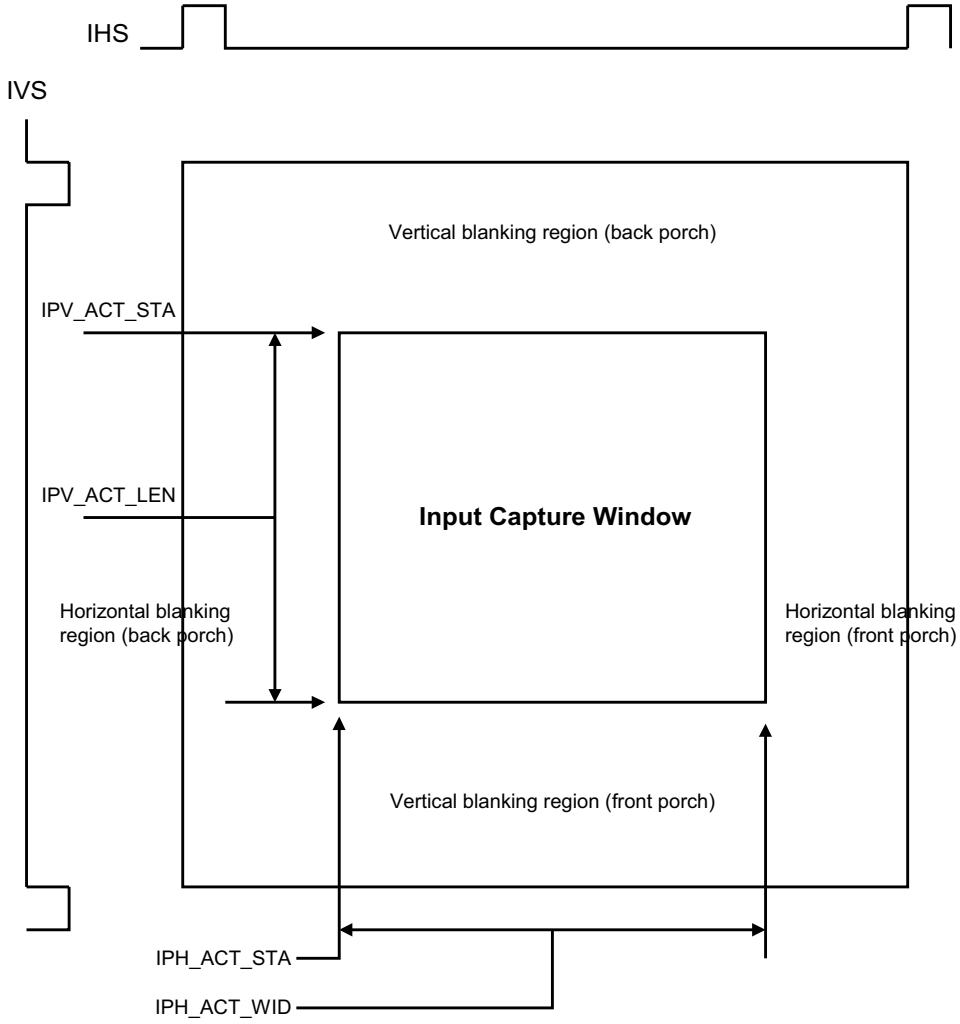


Figure 6 Input Capture Window

4.2 Output

Display Output Timing

The display output port sends single/double pixel data transfer and synchronized display timing to an external device. The display port also support display panel with 6-bit per color, turn on the dithering function to enhance color depth.

In single pixel output mode, single pixel data (24-bit RGB) is transferred to display port A on each active edge of DCLK, the rate of DCLK is also equal to display pixel clock. The sync & enable signals are also sent to display port on each active edge of DCLK.
Seeing figure13 as below

In double pixel output mode, double pixel data (48-bit RGB) is transferred to display port A & B on each active edge of DCLK and the rate of DCLK is equal to half display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of DCLK. Seeing figure14 as below.

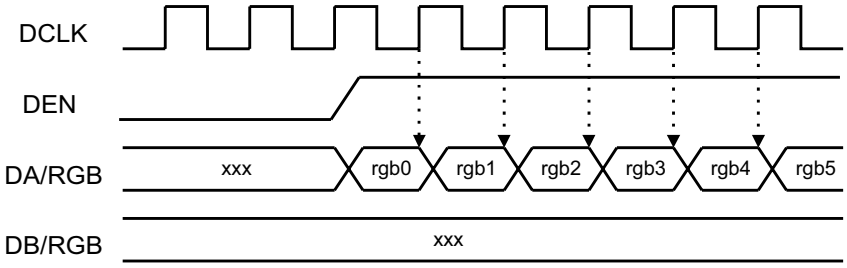


Figure 7 Single Pixel Mode Display Data Timing

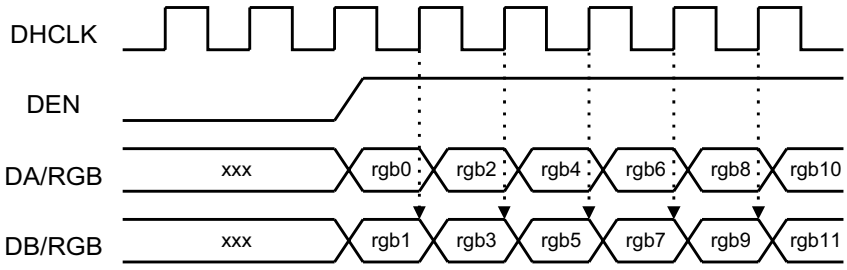


Figure 8 Double Pixel Mode Display Data Timing

Display Active Window

These registers to define the display active window are showed us below in application with frame buffer. In the case of without frame buffer that means frame sync mode, the definitions of these registers are quiet different from the description below. There are two frame sync modes applied to RTD2011 chip for various applications. Refer to the register description for detailed.

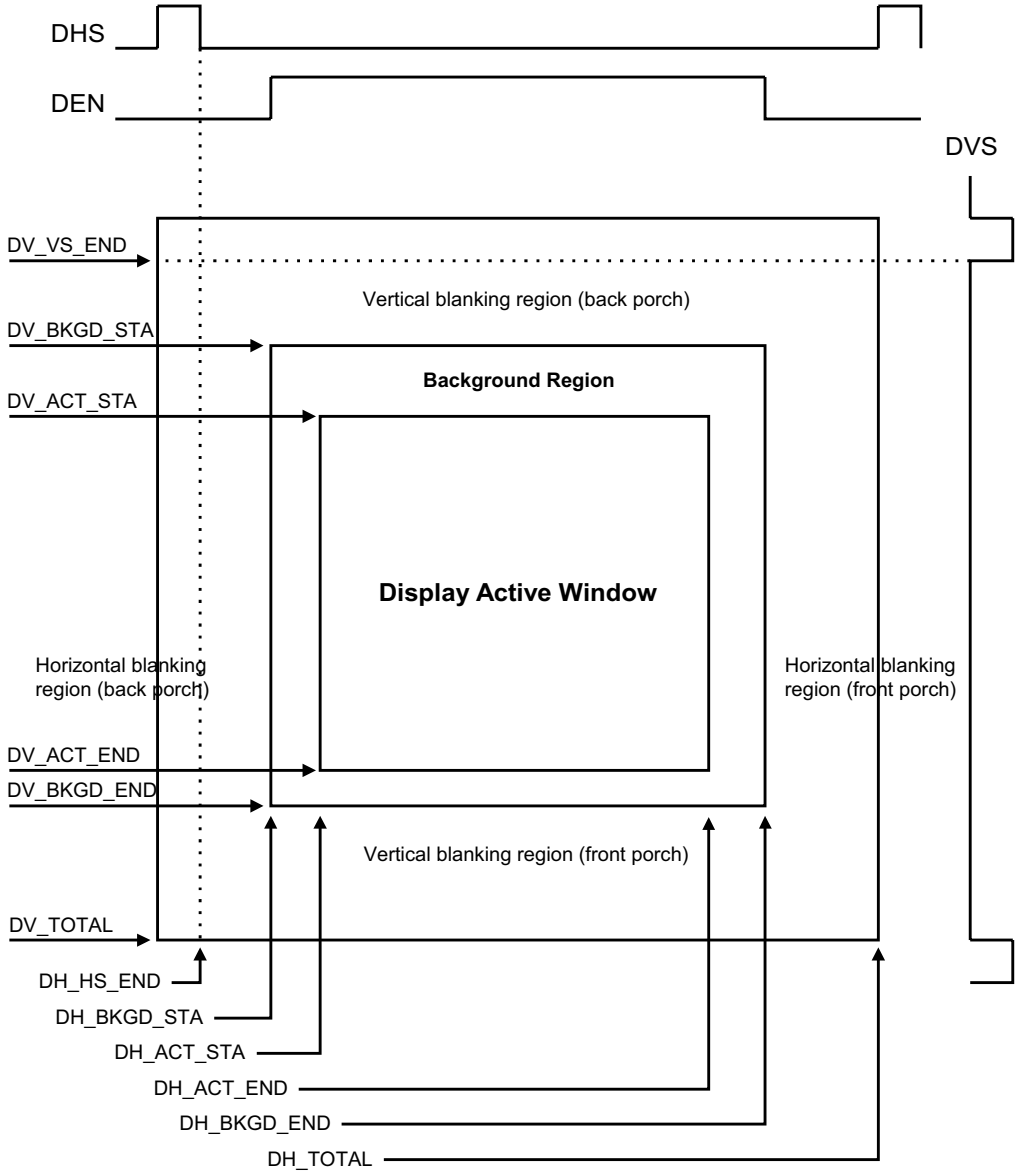


Figure 9 Display Active Window Diagram

4.3 Color Processing

Digital color R & G & B independent channel contrast & brightness controls are built in RTD2011. The contrast control is performed a multiply value from 0/128, 1/128, 2/128… to 255/128 for each R/G/B channel. The brightness control is used to set an offset value from –128 to +127 also for each R/G/B channel.

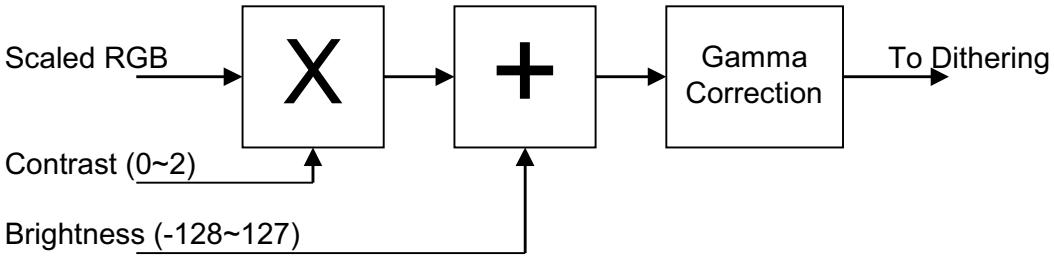


Figure 10 Brightness, Contrast & Gamma Correction block diagram

4.4 OSD & Color LUT

Build-In OSD

The detailed function-description of build-in OSD, please refer to the application note for RTD2011 embedded OSD.

Color LUT & Overlay Port

The following diagram presents the data flow among the gamma correction, dithering, overlay MUX, OSD LUT and output format conversion blocks.

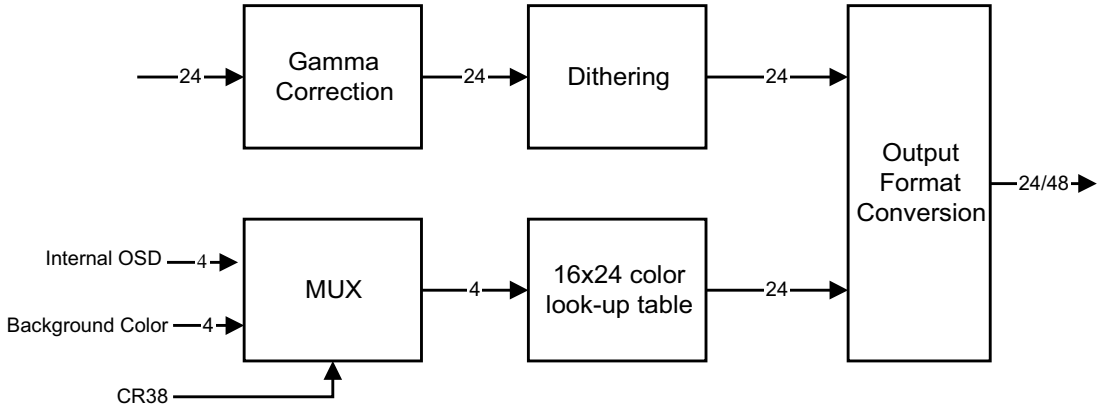


Figure 11 OSD color look-up table data path diagram

4.5 Auto-Adjustment

There are two main independent auto-adjustment functions supported by RTD2011, including auto-position & auto-tracking. The operation procedure is as following;

Auto-Position

1. Define the RGB color noise margin (7B,7C,7D): When the value of color channel R or G or B is greater than these noise margins, a valid pixel is found.
2. Define the threshold-pixel for vertical boundary search (7C[1:0]).
3. Define the boundary window of searching (75 ~ 7A) for horizontal boundary search.
4. Start auto-function (7F[0]) .
5. The result can be read from register (80 ~ 87).

Auto-Tracking

1. Setting the control-registers (7F) for the function (auto-phase, auto-balance) according to the Control-Table.
2. Define the Diff-Threshold (7E).
3. Define the boundary window of searching (75 ~ 7A) for tracking window.
4. Start auto-function (7F[0]) .
5. The result can be read from register (88 ~ 8B).

4.6 PLL System

Inside the RTD2011, there are three PLL systems for display clock and ADC sample clock.

DCLK PLL

PLL provides a wide range of user-programmable frequency synthesis options, and the formula as following; The frequency before VCO_Divide must be 50MHz~450MHz.

DCLK = Fin * DPM / DPN / VCO_Divide,

Meanwhile, Fin = 24.576MHz, the DPLL_M[7:0] & DPLL_N[5:0] are the 8-bit M & 6-bit N value of DCLK. DPM=DPLL_M[7:0]+2, DPN=DPLL_N[5:0]+2.

Of course, you can force this clock from external oscillators through pins REFCLK for your own applications.

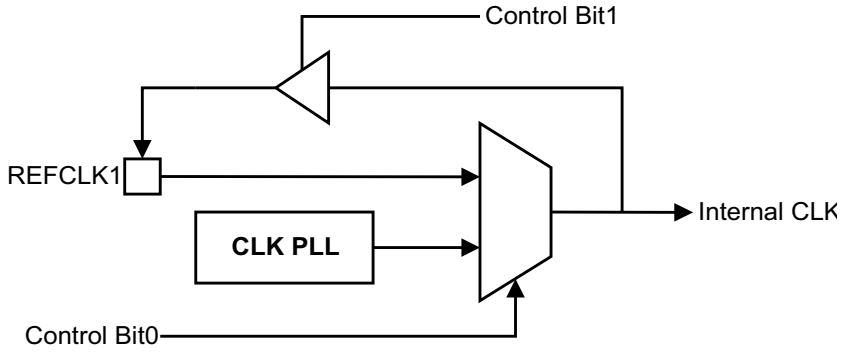
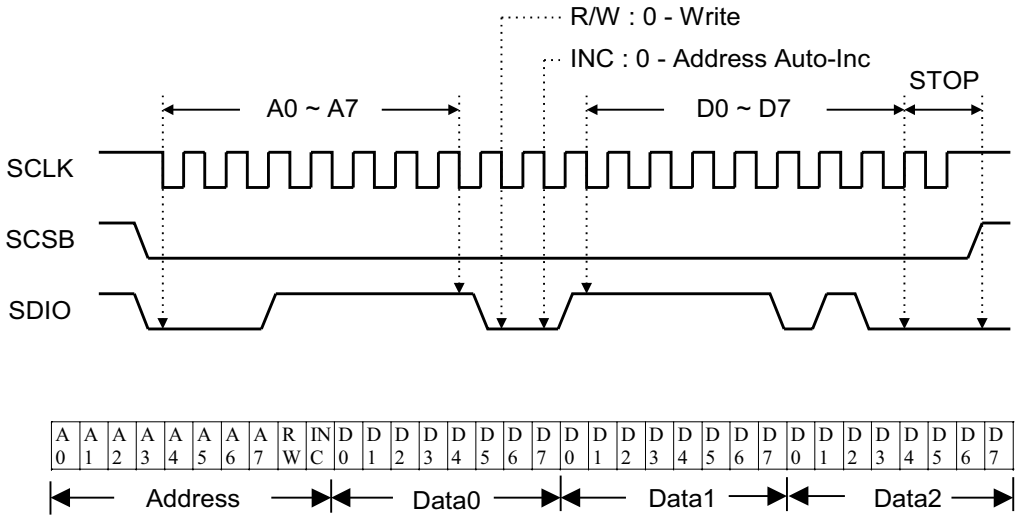


Figure 12 PLL System Control Diagram

Spread-Spectrum function is also build in DCLK to reduce EMI while using TCON. You can control the SSP_I, SSP_W, and FMDIV to fine-tune the EMI.

4.7 Host Interface

Any transaction should start from asserted the SCS# and stop after de-asserted the SCS#. Within this period, any data are driving by clock rising edge and latched by clock falling edge. The detailed timing diagrams are as following;



Address: A0~A7
R/W: Read/Write Mode for Data Phase, 0 -- Write, 1 -- Read
INC: Address Auto-Increasing Mode, 0 -- enable auto-increasing, 1 -- disable

Figure 13 Serial Port Write Timing & Data Format

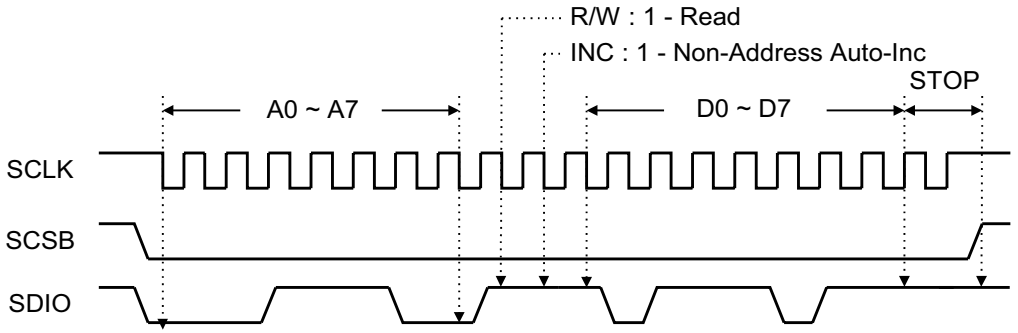


Figure 14 Serial Port Read Timing