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RTL8153-CG

INTEGRATED 10/100/1000M ETHERNET CONTROLLER FOR USB APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2012/09/14	First release.
1.1	2013/03/20	Added section 6.15 Always On Always Connected, page 16. Corrected minor typing errors.

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1. General Description

The Realtek RTL8153-CG 10/100/1000M Ethernet controller combines an IEEE 802.3u compliant Media Access Controller (MAC), USB 3.0 bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8153 offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capabilities. The RTL8153 features embedded One-Time-Programmable (OTP) memory that can replace the external EEPROM (93C46/93C56/93C66/TWSI).

The RTL8153 features USB 3.0 to provide higher bandwidth and improved protocols for data exchange between the host and the device. USB 3.0 also offers more advanced power management features for energy saving.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments.

The RTL8153 supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

The RTL8153 supports 'RealWoW!' technology to enable remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The 'RealWoW!' service requires registration on first time use.

The RTL8153 supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The RTL8153 can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8153 supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8153 supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The RTL8153 is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8153 is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, docking station, and embedded applications.

2. Features

Hardware

- Integrated 10/100/1000M transceiver
- Auto-Negotiation with Next Page capability
- Supports USB 3.0, 2.0, and 1.1
- Supports CDC-ECM
- Supports LPM (Link Power Management)
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Supports Wake-On-LAN and 'RealWoW!' (Wake-On-WAN) Technology (see note 1)
- Supports ECMA-393 ECMA ProxZzzy Standard for sleeping hosts (see note 1)
- XTAL-Less Wake-On-LAN
- Supports power down/link down power saving
- Transmit/Receive on-chip buffer support
- EEPROM Interface
- Embedded OTP memory can replace external EEPROM
- Built-in switching regulator and LDO regulator
- Supports Customizable LEDs
- Supports hardware CRC (Cyclic Redundancy Check) function
- LAN disable with GPIO pin
- Supports 25MHz or 48MHz external clock (from oscillator or system clock source)
- SPI Flash Interface
- 48-pin QFN 'Green' package

Note 1. Select between RealWoW! or ECMA, only one feature can be active at a time.

Software Offload

- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports jumbo frame to 9K bytes

IEEE

- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3 and IEEE 802.3u
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az-2010 (EEE)

Microsoft AOAC (Always On Always Connected)

- Supports 16-set 128-byte Wake-Up Frame pattern exact matching
- Supports link change wake up
- Supports Microsoft WPD (Wake Packet Detection)
- Supports Protocol Offload (ARP & NS)

Intel CPPM (Converged Platform Power Management)

- Supports L1 with 3ms BESL (USB 2.0)
- Dynamic LTM messaging (USB 3.0)
- Supports U1/U2 (USB 3.0)
- Supports selective suspend

3. System Applications

- USB 10/100/1000M Ethernet on Motherboard, Dongle, Notebook, Docking station, or Embedded system

4. Pin Assignments

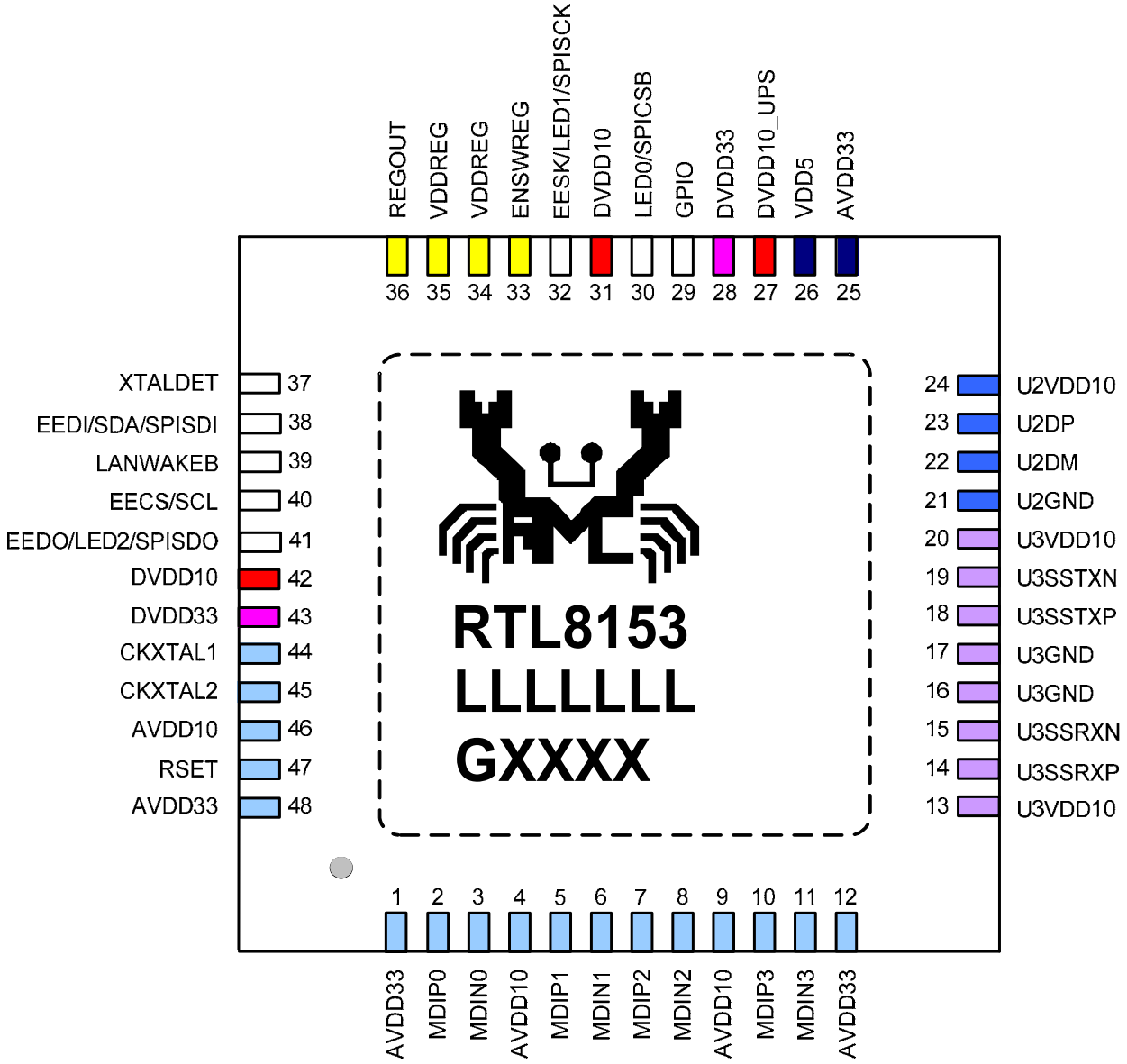


Figure 1. Pin Assignments

4.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 1).

5. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input O: Output

P: Power

5.1. Power Management Pin

Table 1. Power Management Pin

Symbol	Type	Pin No	Description
LANWAKEB	O	39	Power Management Event Output Pin (Active Low).

5.2. SPI (Serial Peripheral Interface) Flash Pins

Table 2. SPI Flash Pins

Symbol	Type	Pin No	Description
SPICSB	O	30	SPI Flash Chip Select.
SPISDO	I	41	Input from SPI Flash Serial Data Output Pin.
SPISDI	O	38	Output to SPI Flash Serial Data Input Pin.
SPISCK	O	32	SPI Flash Serial Data Clock.

5.3. EEPROM Pins

Table 3. EEPROM Pins

Symbol	Type	Pin No	Description
EESK	O	32	Serial Data Clock for 93C46/93C56/93C66.
EEDI/SDA	IO	38	EEDI: Output to serial data input pin of EEPROM (93C46/93C56/93C66) SDA: Data interface for TWSI EEPROM Refer to the reference schematic for strapping pin information. All strapping pins are power-on latch pins. Power-on latch high voltage: TWSI EEPROM Power-on latch low voltage: SPI EEPROM
EEDO	I	41	Input from Serial Data Output Pin of EEPROM (93C46/93C56/93C66). Refer to the reference schematic for strapping pin information. All strapping pins are power-on latch pins. Power-on latch high voltage: 93C46 Power-on latch low voltage: 93C56/93C66
EECS/SCL	O	40	EECS: EEPROM (93C46/93C56/93C66) Chip Select SCL: Serial Data Clock for TWSI EEPROM

Note: The RTL8153 will complete eFUSE auto-load before EEPROM auto-load, and determine the type of EEPROM (93C46/93C56) by the 'select 93C46/56/66' eFUSE auto-load value. 1 indicates 93C46; 0 indicates 93C56/93C66.

5.4. Transceiver Interface Pins

Table 4. Transceiver Interface Pins

Symbol	Type	Pin No	Description
MDIP0	IO	2	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	3	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	5	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	6	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIP2	IO	7	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair.
MDIN2	IO	8	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIP3	IO	10	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair.
MDIN3	IO	11	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.5. Clock Pins

Table 5. Clock Pins

Symbol	Type	Pin No	Description
CKXTAL1	I	44	Input of 25MHz Clock Reference.
CKXTAL2	IO	45	Output of 25MHz Clock Reference. Input of 25MHz or 48MHz External Clock Source.
XTALDET	I	37	Power-Up Strapping Pin. Power-on latch high voltage: 25MHz clock source Power-on latch low voltage: 48MHz clock source

Note: When a 25MHz clock is used the XTALDET pin must be pulled high by a resistor during power-up. When a 48MHz clock is used the XTALDET pin must be pulled low by a resistor during power-up.

5.6. Regulator and Reference Pins

Table 6. Regulator and Reference Pins

Symbol	Type	Pin No	Description
REGOUT	O	36	Switching Regulator 1.2V Output.
ENSWREG	I	33	3.3V: Enable switching regulator 0V: Disable switching regulator, and enable external 1.2V input mode
VDDREG	P	34, 35	Digital 3.3V Power Supply for Switching/LDO Regulator.
AVDD33	P	25	Linear Regulator (LDO) 3.3V Output. *Note: The embedded LDO is designed for RTL8153 internal use only. Do not provide this power source to other devices.*
DVDD10_UPS	P	27	Linear Regulator (LDO) 1.2V Output. *Note: The embedded LDO is designed for RTL8153 internal use only. Do not provide this power source to other devices.*
RSET	I	47	Reference (External Resistor Reference).

5.7. LED Pins

Table 7. LED Pins

Symbol	Type	Pin No	Description
LED0	O	30	See Section 6.2 Customizable LED Configuration, Page 9 for Details.
LED1	O	32	
LED2	O	41	

Note: During power down mode, the LED signals are logic high.

5.8. Power and Ground Pins

Table 8. Power and Ground Pins

Symbol	Type	Pin No	Description
VDD5	P	26	Analog 5.0V Power Supply.
AVDD33	P	1, 12, 25, 48	Analog 3.3V Power Supply.
DVDD33	P	28, 43	Digital 3.3V Power Supply.
AVDD10	P	4, 9, 46	Analog 1.2V Power Supply.
DVDD10	P	31, 42	Digital 1.2V Power Supply.
DVDD10_UPS	P	27	Digital 1.2V Uninterruptible Power Supply.
U3VDD10	P	13, 20	USB 3.0 1.2V Power Supply.
U2VDD10	P	24	USB 2.0/USB 1.1 1.2V Power Supply.
U3GND	P	16, 17	USB 3.0 Ground.
U2GND	P	21	USB 2.0/USB 1.1 Ground.
GND	P	49	Ground (Exposed Pad).

Note: Refer to the most updated schematic circuit for correct configuration.

5.9. GPIO Pin

Table 9. GPIO Pin

Symbol	Type	Pin No	Description
GPIO	IO	29	General Purpose Input/Output Pin. Link OK feature: Output Pin (Active High) Power Saving Feature: Output Pin (Active Low) LAN Disable Mode: Input pin (Active Low)

5.10. USB Interface Pins

Table 10. USB Interface Pins

Symbol	Type	Pin No	Description
U3SSRXP	I	14	USB 3.0 Super-Speed Receive Differential Pair.
U3SSRXN	I	15	USB 3.0 Super-Speed Receive Differential Pair.
U3SSTXP	O	18	USB 3.0 Super-Speed Transmit Differential Pair.
U3SSTXN	O	19	USB 3.0 Super-Speed Transmit Differential Pair.
U2DP	IO	23	USB 2.0/USB 1.1 Differential Signal Pair.
U2DM	IO	22	USB 2.0/USB 1.1 Differential Signal Pair.

6. Functional Description

6.1. USB Interface

The SIE (Serial Interface Engine) employs a robust hardwired USB protocol implementation so that the entire USB interface operation can be done without firmware intervention. For all three types of End Points (Bulk-IN, Bulk-OUT, and Interrupt-IN), appropriate responses and handshake signals are generated by the SIE. The SIE analog transceiver complies fully with driver and receiver characteristics defined in USB Specification Rev. 3.0.

6.1.1. USB Configurations

The RTL8153 supports two networking configurations; ECM (Ethernet Control Model) configuration and in-house configuration. The ECM configuration complies with CDC-ECM, and is a general Ethernet networking model that enables network communication without installing additional vendor specific drivers. The in-house configuration requires a vendor specific driver to support enhanced features and optimized performance.

6.1.2. Endpoint 0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint 0 is the information required to completely describe the USB device. This pipe also provides the register read and write to the RTL8153.

6.1.3. Endpoint 1 Bulk-IN

The maximum Bulk-IN packet size is 1024 bytes. Each Ethernet packet is transferred to the HOST by this Endpoint. If the Ethernet packet is larger than 1024 bytes, the RTL8153 splits the Ethernet packet into multiples of 1024 bytes. The HOST treats USB packets that are less than 1024 bytes or are equal to zero as End of Ethernet packets.

6.1.4. Endpoint 2 Bulk-OUT

The HOST sends the USB packet to Ethernet. If the Ethernet packet is larger than 1024 bytes, the Host will send the Ethernet packet in multiples of 1024 bytes. A USB packet that is less than 1024 bytes or is equal to zero is treated as an End of Ethernet packet.

The Ethernet packet (containing multiple USB packets) will be queued in the TX FIFO and transmitted when possible. If the Ethernet packet is transmitted without error, the TX FIFO space that was occupied by the transmitted Ethernet packet will be released. If the TX FIFO is full, the RTL8153 will respond with a NRDY when the host tries to Bulk-OUT more USB packets.

It is possible to have multiple Ethernet packets in the TX FIFO simultaneously. If an Ethernet packet is to be transmitted but experiences collisions more than 16 times (default), this is called a transmit abort and the packet will be skipped for transmission by the RTL8153.

6.1.5. Endpoint 3 Interrupt-IN

The Interrupt Endpoint (EP3) can be used to poll the current ALDPS state, EEE capability, TX/RX flow control enable, Connection Speed, Duplex mode, and link status of the RTL8153.

6.2. Customizable LED Configuration

The RTL8153 supports customizable LED operation modes via OCP address DD90h~DD91h. Table 11 describes the different LED actions.

Table 11. LED Select (OCP Register Offset DD90h~DD91h)

Bit	Symbol	RW	Description
15:12	LEDCntl	RW	LED Feature Control.
11:8	LEDSEL2	RW	LED Select for PINLED2.
7:4	LEDSEL1	RW	LED Select for PINLED1.
3:0	LEDSEL0	RW	LED Select for PINLED0.

When implementing customized LEDs:

Configure OCP address DD90h to support your own LED signals. For example, if the value in the OCP address DD90h is 0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 2: On only in 1000M mode, with blinking during TX/RX

Table 12. Customized LEDs

Speed	LINK			ACT/Full
	Link 10M	Link 100M	Link 1000M	
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 2	Bit 8	Bit 9	Bit 10	Bit 11
Feature Control	Bit 12	Bit 13	Bit 14	Bit 15

Note: There are two special modes:
LED OFF Mode: Set all bits to 0. All LED pin output become floating (power saving).
Fixed LED Mode: Set Option 1 LED table Mode: LED0=LED1=LED2=1 or 2 (see Table 13).

Table 13. Fixed LED Mode

Bit31~Bit0 Value	LED0	LED1	LED2
1XXX 0001 0001 0001	ACT	LINK	Full Duplex + Collision
1XXX 0010 0010 0010	Transmit	LINK	Receive

Note: 'X' indicates 'irrelevant'.

Table 14. LED Feature Control-1

Feature Control	Bit12	Bit13	Bit14	Bit15
0	LED0 Low Active	LED1 Low Active	LED2 Low Active	Indicates Option 1 of Table 16 is Selected
1	LED0 High Active	LED1 High Active	LED2 High Active	Indicates Option 2 of Table 16 is Selected

Table 15. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 16): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 16): Selected Speed LINK+ All Speed ACT

Table 16. LED Option 1 & Option 2 Settings

Link Bit			Active Bit	Description		
10	100	1000		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	LED Off		
0	0	0	1	-	Act_{10}+Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
0	0	1	0	$Link_{1000}$	-	-
0	0	1	1	$Link_{1000}$	Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
0	1	0	0	$Link_{100}$	-	-
0	1	0	1	$Link_{100}$	Act_{100}	Act_{10}+Act_{100}+Act_{1000}
0	1	1	0	$Link_{100}$+$Link_{1000}$	-	-
0	1	1	1	$Link_{100}$+$Link_{1000}$	Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
1	0	0	0	$Link_{10}$	-	-
1	0	0	1	$Link_{10}$	Act_{10}	Act_{10}+Act_{100}+Act_{1000}
1	0	1	0	$Link_{10}$+$Link_{1000}$	-	-
1	0	1	1	$Link_{10}$+$Link_{1000}$	Act_{10}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
1	1	0	0	$Link_{10}$+$Link_{100}$	-	-
1	1	0	1	$Link_{10}$+$Link_{100}$	Act_{10}+Act_{100}	Act_{10}+Act_{100}+Act_{1000}
1	1	1	0	$Link_{10}$+$Link_{100}$+$Link_{1000}$	-	-
1	1	1	1	$Link_{10}$+$Link_{100}$+$Link_{1000}$	Act_{10}+Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}

Note:
Act_{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act_{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
Act_{1000} = LED blinking when Ethernet packets transmitted/received at 1000Mbps.
$Link_{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link_{100}$ = LED lit when Ethernet connection established at 100Mbps.
$Link_{1000}$ = LED lit when Ethernet connection established at 1000Mbps.

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8153 operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), or CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8153's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the receive MII/GMII interface and sends it to the RX Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.3.3. Link Down Power Saving Mode

The RTL8153 implements link-down power saving, greatly cutting power consumption when the network cable is disconnected. The RTL8153 automatically enters link down power saving mode ten seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

6.3.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.4. EEPROM Interface

Both SPI and TWSI EEPROM interfaces are supported. The SPI interface utilizes a 93C46/93C56/93C66, which is 1K-bit/2K-bit/4K-bit, respectively, EEPROM. The EEPROM interface permits the RTL8153 to read from, and write data to, an external serial EEPROM device.

Values in the internal eFUSE memory or external EEPROM allow default register values to be overridden following a power-on or software EEPROM auto-load command. The RTL8153 will auto-load values from the eFUSE or EEPROM. If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8153 initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register. The EEPROM SPI interface consists of EESK, EECS, EEDO, and EEDI. The TWSI interface shares SCL/SDA with EECS/EEDI.

The correct EEPROM (i.e., 93C46/93C56/93C66) must be used in order to ensure proper LAN function.

Table 17. EEPROM Interface

EEPROM	Description
EECS/SCL	EECS: EEPROM (93C46/93C56/93C66) chip select SCL: Serial data clock for TWSI EEPROM
EESK	Serial Data Clock for EEPROM (93C46/93C56/93C66).
EEDI/SDA	EEDI: Output to serial data input pin of EEPROM (93C46/93C56/93C66) SDA: Data interface for TWSI EEPROM
EEDO	Input from Serial Data Output Pin of EEPROM (93C46/93C56/93C66).

6.5. SPI (Serial Peripheral Interface) Flash

SPI Flash is enabled by the RTL8153 through the Chip Select pin, and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 18. SPI Flash Interface

SPI Flash	Description
SO	Input Data Bus.
SI	Output Data Bus.
SCK	SPI Flash Serial Data Clock.
CS	SPI Flash Chip Select.

6.6. Power Management

The RTL8153 complies with ACPI (Rev 1.0, 1.0b, 2.0), Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8153 can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the USB interface when such a packet or event occurs. The system is then restored to a normal state to process incoming jobs.

When the RTL8153 is in power down mode:

- The RX state machine is stopped. The RTL8153 monitors the network for wake-up events such as a Magic Packet and Wake-Up Frame in order to wake-up the system. When in power down mode, the RTL8153 will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer.
- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8153.
- Transmission is stopped. USB transactions are stopped. The TX on-chip buffer is held.
- After being restored to D0 state, the RTL8153 transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8153, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8153 adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8153, e.g., a broadcast, multicast, or unicast address to the current RTL8153 adapter.
- The received Wake-Up Frame does not contain a CRC error.
- The 16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8153 is configured to allow direct packet wake-up, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8153 supports 16-set 16-bit CRC wake-up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^{5}+1$.

6.7. Link Power Management (LPM)

The RTL8153 supports Link Power Management (LPM). It provides an efficient way to manage bus and system power via hosts and hubs. It implements a power sleep state that reduces power consumption by providing faster suspend and resume times. The four power management states for USB are L0 (On), L1 (Sleep), L2 (Suspend) and L3 (Off). To reduce power consumption when the system is in Low Power State, some of the circuits are disabled.

Refer to http://www.usb.org/developers/docs/.

6.8. Protocol Offload

Protocol offload is a task offload supported by Microsoft Windows 7. It maintains a network presence for a sleeping higher power host. Protocol offload prevents spurious wake-up and further reduces power consumption. It maintains connectivity while hosts are asleep, including receiving requests from other nodes on the network, ignoring packets, generating packets while in the sleep state (e.g., the Ethernet Controller will generate ARP responses if the same MAC and IPv4 address are provided in the configuration data), and intelligently waking up host systems. The RTL8153 supports the ECMA (European Computer Manufacturers Association) specification including proxy configuration and management, IPv4 ARP, IPv6 NDP, and wake-up packets. The RTL8153 also supports optional ECMA items such as QoS tagged packets and duplicate address detection.

6.10. Wake Packet Detection (WPD)

The RTL8153 supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

Refer to the Microsoft Wake Packet Detection (WPD) Interface Specification for details (http://msdn.microsoft.com/en-us/library/hh440160(v=vs.85).aspx).

6.11. 'RealWoW!' (Wake-On-WAN) Technology

The RTL8153 supports Realtek 'RealWoW!' technology that allows the RTL8153 to send keep-alive packets to the Wake Server when the PC is in sleeping mode. Realtek 'RealWoW!' can pass wake-up packets through a NAT (Network Address Translation) device. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Users can login into the Wake Server via the Internet to wake the selected sleeping PC. Registration of Account information to the Wake Server is required on first time use.

6.12. Energy Efficient Ethernet (EEE)

The RTL8153 supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

6.13. XTAL-Less Wake-On-LAN

The RTL8153 supports board level design with an External 25MHz or 48MHz Clock Source instead of the Crystal.

The external clock source may stop generating the clock when in suspend mode (S3/S4/S5). To support the Wake-On-LAN function without an external clock source, the RTL8153 will automatically change its source clock from the external clock to an internal self-oscillating auxiliary clock when it enters suspend mode. Note that when in suspend mode, the auxiliary clock can establish only a 10Mbps link and does not support ARP/NS offload and ECMA ProxZzzy.

6.14. LAN Disable Mode

The RTL8153 supports 'LAN Disable Mode' that can use an external signal to control whether the NIC is enabled or disabled.

6.15. Always On Always Connected

The RTL8153 supports Microsoft's AOAC (Always On Always Connected) model. The AOAC platform can enter the system state 'Connected Standby' and allow the RTL8153 to enter a low-power state. The RTL8153 will maintain Layer 2 connectivity and generate a wake signal when one of the following conditions is satisfied:

- Link status becomes 'connected'
- Link status becomes 'disconnected'
- Receives a WOL pattern
- Receives a wildcard pattern

7. Switching Regulator

The RTL8153 incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 1.2V output pin (REGOUT) must be connected only to DVDD10, AVDD10, U3VDD10, and U2VDD10 (do not provide this power source to other devices).

8. LDO Regulator

The RTL8153 incorporates two linear Low-Dropout (LDO) regulators that feature high power supply ripple rejection and low output noise. The RTL8153 embedded LDO regulators do not require power inductors on the PCB; only an output capacitor between its output and analog ground for phase compensation, which saves cost and PCB real estate.

The output capacitors (and bypass capacitors) should be placed as close as possible to the power pins for adequate filtering.

Note 1: The embedded LDO is designed for the RTL8153 internal use only. Do not provide this power source to other devices.

Note 2: The digital LDO output pin (DVDD10_UPS) should be separated from the other 1.2V SWR output pin (REGOUT).

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 19. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD5	5.0V Supply Voltage	-0.3	5.5	V
DVDD33, AVDD33	3.3V Supply Voltage	-0.3	3.63	V
DVDD10, AVDD10, U3VDD10, U2VDD10, DVDD10_UPS	1.2V Supply Voltage	-0.3	1.32	V
Dcinput	Input Voltage	-0.3	Corresponding Supply Voltage + 10%	V
Dcoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 10%	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.2. Recommended Operating Conditions

Table 20. Recommended Operating Conditions

Description	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD5	4.75	5.0	5.25	V
	DVDD33, AVDD33	3.14	3.3	3.46	V
	DVDD10, AVDD10, U3VDD10, U2VDD10, DVDD10_UPS	1.14	1.2	1.26	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.3. Crystal Requirements

Table 21. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type	-	25/48	-	MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a=0°C ~ +70°C	-30	-	+30	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a=25°C	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	30	Ω
CL	Load Capacitance	16	-	20	pF
Jitter	Broadband Peak-to-Peak Jitter	-	-	200	ps
DL	Drive Level	-	-	0.3	mW

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.
Note 3: The ESR maximum value of 70ohm is based on shunt capacitance (Co) less than 7pF.
Note 4: The accuracy of the crystal resonance frequency can be achieved by matching the load capacitance correctly to the designed-in circuit. The latest schematic circuit recommends two external capacitors of 27pF connected between the crystal and ground. To match this use the load capacitance specified by the crystal manufacturer of 16~20pF.

9.4. Oscillator Requirements

Table 22. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25/48	-	MHz
Frequency Stability	T_a = 0°C ~ +70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter	-	-	-	200	ps
Vp-p	-	3.15	3.3	3.45	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

9.5. Environmental Characteristics

Table 23. Environmental Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Moisture Sensitivity Level (MSL)	Level 3		N/A

9.6. DC Characteristics

Table 24. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD5	5.0V Supply Voltage	-	4.75	5.00	5.25	V
DVDD33, AVDD33	3.3V Supply Voltage	-	3.14	3.3	3.46	V
DVDD10, AVDD10, U3VDD10, U2VDD10, DVDD10_USP	1.2V Supply Voltage	-	1.14	1.2	1.26	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
V_{ih}	Minimum High Level Input Voltage	-	2.0	-	-	V
V_{il}	Maximum Low Level Input Voltage	-	-	-	0.8	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	µA
Icc5	Average Operating Supply Current from 5.0V	At 1000Mbps with heavy network traffic	-	0.5	-	mA
Icc33	Average Operating Supply Current from 3.3V	At 1000Mbps with heavy network traffic	-	60	-	mA
Icc10	Average Operating Supply Current from 1.2V	At 1000Mbps with heavy network traffic	-	300	-	mA

Note: Refer to the most updated schematic circuit for correct configuration.

9.7. Reflow Profile Recommendations

Table 25. Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max.	3°C/second max.
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time $(t_p)^2$ within 5°C of Peak T_P	20 seconds	20 seconds
Ramp-Down Rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature (T_p)	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the topside of the package, measured on the package body surface.
Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.
Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

9.8. AC Characteristics

9.8.1. SPI EEPROM Interface Timing

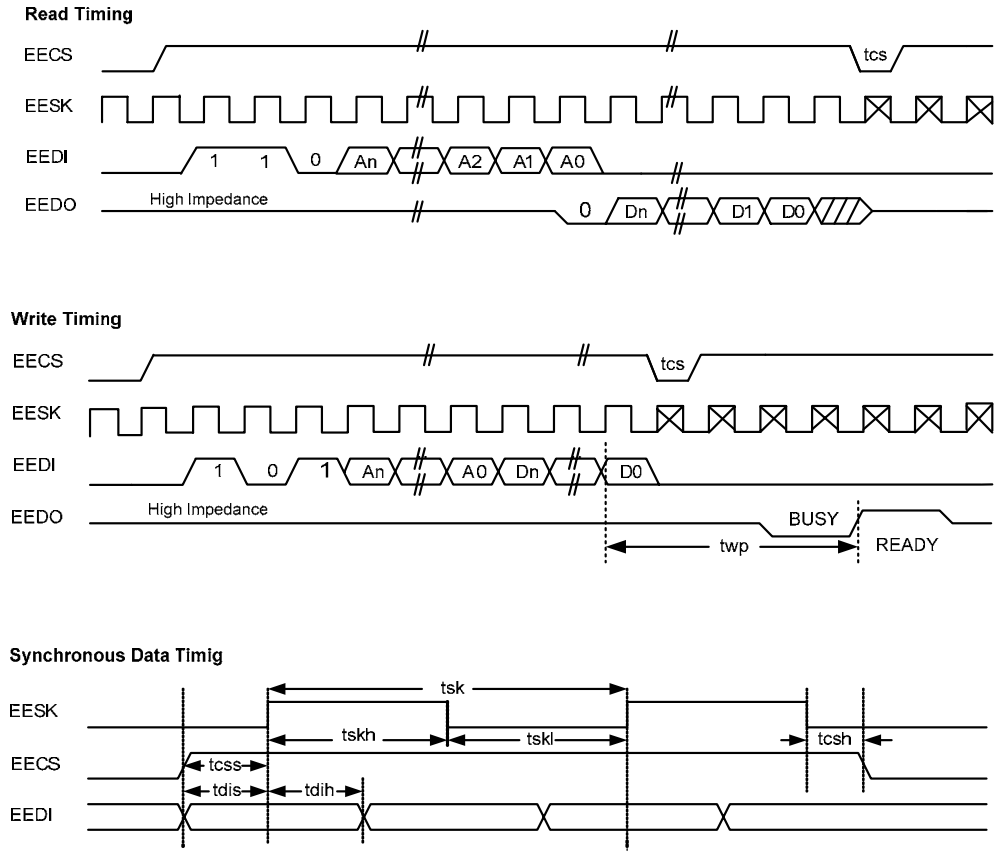


Figure 2. SPI EEPROM Interface Timing

Table 26. SPI EEPROM Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
tcs	Minimum CS Low Time	1024	4096	-	ns
tcss	CS Setup Time	512	512	-	ns
tcsh	CS Hold Time	-	0	-	ns
tskh	SK High Time	512	512	8192	ns
tskl	SK Low Time	512	512	8192	ns
tsk	SK Clock Cycle Time	1024	1024	16384	ns
tdis	DI Setup Time	512	512	-	ns
tdih	DI Hold Time	512	512	-	ns
twp	Write Cycle Time	-	6	10	ms

9.8.2. TWSI EEPROM Interface Timing

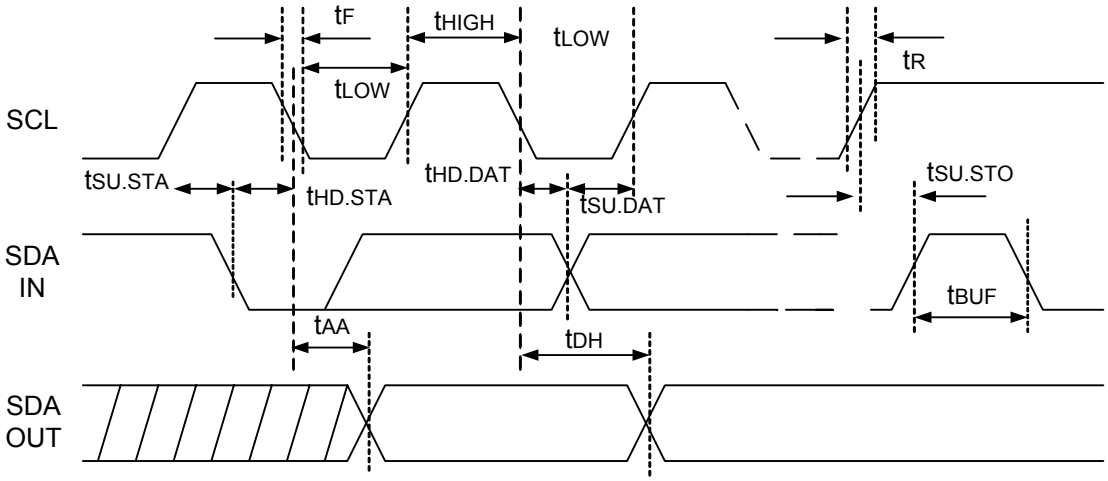


Figure 3. TWSI EEPROM Interface Timing-1

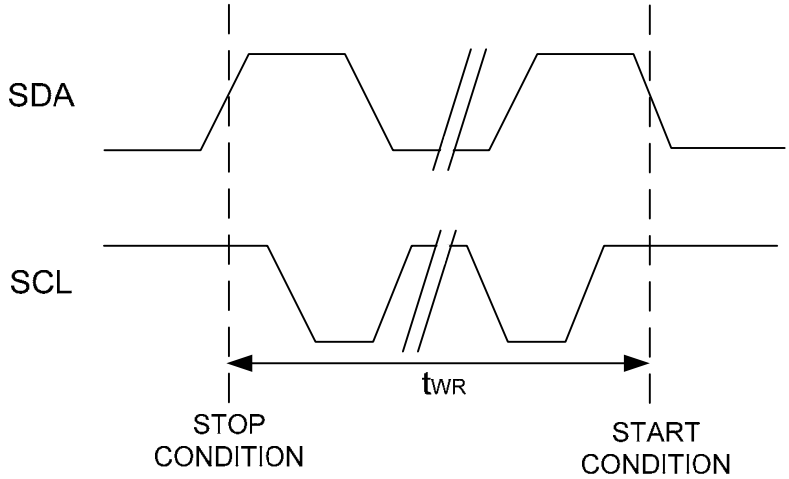


Figure 4. TWSI EEPROM Interface Timing-2

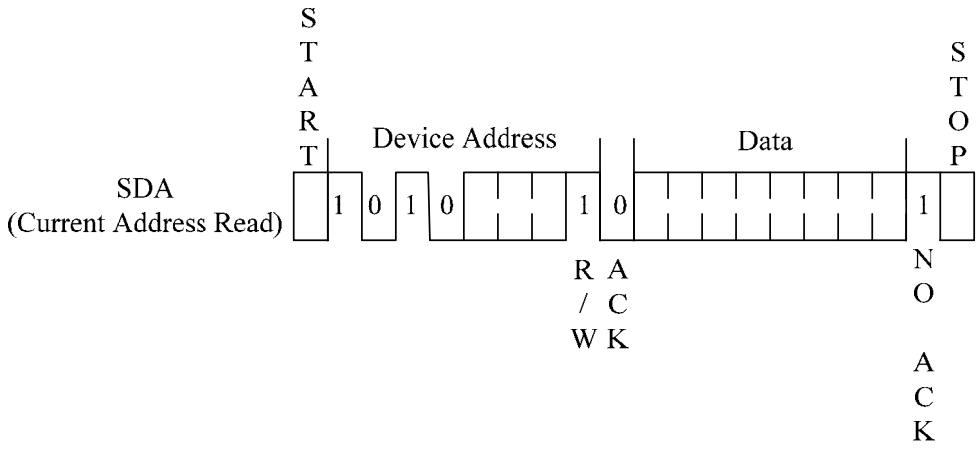


Figure 5. TWSI EEPROM Interface Timing-3

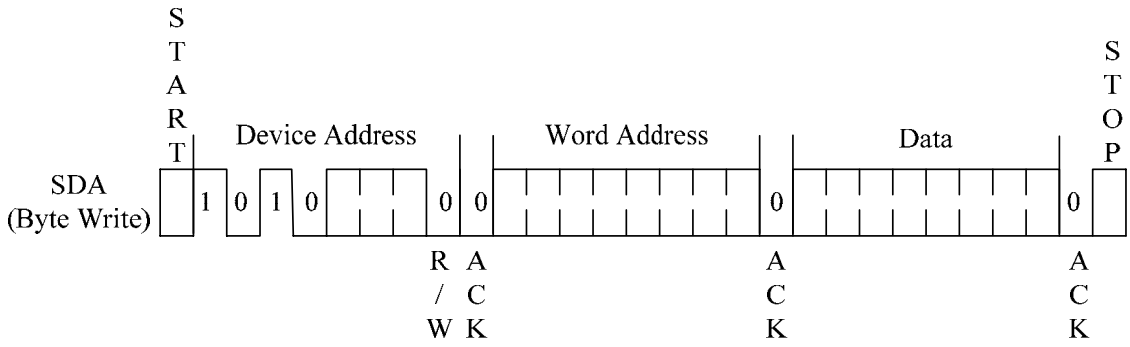


Figure 6. TWSI EEPROM Interface Timing-4

Table 27. TWSI EEPROM Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{LOW}	Clock Pulse Width Low	512	-	8192	ns
t_{HIGH}	Clock Pulse Width High	512	-	8192	ns
t_{AA}	Clock Low to DO Valid		504	514	ns
t_{BUF}	Time the Bus Must be Free before a New Transmission Can Start	-	-	-	ns
$t_{HD.STA}$	Start Hold Time	247	252	257	ns
$t_{SU.STA}$	Start Setup Time	247	252	257	ns
$t_{HD.DAT}$	DI Hold Time	247	252	257	ns
$t_{SU.DAT}$	DI Setup Time	247	252	257	ns
t_R	Input Rise Time	-	-	-	ns
t_F	Input Fall Time	-	-	-	ns
$t_{SU.STO}$	Stop Setup Time	494	504	514	ns
t_{DH}	DO Hold Time	494	504	514	ns
t_{WR}	Write Cycle Time	5.88	6	6.12	ms

9.8.3. SPI Flash Commands

Table 28. SPI Flash Commands

Command	Operation Code	Action
WREN	06h	Write Enable
WRDI	04h	Write Disable
RDID	9Fh	Read Manufacturer and Product ID
RDSR	05h	Read Status Register
WRSR	01h	Write Status Register
Read	03h	Read
Page Program	02h	Page Program
Sector Erase (4K)	20h	Erase The Selected Sector
Block Erase (64K)	D8h	Erase The Selected Block
Chip Erase	60h or C7h	Erase Whole Chip

9.8.4. SPI Flash Interface Timing Sequences

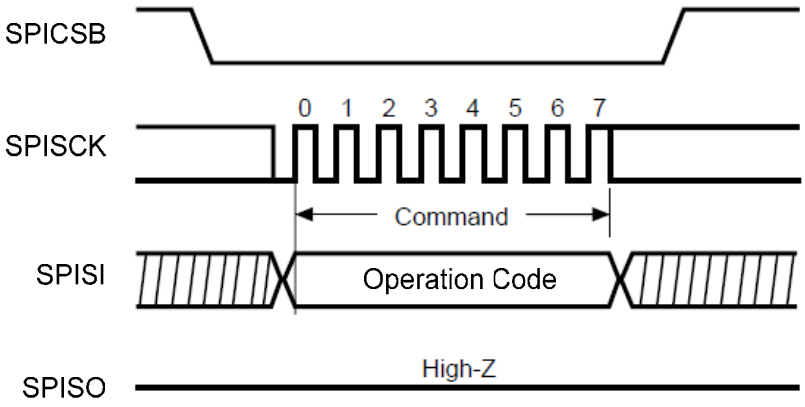


Figure 7. WREN/WRDI Timing Sequence

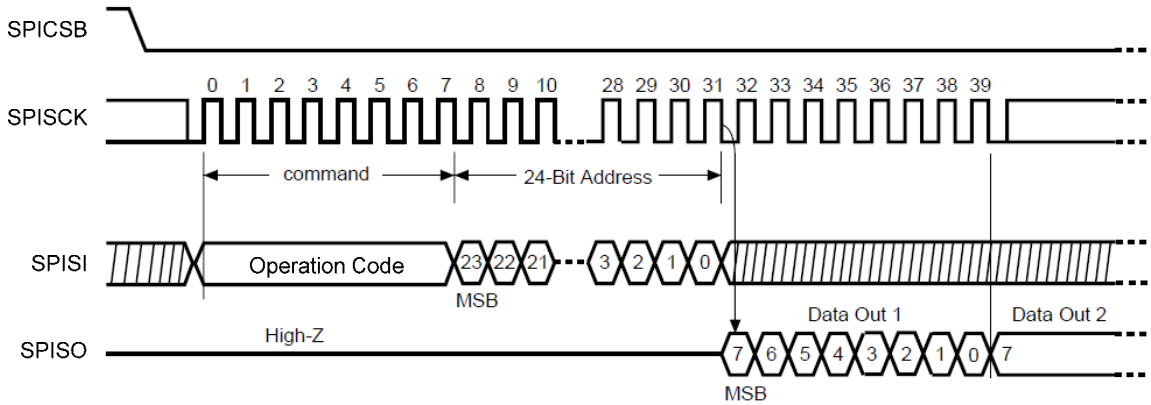


Figure 8. Read Timing Sequence

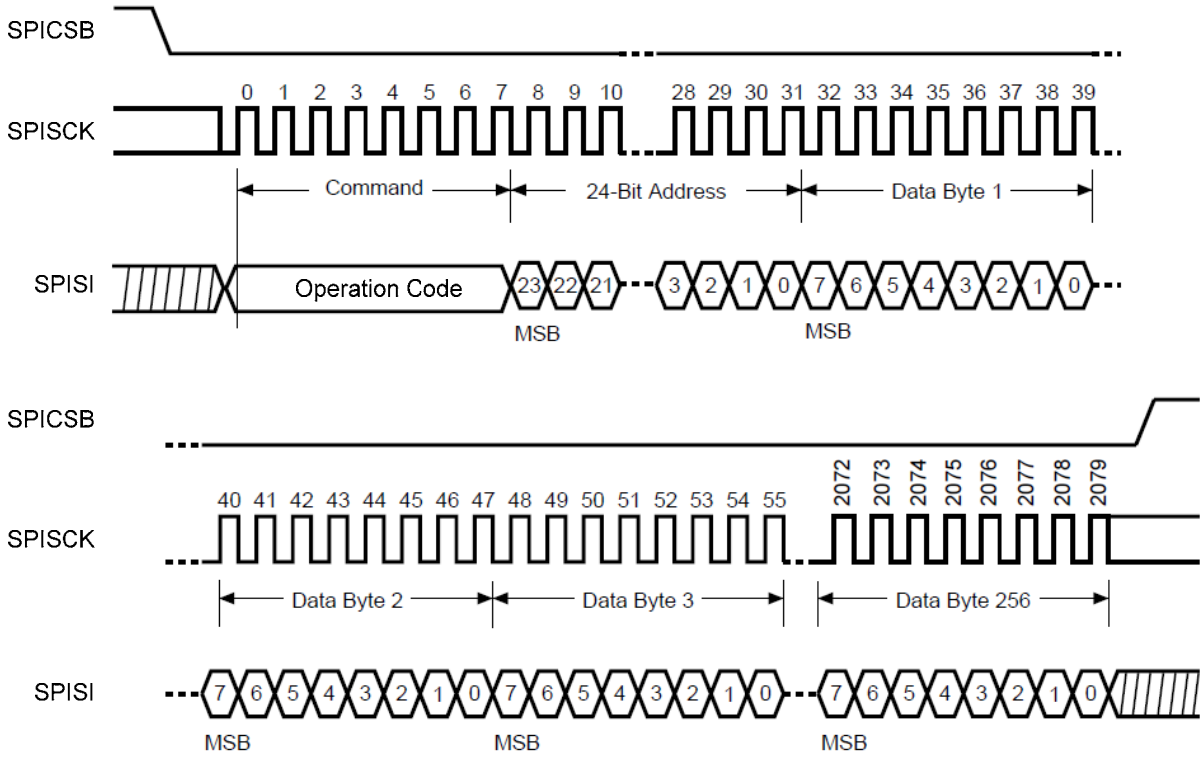


Figure 9. Page Program Timing Sequence

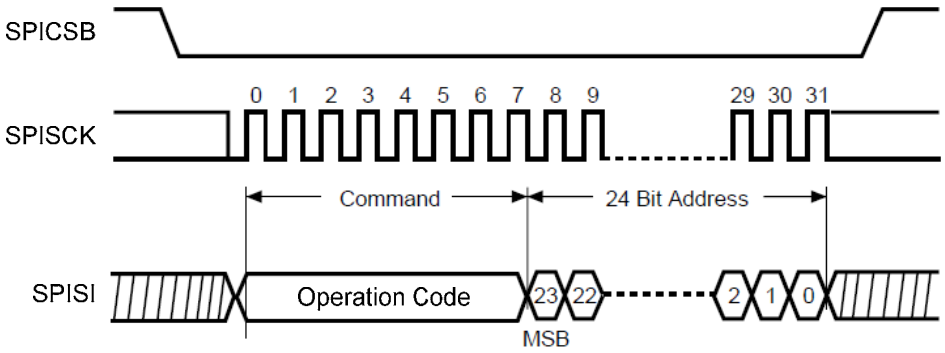


Figure 10. Sector/Block Erase Timing Sequence

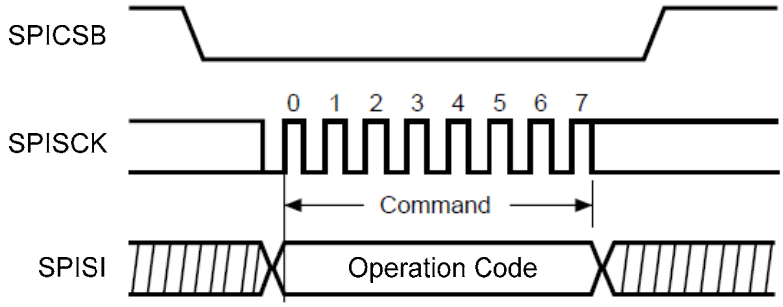


Figure 11. Chip Erase Timing Sequence

9.8.5. SPI Flash Type Supported

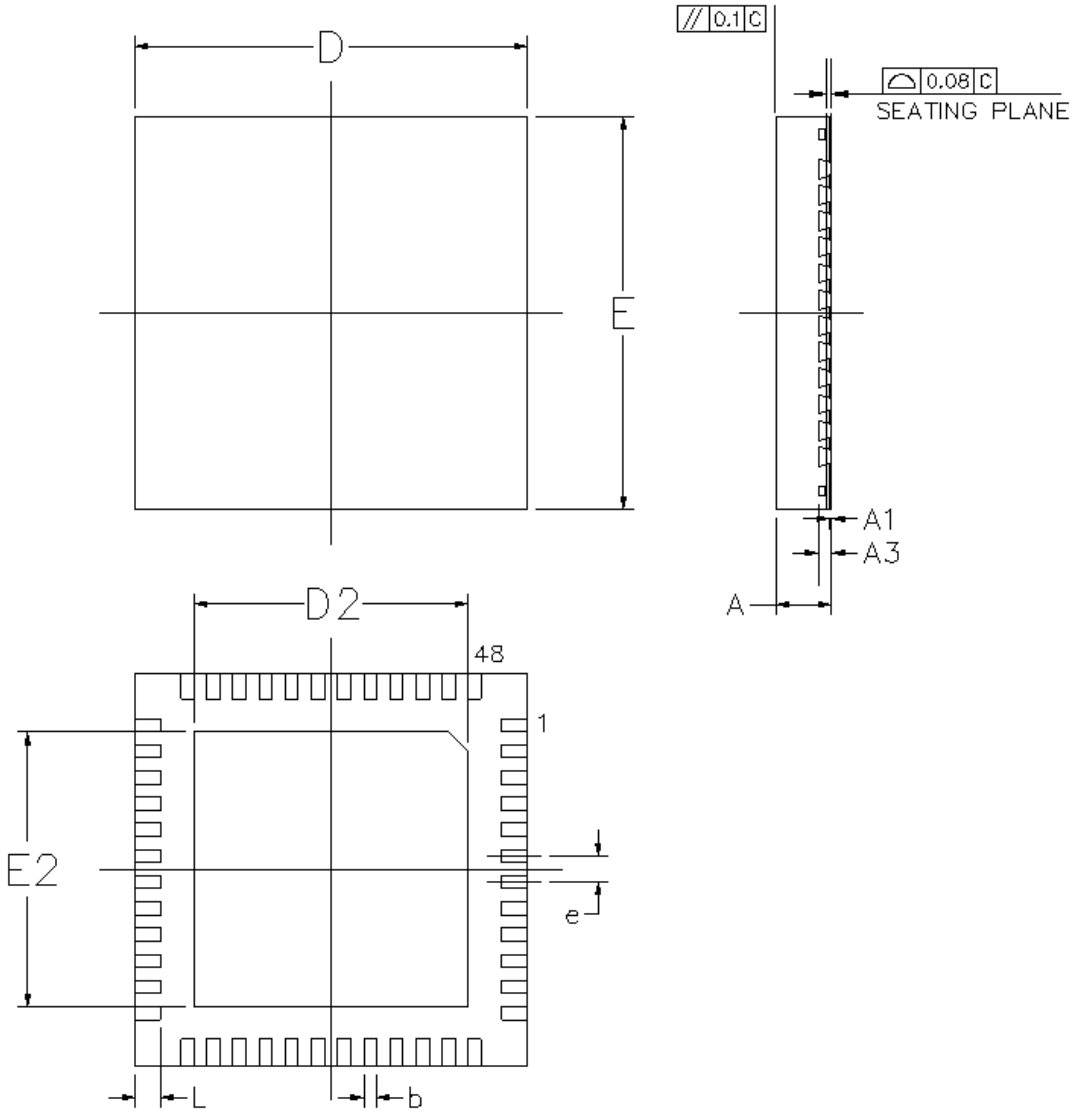
Table 29. SPI Flash Types Supported

Manufacturer	Flash Part No.	Density (Mb)	Max Freq (MHz)
MXIC	MX25L4006E	4	86
	MX25L8006E	8	86
	MX25L1606E	16	86
Winbond	W25X40CV	4	80
	W25Q40BV	4	80
	W25Q80BV	8	80
	W25Q16CV	16	80
Micron	M25P40	4	75
	M25PX80	8	75
	M25PX16	16	75

Note 1: The Flash clock frequency should be 33MHz or higher.

Note 2: Flash density should be 4Mb or more. 4Mb is only for single OS driver. For feature extensions, 8Mb is recommended.

10. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20REF			0.008REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		6.00BSC			0.236BSC	
D_2/E_2	4.15	4.4	4.65	0.163	0.173	0.183
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 30. Ordering Information

Part Number	Package	Status
RTL8153-CG	48-Pin QFN 'Green' Package	MP

Note: See page 4 for package ID information.

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