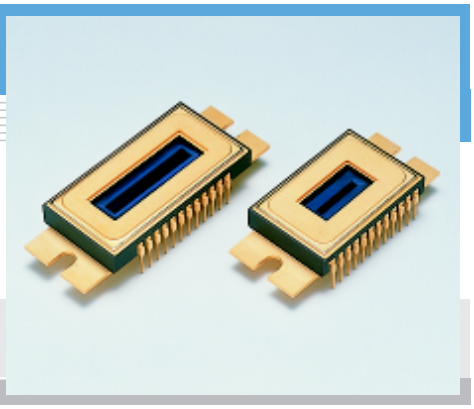

CCD area image sensor
S10140/S10141 series

Low readout noise, high resolution (pixel size: 12 µm)

S10140/S10141 series is a family of back-thinned FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S10140/S0141 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S10140/S10141 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S10140/S10141 series also features low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
S10140/S10141 series has an effective pixel size of 12 × 12 µm and is available in image areas ranging from 12.288 (H) × 1.464 (V) mm^2 (1024 × 122 pixels) up to a large image area of 24.576 (H) × 6.072 (V) mm^2 (2048 × 506 pixels).

Features

- Low readout noise: 4 e^-rms Typ.
- High resolution: pixel size 12 × 12 µm
- Non-cooled type: S10140 series
  One-stage TE-cooled type: S10141 series
- Line, pixel binning, area scanning
- Greater than 90 % quantum efficiency at peak sensitivity wavelength
- Wide spectral response range
- Wide dynamic range
- MPP operation
- High UV sensitivity with good stability
- Same pin connections as S7030/S7031 series

Applications

- Fluorescence spectrometer, ICP
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Suitable multichannel detector head
S10140-1007	Non-cooled	1044 × 128	1024 × 122	12.288 × 1.464	C10150
S10140-1008		1044 × 256	1024 × 250	12.288 × 3.000	
S10140-1009		1044 × 512	1024 × 506	12.288 × 6.072	
S10140-1107		2068 × 128	2048 × 122	24.576 × 1.464	
S10140-1108		2068 × 256	2048 × 250	24.576 × 3.000	
S10140-1109		2068 × 512	2048 × 506	24.576 × 6.072	
S10141-1007S	One-stage TE-cooled	1044 × 128	1024 × 122	12.288 × 1.464	C10151
S10141-1008S		1044 × 256	1024 × 250	12.288 × 3.000	
S10141-1009S		1044 × 512	1024 × 506	12.288 × 6.072	
S10141-1107S		2068 × 128	2048 × 122	24.576 × 1.464	
S10141-1108S		2068 × 256	2048 × 250	24.576 × 3.000	
S10141-1109S		2068 × 512	2048 × 506	24.576 × 6.072	

■ General ratings

Parameter	S10140 series	S10141 series
Pixel size	12 (H) × 12 (V) µm	
Vertical clock phase	2 phases	
Horizontal clock phase	2 phases	
Output circuit	One-stage MOSFET source follower	
Package	24 pin ceramic DIP (refer to dimensional outlines)	
Window *1	Quartz glass	AR-coated sapphire

*1: Window-less is available upon request.

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+30	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	-	24	-	V
Reset drain voltage		V_{RD}	-	12	-	V
Output gate voltage		V_{OG}	-	3	-	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-9	-8	0	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-9	-8	0	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	-	3	-	V
	Low	V_{P1VL}, V_{P2VL}	-	-8	-	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	-	5	-	V
	Low	V_{P1HL}, V_{P2HL}	-	-8	-	
Summing gate voltage	High	V_{SGH}	-	5	-	V
	Low	V_{SGL}	-	-8	-	
Reset gate voltage	High	V_{RGH}	-	5	-	V
	Low	V_{RGL}	-	-8	-	
Transfer gate voltage	High	V_{TGH}	-	3	-	V
	Low	V_{TGL}	-	-8	-	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	250	500	kHz
Vertical shift register capacitance *2	C_{P1V}, C_{P2V}	-	3600	-	pF
Horizontal shift register capacitance *2	C_{P1H}, C_{P2H}	-	150	-	pF
Summing gate capacitance	C_{SG}	-	30	-	pF
Reset gate capacitance	C_{RG}	-	30	-	pF
Transfer gate capacitance	C_{TG}	-	75	-	pF
Charge transfer efficiency *3	CTE	0.99995	0.99999	-	-
DC output level *4	Vout	12	17	18	V
Output impedance *4	Zo	-	8	-	kΩ
Power consumption *4 *5	P	-	4	-	mW

*2: S10140-1108, S10141-1108S
*3: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*4: The values depend on the load resistance. (Typical, VOD=24 V, Load resistance=100 kΩ)
*5: Power consumption of the on-chip amplifier

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

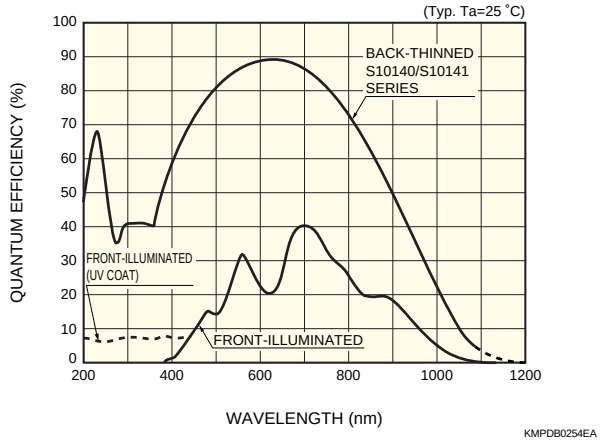
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical		Fw	60	75	-	ke⁻
	Horizontal			120	150	-	
	Summing			150	200	-	
CCD node sensitivity			Sv	4	5	6	μV/e⁻
Dark current *6 MPP mode	25 °C		DS	-	100	1000	e⁻/pixel/s
	0 °C			-	5	50	
Readout noise *7			Nr	-	4	18	e⁻ rms
Dynamic range *8	Line binning		DR	30000	37500	-	-
	Area scanning			15000	18500	-	-
Photo response non-uniformity *9			PRNU	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect *10	White spots	-	-	-	0	-
		Black spots		-	-	10	-
	Cluster defect *11			-	-	3	-
	Column defect *12			-	-	0	-

*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*7: -50 °C, Operating frequency is 20 kHz.
*8: Dynamic range (DR) = Full well/Readout noise
*9: Measured at the half of the full well capacity output.

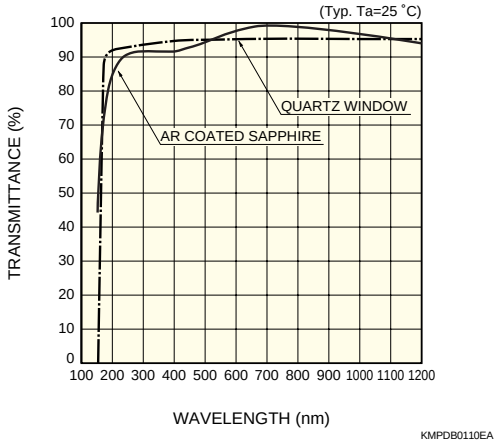
$$\text{Photo response non-uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*10: White spots
Pixels whose dark current is higher than 1 ke⁻ after one-second integration at 0 °C.
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output. (Measured with uniform light producing one-half of the saturation charge)
*11: 2 to 9 contiguous defective pixels
*12: 10 or more contiguous defective pixels

■ Spectral response (without window) *10

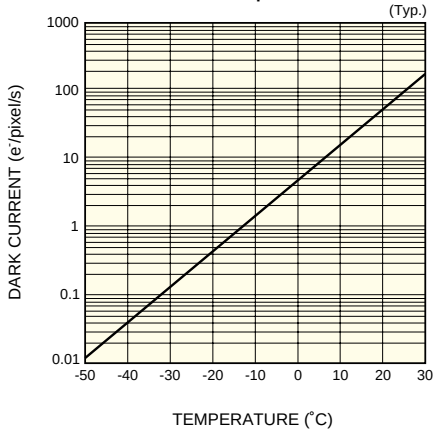


■ Spectral transmittance characteristics



*10: Spectral response with quartz glass or AR-coated sapphire are decreased by the transmittance.

■ Dark current vs. temperature

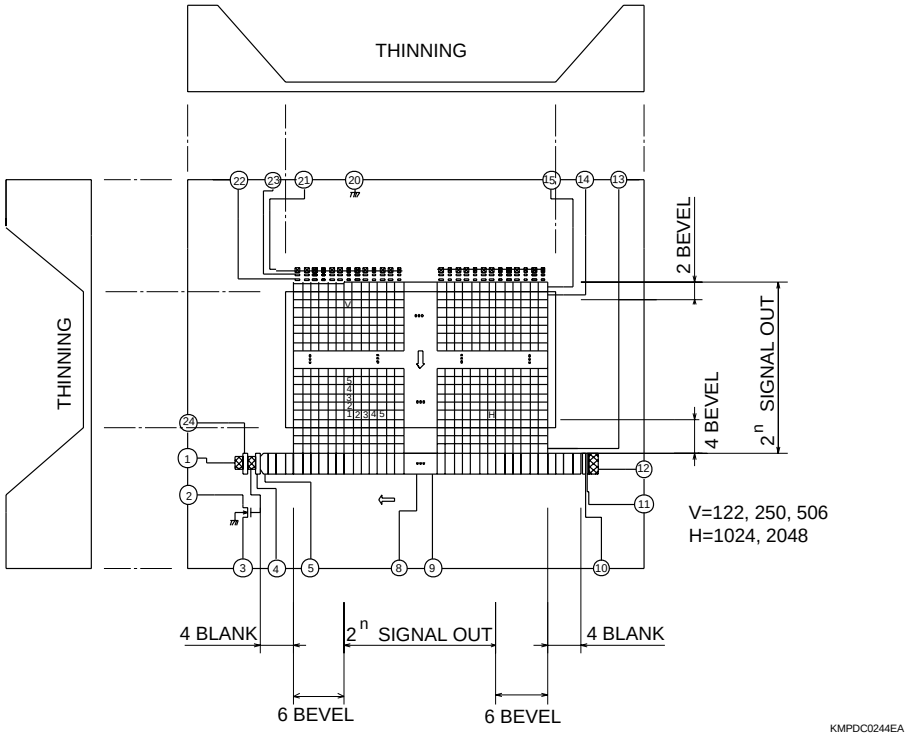


● Window material

Type No.	Window material
S10140 series	Quartz glass *11 (option: window-less)
S10141 series	AR-coated sapphire *12 (option: window-less)
S10142 series (two-stage TE-cooled types, made to order)	AR-coated sapphire *12 (option: window-less)

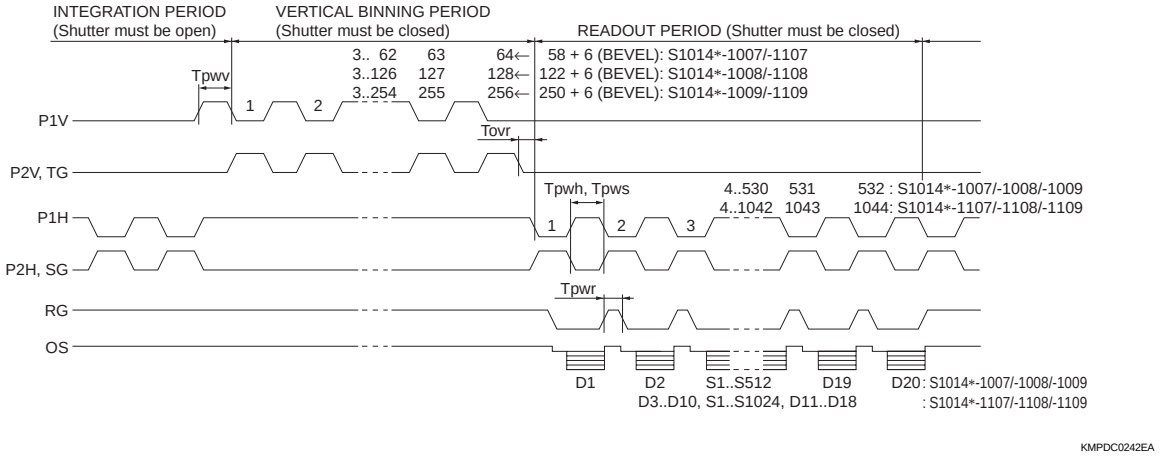
*11: Resin sealing
*12: Hermetic sealing

■ Device structure (Conceptual drawing of top view)



■ Timing chart

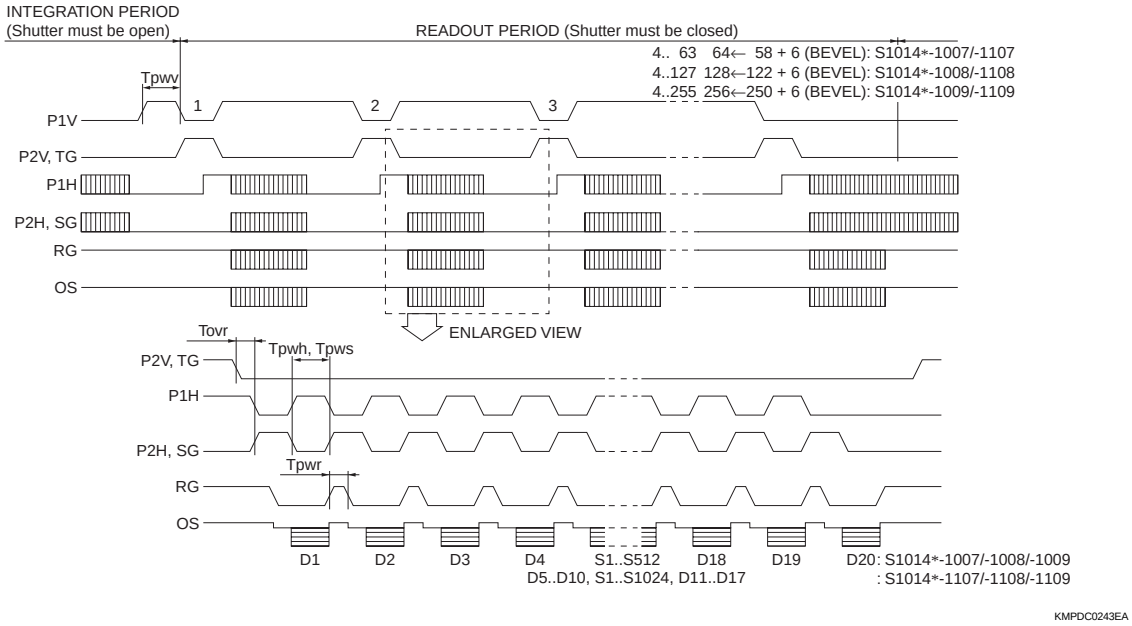
Line bininng



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*13	6	8	-	µs
	Rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H	Pulse width	Tpwh	*13	1000	2000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		40	50	60	%
SG	Pulse width	Tpws	-	1000	2000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		40	50	60	%
RG	Pulse width	Tpwr	-	100	1000	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	1	2	-	µs

*13: The clock pulses should be overlapped at 50 % of clock pulse amplitude.

Area scanning



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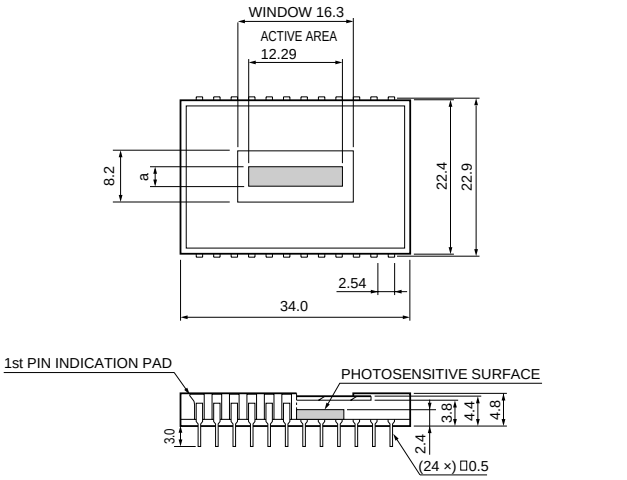
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*14	6	8	-	µs
	Rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H	Pulse width	Tpwh	*14	1000	2000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		40	50	60	%
SG	Pulse width	Tpws	-	1000	2000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		40	50	60	%
RG	Pulse width	Tpwr	-	100	1000	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	1	2	-	µs

*14: The clock pulses should be overlapped at 50 % of clock pulse amplitude.

■ Dimensional outlines (unit: mm)

S10140-1007/-1008/-1009



S10140-1007: a=1.464
S10140-1008: a=3.000
S10140-1009: a=6.072

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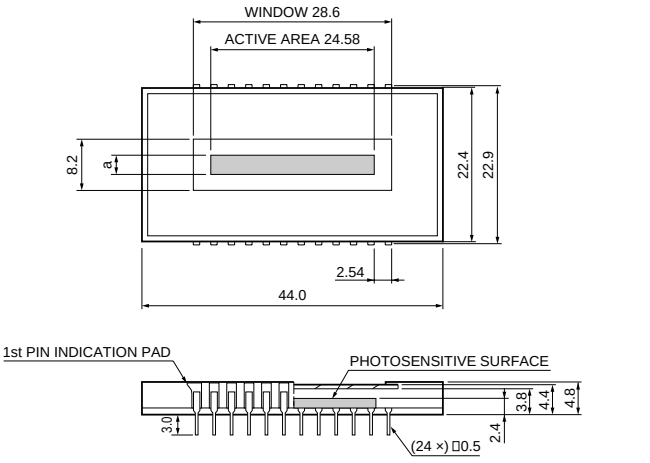
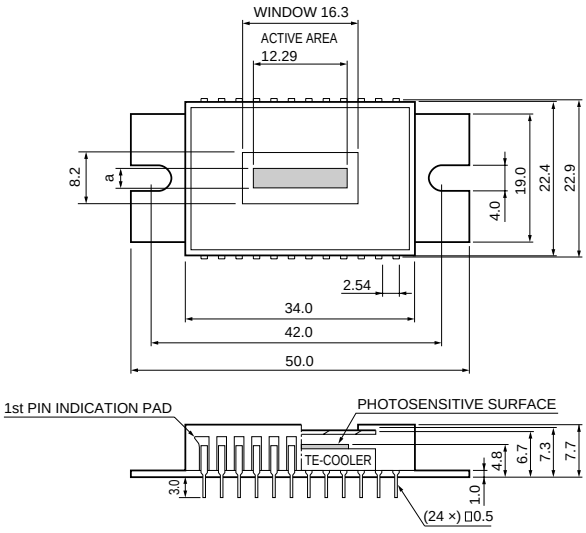
S10140-1107/-1108/-1109



S10140-1107: a=1.464
S10140-1108: a=3.000
S10140-1109: a=6.072

KMPDA0208EA

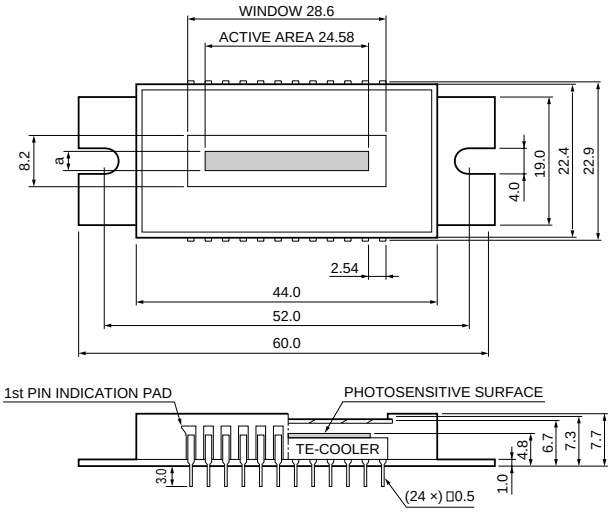
S10141-1007S/-1008S/-1009S



S10141-1007S: a=1.464
S10141-1008S: a=3.000
S10141-1009S: a=6.072

KMPDA0209EB

S10141-1107S/-1108S/-1109S



S10141-1107S: a=1.464
S10141-1108S: a=3.000
S10141-1109S: a=6.072

KMPDA0210EB

■ Pin connections

Pin No.	S10140 series		S10141 series		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	RL=100 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+24 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG *15	Transfer gate	TG *15	Transfer gate	Same pulse as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	
24	RG	Reset gate	RG	Reset gate	

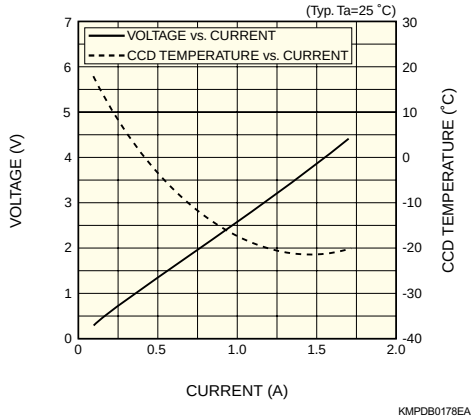
*15: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

■ Specifications of built-in TE-cooler (Typ.)

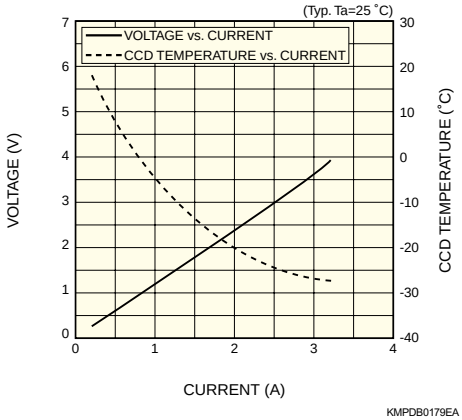
Parameter	Symbol	Condition	S10141-1007S/-1008S/-1009S	S10141-1107S/-1108S/-1109S	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	Ω
Maximum current *16	Imax	Tc *17=Th *18=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc *17=Th *18=25 °C	3.8	3.6	V
Maximum heat absorption *19	Qmax		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

*16: Maximum current Imax:
If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*17: Temperature of the cooling side of thermoelectric cooler.
*18: Temperature of the heat radiating side of thermoelectric cooler.
*19: Maximum heat absorption Qmax.
This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S10141-1007S/-1008S/-1009S



S10141-1107S/-1108S/-1109S



■ Specifications of built-in temperature sensor

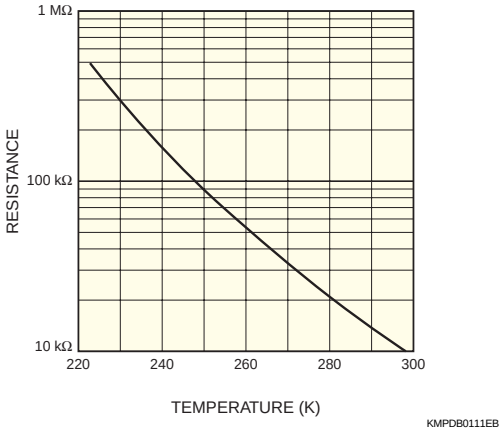
A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R1 = R2 \times \exp B\,(1 / T1 - 1 / T2)$

where R1 is the resistance at absolute temperature T1 (K)
R2 is the resistance at absolute temperature T2 (K)
B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.

R (298K) = 10 kΩ
B (298K / 323K) = 3450 K



■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

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