EPSON

# Micro MINI S1C60N05

## 4-bit Single Chip Microcomputer

Low Voltage Operation Products

- S1C6200B Core CPU
- Low Voltage and Low Power
- Built-in LCD Driver
- Built-in A/D Converter (2ch.)

## ■ INTRODUCTION

Each member of the S1C60N05 Series of single chip microcomputers feature a 4-bit S1C6200B core CPU, 1,536 words of ROM (12 bits per word), 80 words of RAM (4 bits per word), an LCD driver, 4 bits for input ports (K00–K03), 4 bits for output ports (R00–R03), one 4-bit I/O port (P00–P03), clock timer and A/D converter. Because of their low voltage operation and low power consumption, the S1C60N05 Series are ideal for a wide range of applications.

## ■ CONFIGURATION

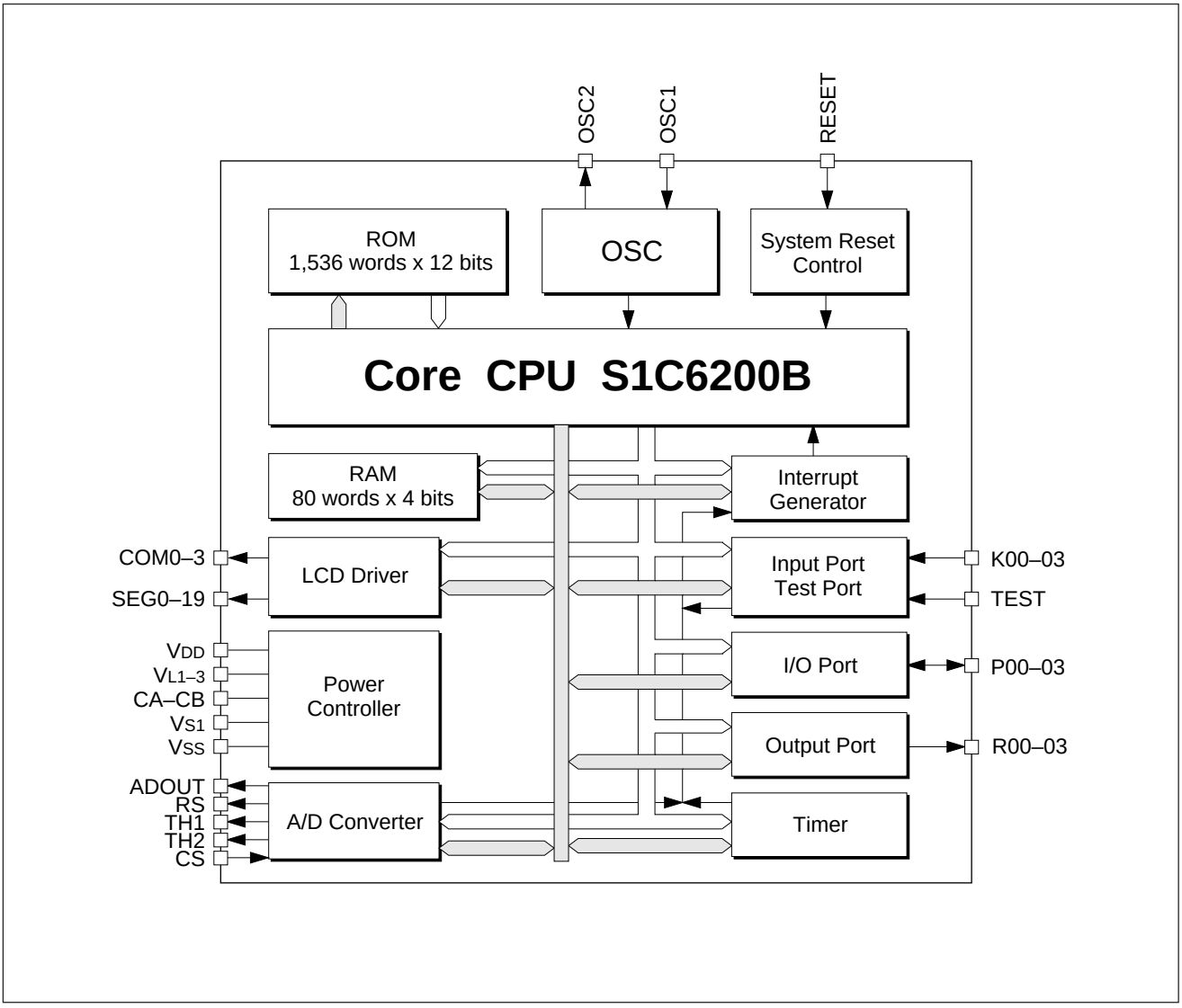
The S1C60N05 Series are configured as follows, depending on the supply voltage.

| Model | Supply voltage | Oscillation circuits |
|---|---|---|
| S1C60N05 | 1.8–3.5 V | Crystal or CR |
| S1C60L05 | 1.2–2.0 V | Crystal or CR |

## ■ FEATURES

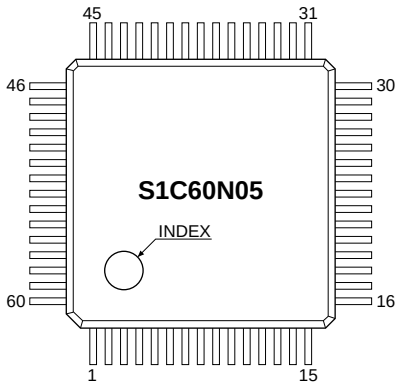
- Core CPU ..... S1C6200B
- Built-in oscillation circuit ..... Crystal or CR oscillation circuit, 32,768 Hz (typ.)
- nstruction set ..... 100 instructions
- ROM capacity ..... 1,536 words × 12 bits
- RAM capacity (data RAM) ..... 80 words × 4 bits
- Input port ..... 4 bits (Supplementary pull-down resistors may be used)
- Output port ..... 4 bits (Piezo buzzer and programmable frequency output can be driven directry by mask option)
- Input/output port ..... 4 bits
- LCD driver ..... 20 segments × 4 common duty (or 3 and 2 common duty)
- Timer ..... Clock timer
- A/D converter ..... CR oscillation type A/D converter built-in (2 channels)
- Interrupts:
  - External interrupt ..... Input port interrupt 1 system
  - Internal interrupt ..... Timer interrupt 1 system
  - A/D converter interrupt 1 system
- Supply voltage ..... 1.5 V (1.2–2.0 V) S1C60L05 (During A/D conversion)
  3.0 V (1.8–3.5 V) S1C60N05
- Current consumption (typ.) ..... 0.8 µA (Crystal oscillation CLK = 32,768 Hz, when halted)
  1.5 µA (Crystal oscillation CLK = 32,768 Hz, when executing)
- Supply form ..... QFP6-60pin (plastic) or chip

## ■ BLOCK DIAGRAM




## ■ PIN CONFIGURATION

**QFP6-60pin**




| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---|---|---|---|---|---|---|---|
| 1 | N.C. | 16 | N.C. | 31 | TEST | 46 | $V_{L3}$ |
| 2 | N.C. | 17 | ADOUT | 32 | RESET | 47 | $V_{L2}$ |
| 3 | K00 | 18 | SEG0 | 33 | SEG12 | 48 | $V_{L1}$ |
| 4 | K01 | 19 | SEG1 | 34 | SEG13 | 49 | CA |
| 5 | K02 | 20 | SEG2 | 35 | SEG14 | 50 | CB |
| 6 | K03 | 21 | SEG3 | 36 | SEG15 | 51 | $V_{SS}$ |
| 7 | R00 | 22 | SEG4 | 37 | SEG16 | 52 | $V_{DD}$ |
| 8 | R01 | 23 | SEG5 | 38 | SEG17 | 53 | OSC1 |
| 9 | R02 | 24 | SEG6 | 39 | SEG18 | 54 | OSC2 |
| 10 | R03 | 25 | SEG7 | 40 | SEG19 | 55 | $V_{S1}$ |
| 11 | RS | 26 | SEG8 | 41 | COM0 | 56 | P00 |
| 12 | TH1 | 27 | SEG9 | 42 | COM1 | 57 | P01 |
| 13 | TH2 | 28 | SEG10 | 43 | COM2 | 58 | P02 |
| 14 | CS | 29 | SEG11 | 44 | COM3 | 59 | P03 |
| 15 | N.C. | 30 | N.C. | 45 | N.C. | 60 | N.C. |

N.C. : No Connection

## ■ PIN DESCRIPTION

| Pin name | Pin No. | In/Out | Function |
|---|---|---|---|
| $V_{DD}$ | 52 | (I) | Power source (+) terminal |
| $V_{SS}$ | 51 | (I) | Power source (-) terminal |
| $V_{S1}$ | 55 | O | Oscillation and internal logic system regulated voltage output terminal |
| $V_{L1}$ | 48 | O | LCD system regulated voltage output terminal |
| $V_{L2}$ | 47 | O | LCD system booster output terminal |
| $V_{L3}$ | 46 | O | LCD system booster output terminal |
| CA, CB | 49, 50 | – | Booster capacitor connecting terminal |
| OSC1 | 53 | I | Crystal or CR oscillation input terminal |
| OSC2 | 54 | O | Crystal or CR oscillation output terminal |
| K00–K03 | 3–6 | I | Input terminal |
| P00–P03 | 56–59 | I/O | I/O terminal |
| R00–R03 | 7–10 | O | Output terminal |
| SEG0–19 | 18–29<br>33–40 | O | LCD segment output terminal<br>(convertible to DC output terminal by mask option) |
| COM0–3 | 41–44 | O | LCD common output terminal |
| CS | 14 | I | A/D converter CR oscillation input terminal |
| RS | 11 | O | A/D converter CR oscillation output terminal |
| TH1, TH2 | 12, 13 | O | A/D converter CR oscillation output terminal |
| ADOUT | 17 | O | A/D converter oscillation frequency output terminal |
| RESET | 32 | I | Initial setting input terminal |
| TEST | 31 | I | Test input terminal |

## ■ OPTION LIST

1. DEVICE TYPE AND LCD VOLTAGE

☐ 1. E0C6005 (Normal Type <S1C60N05>) LCD 3 V
☐ 2. E0C6005 (Normal Type <S1C60N05>) LCD 4.5 V
☐ 3. E0C60L05 (Low Power Type <S1C60L05>) LCD 3 V
☐ 4. E0C60L05 (Low Power Type <S1C60L05>) LCD 4.5 V

2. MULTIPLE KEY ENTRY RESET

• COMBINATION ..... ☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

3. INTERRUPT NOISE REJECTOR

• K00–K03 ..... ☐ 1. Use ☐ 2. Not Use

4. INPUT PORT PULL DOWN RESISTOR

• K00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
• K01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
• K02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
• K03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

5. R00 SPECIFICATION

• OUTPUT TYPE ..... ☐ 1. DC Output
☐ 2. Buzzer Inverted Output (Control bit is R00)
☐ 3. Buzzer Inverted Output (Control bit is R01)
☐ 4. FOUT Output

• FOUT OUTPUT SPACIFICATION

F1 ..... ☐ 1. 256[Hz] F2 ..... ☐ 1. 1.512[Hz]
☐ 2. 512[Hz] ☐ 2. 1,024[Hz]
☐ 3. 1,024[Hz] ☐ 3. 2,048[Hz]
☐ 4. 2,048[Hz] ☐ 4. 4,096[Hz]
☐ 5. 4,096[Hz] ☐ 5. 8,192[Hz]

F3 ..... ☐ 1. 1,024[Hz] F4 ..... ☐ 1. 2,048[Hz]
☐ 2. 2,048[Hz] ☐ 2. 4,096[Hz]
☐ 3. 4,096[Hz] ☐ 3. 8,192[Hz]
☐ 4. 8,192[Hz] ☐ 4. 16,384[Hz]
☐ 5. 16,384[Hz] ☐ 5. 32,768[Hz]

• OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

6. R01 SPECIFICATION
• OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output
• OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

7. OUTPUT SPECIFICATION (R02, R03)
• R02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
• R03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

8. I/O PORT SPECIFICATION
• P00 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
• P01 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
• P02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
• P03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

9. LCD COMMON DUTY AND BIAS
☐ 1. 1/4 Duty 1/3 Bias
☐ 2. 1/3 Duty 1/3 Bias
☐ 3. 1/2 Duty 1/3 Bias
☐ 4. 1/4 Duty 1/2 Bias
☐ 5. 1/3 Duty 1/2 Bias
☐ 6. 1/2 Duty 1/2 Bias

10.OSC1 SYSTEM CLOCK
☐ 1. Crystal
☐ 2. CR

## ■ ELECTRICAL CHARACTERISTICS

### ● Absolute Maximum Ratings

($V_{DD}$=0V)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power voltage | $V_{SS}$ | -5.0 to 0.5 | V |
| Input voltage (1) | $V_I$ | $V_{SS}$ - 0.3 to 0.5 | V |
| Input voltage (2) | $V_{IOSC}$ | $V_{SS}$ - 0.3 to 0.5 | V |
| Operating temperature | Topr | -20 to 70 | °C |
| Storage temperature | Tstg | -65 to 150 | °C |
| Soldering temperature / Time | Tsol | 260°C, 10sec (lead section) | – |
| Allowable dissipation *1 | $P_D$ | 250 | mW |

*1: In case of plastic package (QFP6-60pin).

### ● Recommended Operating Conditions

**S1C60N05**

(Ta=-20 to 70°C)

| Condition | Symbol | Remark | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power voltage | $V_{SS}$ | $V_{DD}$=0V | -3.5 | -3.0 | -1.8 | V |
| Oscillation frequency | $f_{OSC1}$ | Crystal oscillation | | 32.768 | | kHz |
| | $f_{OSC2}$ | CR oscillation, R=420kΩ | | 65 | 80 | kHz |
| Booster capacitor | $C_1$ | | 0.1 | | | µF |
| Capacitor between $V_{DD}$ and $V_{S1}$ | $C_2$ | | 0.1 | | | µF |

### S1C60L05

(Ta=-20 to 70°C)

| Condition | Symbol | Remark | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power voltage | $V_{SS}$ | $V_{DD}$=0V *1 | -2.0 | -1.5 | -1.2 | V |
| Oscillation frequency | $f_{OSC1}$ | Crystal oscillation | | 32.768 | | kHz |
| | $f_{OSC2}$ | CR oscillation, R=420kΩ | | 65 | 80 | kHz |
| Booster capacitor | $C_1$ | | 0.1 | | | µF |
| Capacitor between $V_{DD}$ and $V_{S1}$ | $C_2$ | | 0.1 | | | µF |

*1: When there is no software control during CR oscillation or crystal oscillation.

## ● DC Characteristics

### S1C60N05

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, $f_{OSC}$=32.768kHz, Ta=25°C, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| High level input voltage (1) | $V_{IH1}$ | | K00–K03, P00–P03 | 0.2•$V_{SS}$ | | 0 | V |
| High level input voltage (2) | $V_{IH2}$ | | RESET, TEST | 0.15•$V_{SS}$ | | 0 | V |
| Low level input voltage (1) | $V_{IL1}$ | | K00–K03, P00–P03 | $V_{SS}$ | | 0.8•$V_{SS}$ | V |
| Low level input voltage (2) | $V_{IL2}$ | | RESET, TEST | $V_{SS}$ | | 0.85•$V_{SS}$ | V |
| High level input current (1) | $I_{IH1}$ | $V_{IH1}$=0V, No pull down resistor | K00–K03, P00–P03 | 0 | | 0.5 | µA |
| High level input current (2) | $I_{IH2}$ | $V_{IH2}$=0V, With pull down resistor | K00–K03 | 10 | | 40 | µA |
| High level input current (3) | $I_{IH3}$ | $V_{IH3}$=0V, With pull down resistor | P00–P03<br>RESET, TEST | 30 | | 100 | µA |
| Low level input current | $I_{IL}$ | $V_{IL}$=$V_{SS}$ | K00–K03, P00–P03<br>RESET, TEST | -0.5 | | 0 | µA |
| High level output current (1) | $I_{OH1}$ | $V_{OH1}$=0.1•$V_{SS}$ | R02, R03, P00–P03 | | | -1.0 | mA |
| High level output current (2) | $I_{OH2}$ | $V_{OH2}$=0.1•$V_{SS}$<br>(built-in protection resistance) | R00, R01 | | | -1.0 | mA |
| High level output current (3) | $I_{OH3}$ | $V_{OH3}$=-1.0V | ADOUT | | | -1.0 | mA |
| Low level output current (1) | $I_{OL1}$ | $V_{OL1}$=0.9•$V_{SS}$ | R02, R03, P00–P03 | 3.0 | | | mA |
| Low level output current (2) | $I_{OL2}$ | $V_{OL2}$=0.9•$V_{SS}$<br>(built-in protection resistance) | R00, R01 | 3.0 | | | mA |
| Low level output current (3) | $I_{OL3}$ | $V_{OL3}$=-2.0V | ADOUT | 3.0 | | | mA |
| Common output current | $I_{OH4}$ | $V_{OH4}$=-0.05V | COM0–COM3 | | | -3 | µA |
| | $I_{OL4}$ | $V_{OL4}$=$V_{L3}$+0.05V | | 3 | | | µA |
| Segment output current | $I_{OH5}$ | $V_{OH5}$=-0.05V | SEG0–SEG19 | | | -3 | µA |
| (during LCD output) | $I_{OL5}$ | $V_{OL5}$=$V_{L3}$+0.05V | | 3 | | | µA |
| Segment output current | $I_{OH6}$ | $V_{OH6}$=0.1•$V_{SS}$ | SEG0–SEG19 | | | -300 | µA |
| (during DC output) | $I_{OL6}$ | $V_{OL6}$=0.9•$V_{SS}$ | | 300 | | | µA |

### S1C60L05

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, $f_{OSC}$=32.768kHz, Ta=25°C, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| High level input voltage (1) | $V_{IH1}$ | | K00–K03, P00–P03 | 0.2•$V_{SS}$ | | 0 | V |
| High level input voltage (2) | $V_{IH2}$ | | RESET, TEST | 0.15•$V_{SS}$ | | 0 | V |
| Low level input voltage (1) | $V_{IL1}$ | | K00–K03, P00–P03 | $V_{SS}$ | | 0.8•$V_{SS}$ | V |
| Low level input voltage (2) | $V_{IL2}$ | | RESET, TEST | $V_{SS}$ | | 0.85•$V_{SS}$ | V |
| High level input current (1) | $I_{IH1}$ | $V_{IH1}$=0V, No pull down resistor | K00–K03, P00–P03 | 0 | | 0.5 | µA |
| High level input current (2) | $I_{IH2}$ | $V_{IH2}$=0V, With pull down resistor | K00–K03 | 5.0 | | 20 | µA |
| High level input current (3) | $I_{IH3}$ | $V_{IH3}$=0V, With pull down resistor | P00–P03<br>RESET, TEST | 9.0 | | 100 | µA |
| Low level input current | $I_{IL}$ | $V_{IL}$=$V_{SS}$ | K00–K03, P00–P03<br>RESET, TEST | -0.5 | | 0 | µA |
| High level output current (1) | $I_{OH1}$ | $V_{OH1}$=0.1•$V_{SS}$ | R02, R03, P00–P03 | | | -200 | µA |
| High level output current (2) | $I_{OH2}$ | $V_{OH2}$=0.1•$V_{SS}$<br>(built-in protection resistance) | R00, R01 | | | -200 | µA |
| High level output current (3) | $I_{OH3}$ | $V_{OH3}$=-0.5V | ADOUT | | | -200 | µA |
| Low level output current (1) | $I_{OL1}$ | $V_{OL1}$=0.9•$V_{SS}$ | R02, R03, P00–P03 | 700 | | | µA |
| Low level output current (2) | $I_{OL2}$ | $V_{OL2}$=0.9•$V_{SS}$<br>(built-in protection resistance) | R00, R01 | 700 | | | µA |
| Low level output current (3) | $I_{OL3}$ | $V_{OL3}$=-1.0V | ADOUT | 700 | | | µA |
| Common output current | $I_{OH4}$ | $V_{OH4}$=-0.05V | COM0–COM3 | | | -3 | µA |
| | $I_{OL4}$ | $V_{OL4}$=$V_{L3}$+0.05V | | 3 | | | µA |
| Segment output current | $I_{OH5}$ | $V_{OH5}$=-0.05V | SEG0–SEG19 | | | -3 | µA |
| (during LCD output) | $I_{OL5}$ | $V_{OL5}$=$V_{L3}$+0.05V | | 3 | | | µA |
| Segment output current | $I_{OH6}$ | $V_{OH6}$=0.1•$V_{SS}$ | SEG0–SEG19 | | | -100 | µA |
| (during DC output) | $I_{OL6}$ | $V_{OL6}$=0.9•$V_{SS}$ | | 130 | | | µA |

## ● Analog Circuit Characteristics and Current Consumption

### S1C60N05 (Normal Operating Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, $f_{OSC}$=32.768kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
<During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | 1/2•$V_{L2}$ -0.1 | | 1/2•$V_{L2}$ ×0.9 | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3/2•$V_{L2}$ -0.1 | | 3/2•$V_{L2}$ ×0.9 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 0.8 | 1.4 | µA |
| | | During execution | | | 1.5 | 5.0 | µA |
| | | During A/D conversion (HALT) | | | 30 | 40 | µA |

### S1C60N05 (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, $f_{OSC}$=32.768kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
<During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | 1/2•$V_{L2}$ -0.1 | | 1/2•$V_{L2}$ ×0.85 | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3/2•$V_{L2}$ -0.1 | | 3/2•$V_{L2}$ ×0.85 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 2.0 | 5.5 | µA |
| | | During execution | | | 5.5 | 10.0 | µA |
| | | During A/D conversion (HALT) | | | 31 | 41.5 | µA |

### S1C60L05 (Normal Operating Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, $f_{OSC}$=32.768kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
<During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | 2•$V_{L1}$ -0.1 | | 2•$V_{L1}$ ×0.9 | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3•$V_{L1}$ -0.1 | | 3•$V_{L1}$ ×0.9 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 0.8 | 1.4 | µA |
| | | During execution | | | 1.5 | 5.0 | µA |
| | | During A/D conversion (HALT) | | | 30 | 40 | µA |

### S1C60L05 (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, $f_{OSC}$=32.768kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
<During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | 2•$V_{L1}$ -0.1 | | 2•$V_{L1}$ ×0.85 | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3•$V_{L1}$ -0.1 | | 3•$V_{L1}$ ×0.85 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 2.0 | 5.5 | µA |
| | | During execution | | | 5.5 | 10.0 | µA |
| | | During A/D conversion (HALT) | | | 31 | 41.5 | µA |

### S1C60N05 (CR, Normal Operating Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, $f_{OSC}$=65kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
Recommended external resistance for CR oscillation=420kΩ <During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | 1/2•$V_{L2}$ -0.1 | | 1/2•$V_{L2}$ ×0.9 | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3/2•$V_{L2}$ -0.1 | | 3/2•$V_{L2}$ ×0.9 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 8.0 | 15.0 | µA |
| | | During execution | | | 15.0 | 20.0 | µA |
| | | During A/D conversion (HALT) | | | 37 | 52.5 | µA |

### S1C60N05 (CR, Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, $f_{OSC}$=65kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
Recommended external resistance for CR oscillation=420kΩ <During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | 1/2•$V_{L2}$ -0.1 | | 1/2•$V_{L2}$ ×0.85 | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3/2•$V_{L2}$ -0.1 | | 3/2•$V_{L2}$ ×0.85 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 16.0 | 30.0 | µA |
| | | During execution | | | 30.0 | 40.0 | µA |
| | | During A/D conversion (HALT) | | | 45 | 57.5 | µA |

### S1C60L05 (CR, Normal Operating Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, $f_{OSC}$=65kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
Recommended external resistance for CR oscillation=420kΩ <During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | 2•$V_{L1}$ -0.1 | | 2•$V_{L1}$ ×0.9 | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3•$V_{L1}$ -0.1 | | 3•$V_{L1}$ ×0.9 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 8.0 | 15.0 | µA |
| | | During execution | | | 15.0 | 20.0 | µA |
| | | During A/D conversion (HALT) | | | 37 | 52.5 | µA |

### S1C60L05 (CR, Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, $f_{OSC}$=65kHz, Ta=25°C, $C_G$=25pF, $V_{S1}$/$V_{L1}$–$V_{L3}$ are internal voltage, $C_1$=$C_2$=0.1µF
Recommended external resistance for CR oscillation=420kΩ <During A/D conversion: $R_S$=49.8kΩ, TH=50kΩ, $C_{AD}$=2,200pF>)

| Characteristic | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Internal voltage | $V_{L1}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load) | | | $V_{SS}$ | | V |
| | $V_{L2}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load) | | 2•$V_{L1}$ -0.1 | | 2•$V_{L1}$ ×0.85 | V |
| | $V_{L3}$ | Connect 1MΩ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load) | | 3•$V_{L1}$ -0.1 | | 3•$V_{L1}$ ×0.85 | V |
| Power current consumption | $I_{OP}$ | During HALT | Without panel load | | 16.0 | 30.0 | µA |
| | | During execution | | | 30.0 | 40.0 | µA |
| | | During A/D conversion (HALT) | | | 45 | 57.5 | µA |

## ● Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, boad pattern). Use the following characteristics are as reference values.

### S1C60N05

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, Crystal: Q13MC146, $C_G$=25pF, $C_D$=built-in, Ta=25°C)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation start voltage | Vsta | tsta≤5sec ($V_{SS}$) | -1.8 | | | V |
| Oscillation stop voltage | Vstp | tstp≤10sec ($V_{SS}$) | -1.8 | | | V |
| Built-in capacitance (drain) | $C_D$ | Including the parasitic capacity inside the IC | | 20 | | pF |
| Frequency/voltage deviation | ∂f/∂V | $V_{SS}$=-1.8 to -3.5V | | | 5 | ppm |
| Frequency/IC deviation | ∂f/∂IC | | -10 | | 10 | ppm |
| Frequency adjustment range | ∂f/∂$C_G$ | $C_G$=5 to 25pF | 40 | | | ppm |
| Harmonic oscillation start voltage | $V_{hho}$ | $C_G$=5pF ($V_{SS}$) | | | -3.6 | V |
| Allowable leak resistance | $R_{leak}$ | Between OSC1 and $V_{DD}$, and between $V_{SS}$ and OSC1 | 200 | | | MΩ |

### S1C60L05

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, Crystal: Q13MC146, $C_G$=25pF, $C_D$=built-in, Ta=25°C)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation start voltage | Vsta | tsta≤5sec ($V_{SS}$) | -1.2 | | | V |
| Oscillation stop voltage | Vstp | tstp≤10sec ($V_{SS}$) | -1.2 | | | V |
| Built-in capacitance (drain) | $C_D$ | Including the parasitic capacity inside the IC | | 20 | | pF |
| Frequency/voltage deviation | ∂f/∂V | $V_{SS}$=-1.2 to -2.0V (-0.9) *1 | | | 5 | ppm |
| Frequency/IC deviation | ∂f/∂IC | | -10 | | 10 | ppm |
| Frequency adjustment range | ∂f/∂$C_G$ | $C_G$=5 to 25pF | 40 | | | ppm |
| Harmonic oscillation start voltage | $V_{hho}$ | $C_G$=5pF ($V_{SS}$) | | | -2.0 | V |
| Allowable leak resistance | $R_{leak}$ | Between OSC1 and $V_{DD}$, and between $V_{SS}$ and OSC1 | 200 | | | MΩ |

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

### S1C60N05 (CR)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-3.0V, $R_{CR}$=480kΩ, Ta=25°C)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency dispersion | $f_{OSC}$ | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | Vsta | | -1.8 | | | V |
| Oscillation start time | tsta | $V_{SS}$=-1.8 to -3.5V | | 3 | | mS |
| Oscillation stop voltage | Vstp | | -1.8 | | | V |

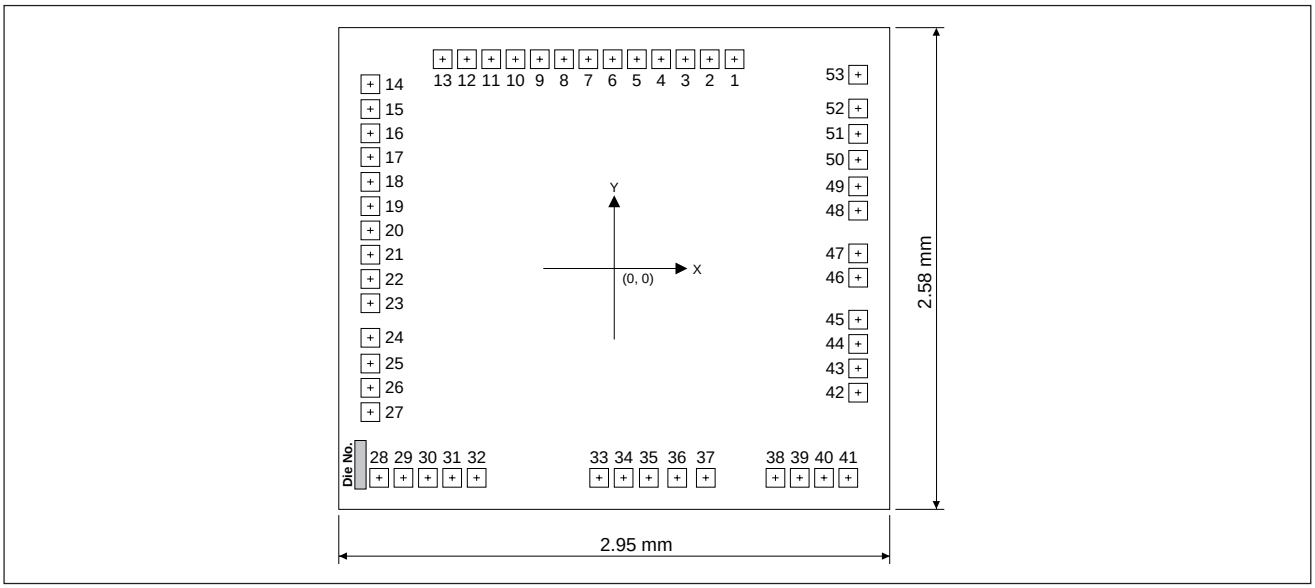
### S1C60L05 (CR)

(Unless otherwise specified: $V_{DD}$=0V, $V_{SS}$=-1.5V, $R_{CR}$=480kΩ, Ta=25°C)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency dispersion | $f_{OSC}$ | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | Vsta | | -1.2 | | | V |
| Oscillation start time | tsta | $V_{SS}$=-1.2 to -2.0V | | 3 | | mS |
| Oscillation stop voltage | Vstp | | -1.2 | | | V |

## ■ PAD LAYOUT

### ● Diagram of Pad Layout



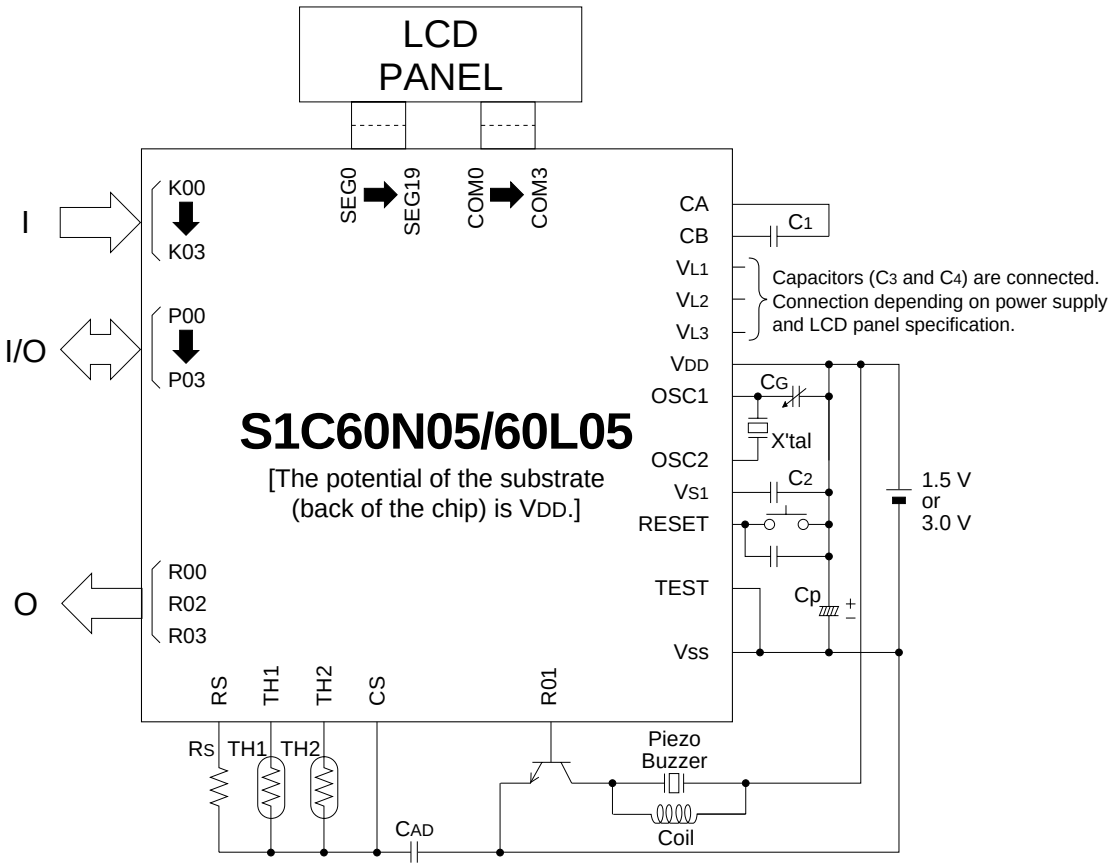

### ● Pad Coordinates

| Pad No. | Pad name | X | Y | Pad No. | Pad name | X | Y |
|---|---|---|---|---|---|---|---|
| 1 | ADOUT | 644 | 1,121 | 28 | $V_{L3}$ | -1,259 | -1,121 |
| 2 | SEG0 | 511 | 1,121 | 29 | $V_{L2}$ | -1,129 | -1,121 |
| 3 | SEG1 | 381 | 1,121 | 30 | $V_{L1}$ | -998 | -1,121 |
| 4 | SEG2 | 251 | 1,121 | 31 | CA | -868 | -1,121 |
| 5 | SEG3 | 121 | 1,121 | 32 | CB | -737 | -1,121 |
| 6 | SEG4 | -9 | 1,121 | 33 | $V_{SS}$ | -81 | -1,121 |
| 7 | SEG5 | -139 | 1,121 | 34 | $V_{DD}$ | 50 | -1,121 |
| 8 | SEG6 | -269 | 1,121 | 35 | OSC1 | 185 | -1,121 |
| 9 | SEG7 | -399 | 1,121 | 36 | OSC2 | 337 | -1,121 |
| 10 | SEG8 | -529 | 1,121 | 37 | $V_{S1}$ | 490 | -1,121 |
| 11 | SEG9 | -659 | 1,121 | 38 | P00 | 863 | -1,121 |
| 12 | SEG10 | -789 | 1,121 | 39 | P01 | 993 | -1,121 |
| 13 | SEG11 | -919 | 1,121 | 40 | P02 | 1,123 | -1,121 |
| 14 | TEST | -1,306 | 987 | 41 | P03 | 1,253 | -1,121 |
| 15 | RESET | -1,306 | 854 | 42 | K00 | 1,306 | -665 |
| 16 | SEG12 | -1,306 | 724 | 43 | K01 | 1,306 | -535 |
| 17 | SEG13 | -1,306 | 597 | 44 | K02 | 1,306 | -404 |
| 18 | SEG14 | -1,306 | 464 | 45 | K03 | 1,306 | -274 |
| 19 | SEG15 | -1,306 | 334 | 46 | R00 | 1,306 | -49 |
| 20 | SEG16 | -1,306 | 204 | 47 | R01 | 1,306 | 81 |
| 21 | SEG17 | -1,306 | 74 | 48 | R02 | 1,306 | 310 |
| 22 | SEG18 | -1,306 | -56 | 49 | R03 | 1,306 | 440 |
| 23 | SEG19 | -1,306 | -186 | 50 | RS | 1,306 | 582 |
| 24 | COM0 | -1,306 | -371 | 51 | TH1 | 1,306 | 721 |
| 25 | COM1 | -1,306 | -509 | 52 | TH2 | 1,306 | 857 |
| 26 | COM2 | -1,306 | -639 | 53 | CS | 1,306 | 1,038 |
| 27 | COM3 | -1,306 | -769 | | | | |

(Unit: μm)

## ■ BASIC EXTERNAL CONNECTION DIAGRAM

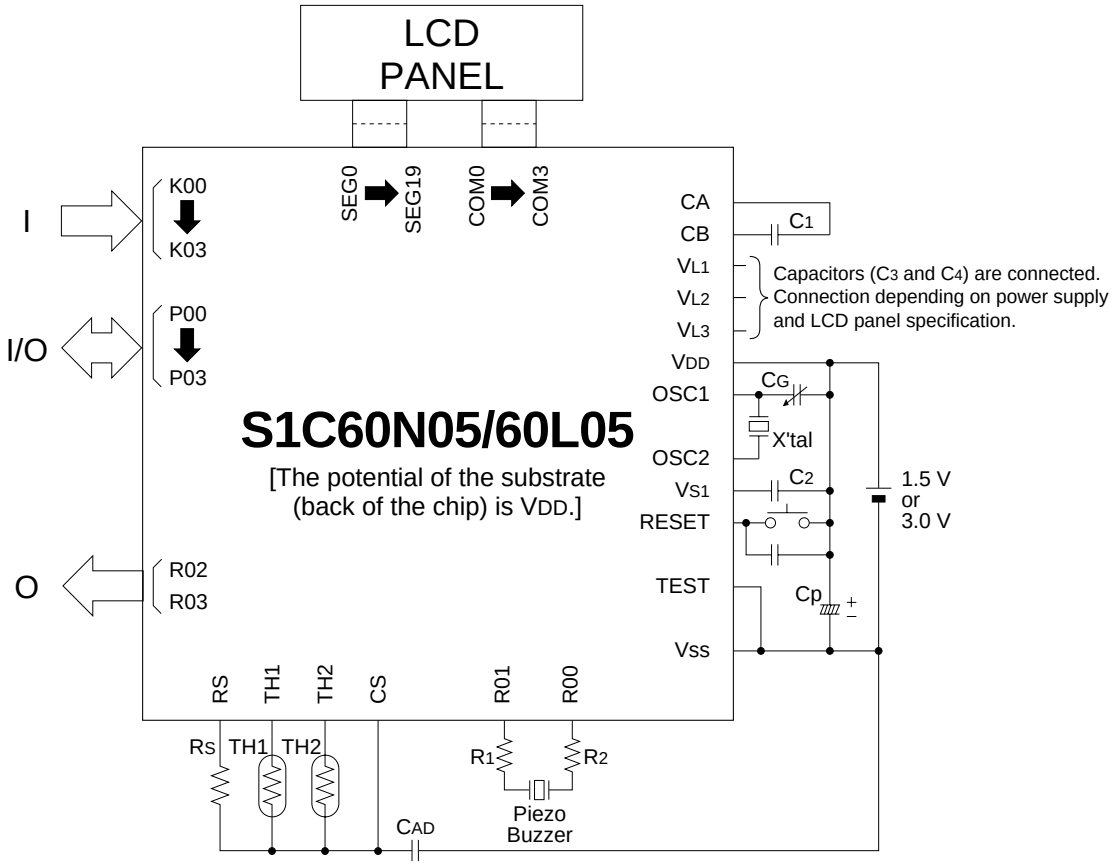
**Piezo Buzzer Single Terminal Driving**




| | | |
|---|---|---|
| X'tal | Crystal oscillator | 32,768 Hz CI(MAX) = 35 kΩ |
| $C_G$ | Trimmer capacitor | 5–25 pF |
| $C_1$, $C_2$, $C_3$, $C_4$ | Capacitor | 0.1 µF |
| Cp | Capacitor | 3.3 µF |
| TH1, TH2 | Thermistor | 50 kΩ |
| $R_S$ | Resistor | 49.8 kΩ |
| $C_{AD}$ | Capacitor | 2,200 pF |

Note: The above table is simply an example, and is not guaranteed to work.

**Piezo Buzzer Direct Driving**

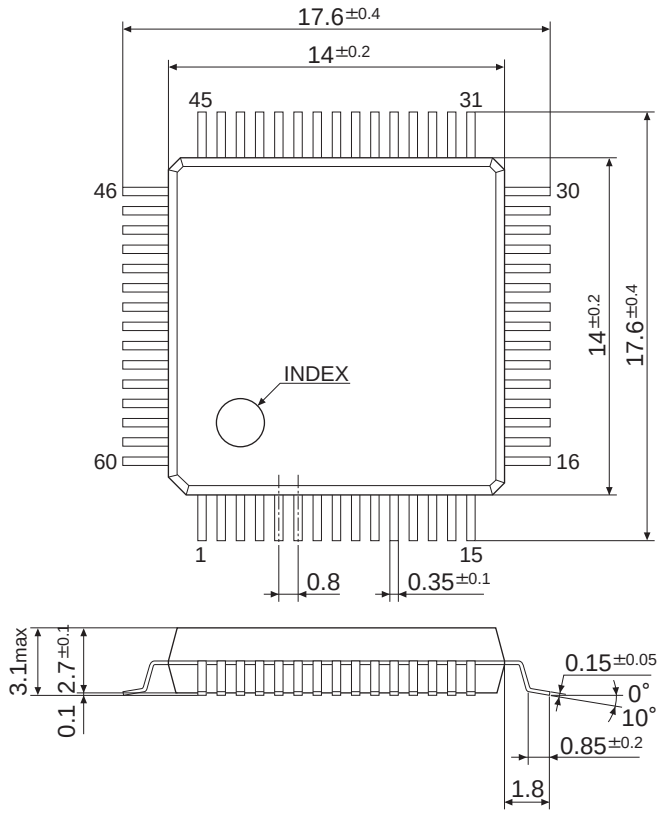



| | | |
|---|---|---|
| X'tal | Crystal oscillator | 32,768 Hz CI(MAX) = 35 kΩ |
| $C_G$ | Trimmer capacitor | 5–25 pF |
| $C_1$, $C_2$, $C_3$, $C_4$ | Capacitor | 0.1 µF |
| Cp | Capacitor | 3.3 µF |
| TH1, TH2 | Thermistor | 50 kΩ |
| $R_S$ | Resistor | 49.8 kΩ |
| $R_1$, $R_2$ | Resistor | 100 Ω |
| $C_{AD}$ | Capacitor | 2,200 pF |

Note: The above table is simply an example, and is not guaranteed to work.

## ■PACKAGE

**Plastic QFP6-60pin**




(Unit: mm)



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