EPSON
EXCEED YOUR VISION

# S1R72U06
# Data Sheet

SEIKO EPSON CORPORATION

Rev. 1.10

## NOTICE

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of Economy, Trade and Industry or other approval from another government agency.

All brands or product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

# Table of Contents

# 1. Overview

The S1R72U06 is a serial (UART/SPI) - USB 2.0 host/device bridge LSI supporting USB 2.0 FS/LS. The main CPU controls the LSI's USB functions using simplified commands. No USB driver is required. The USB classes supported are Mass Storage class (for USB host operation) and Human Interface Device class (for USB host/device operation).

# 2. Features

■ **Ease of use and easy connections (serial connections)**

**Uses simplified commands to control USB functions**

The main CPU controls this LSI's USB functions using simplified commands. No USB driver needs to be installed.

The UART (2-wire asynchronous) or SPI (clock synchronous) serial interface permits the easy connection of various CPU types.

■ **Built-in regulator**

**USB regulator**

**Core voltage regulator**

The S1R72U06 has two regulators: one (input range: 3.3 to 5.0 V) to generate 3.3 V for the USB and another (input voltage: 3.3 to 5.0 V) to generate the internal core voltage of 1.8 V. This allows the S1R72U06 to operate from a single power source as long as the supplied voltage is at least 3.3 V.

■ **Built-in VBUS supply function**

**No external VBUS power SW required**

The S1R72U06 features a built-in VBUS supply function for USB host operations, eliminating the need for the external VBUS power SW previously required by the USB host controller. The S1R72U06 features an interface that controls the external VBUS power SW if the built-in VBUS supply function cannot supply adequate current. If necessary, connect an external VBUS power SW to ensure sufficient current capacity for bus-powered devices.

■ **Product (system) development support function**

**History display**

The S1R72U06 uses a serial interface (asynchronous type) to display the history of internal LSI processing, etc. This function provides useful information during product (system) development.

# 3. Block Diagram

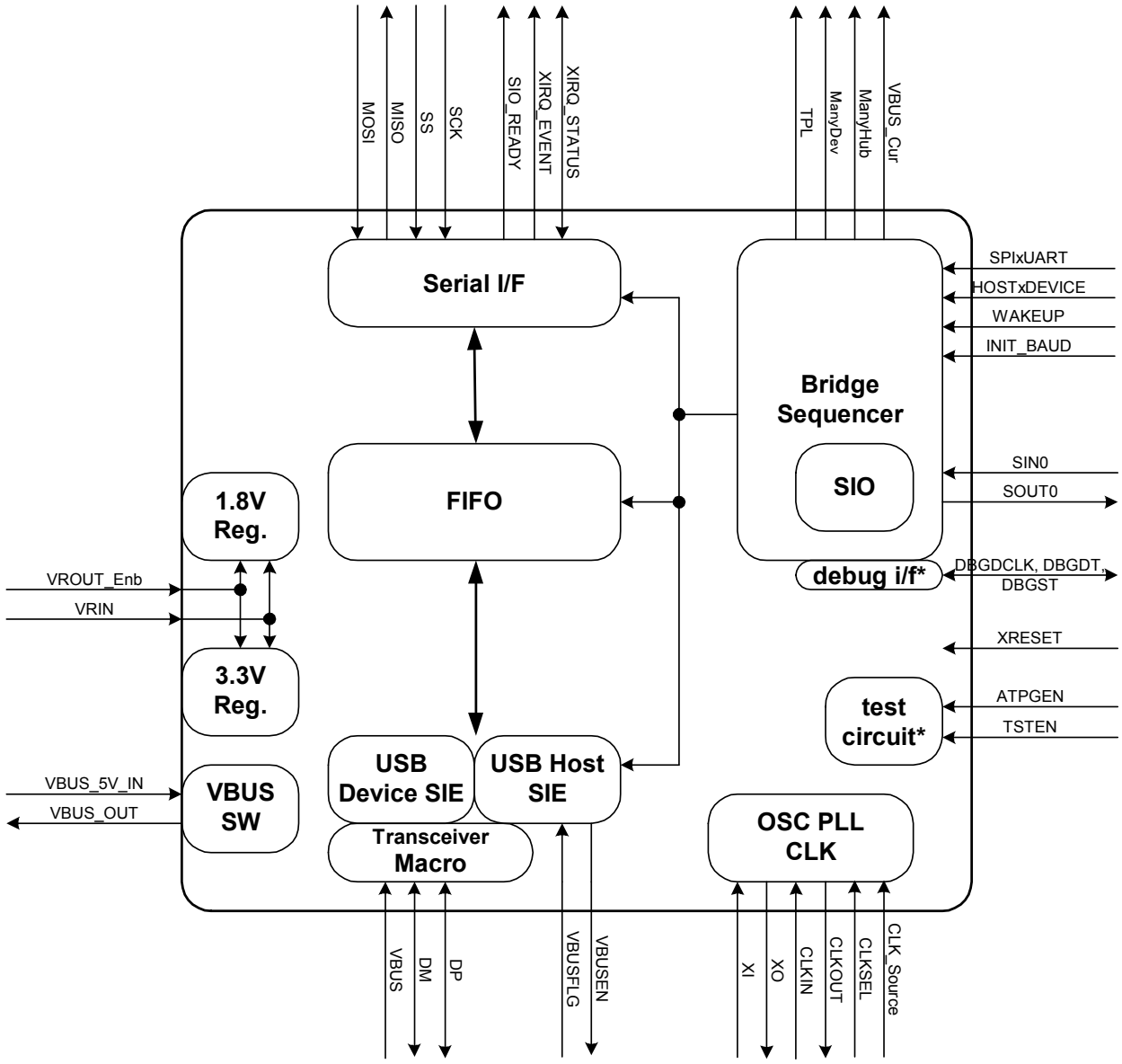



Figure 3.1 Block diagram

# 4. Functions

## 4.1 Serial I/F (UART/SPI)

The S1R72U06 is connected to the main CPU via UART (2-wire asynchronous) or SPI (clock synchronous). When using with UART, set the SPIxUART mode setting pin to Low. When using with SPI, set the SPIxUART mode setting pin to High.

The interface voltage (CVDD) can be used across a broad range, from 1.8 to 5.0 V.

- UART connection (asynchronous serial I/F)

  Initial baud rate: 300/9600 bps (set by mode setting pin INIT_BAUD)

  Baud rate: Settable (max. 3 Mbps)

  lsb first

  8-bit data

  1/2 stop bit

  Odd/Even/No parity

- SPI connection (clock synchronous serial I/F)

  SPI slave

  Mode 0 (Positive pulse latch first)

  Baud rate: Max. 6 Mbps (SCK pin input)

  msb first

  8-bit data

## 4.2 USB Host SIE

The USB host function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard. It supports FS (12 Mbps) and LS (1.5 Mbps) speed modes. The USB functions are controlled by the Bridge Sequencer block inside the LSI. The USB classes supported are the Mass Storage Class and the Human Interface Device Class.

## 4.3 USB Device SIE

The USB device function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard. It supports FS (12 Mbps) and LS (1.5 Mbps) speed modes. The USB function is controlled by the Bridge Sequencer block inside the LSI. The USB class supported is the Human Interface Device Class.

## 4.4 Transceiver Macro

This is a USB analog macro block shared by host and device.

## 4.5 FIFO

This FIFO block serves as a buffer for data between the serial interface and the USB.

## 4.6 Bridge Sequencer

This controls the USB functions based on commands from the serial interface.

## 4.7 SIO

This block is used to display the history of the product (system) development support functions and for analog tests.

## 4.8 Debug I/F

This is a debugging pin for the built-in Bridge Sequencer. It is not intended for use by the user and should be disregarded.

## 4.9 1.8-V Regulator

This regulator generates 1.8-V internal core voltage. The range of input voltages is from 3.3 to 5.0 V.

## 4.10 3.3-V Regulator

This regulator generates 3.3 V for the USB. The range of input voltages is from 3.3 to 5.0 V.

## 4.11 VBUS SW

This is a VBUS output block built into the LSI.

## 4.12 Test Circuit

This is a circuit for IC tests. It is not intended for use by the user and should be disregarded.

# 5. Pin Layout Diagram

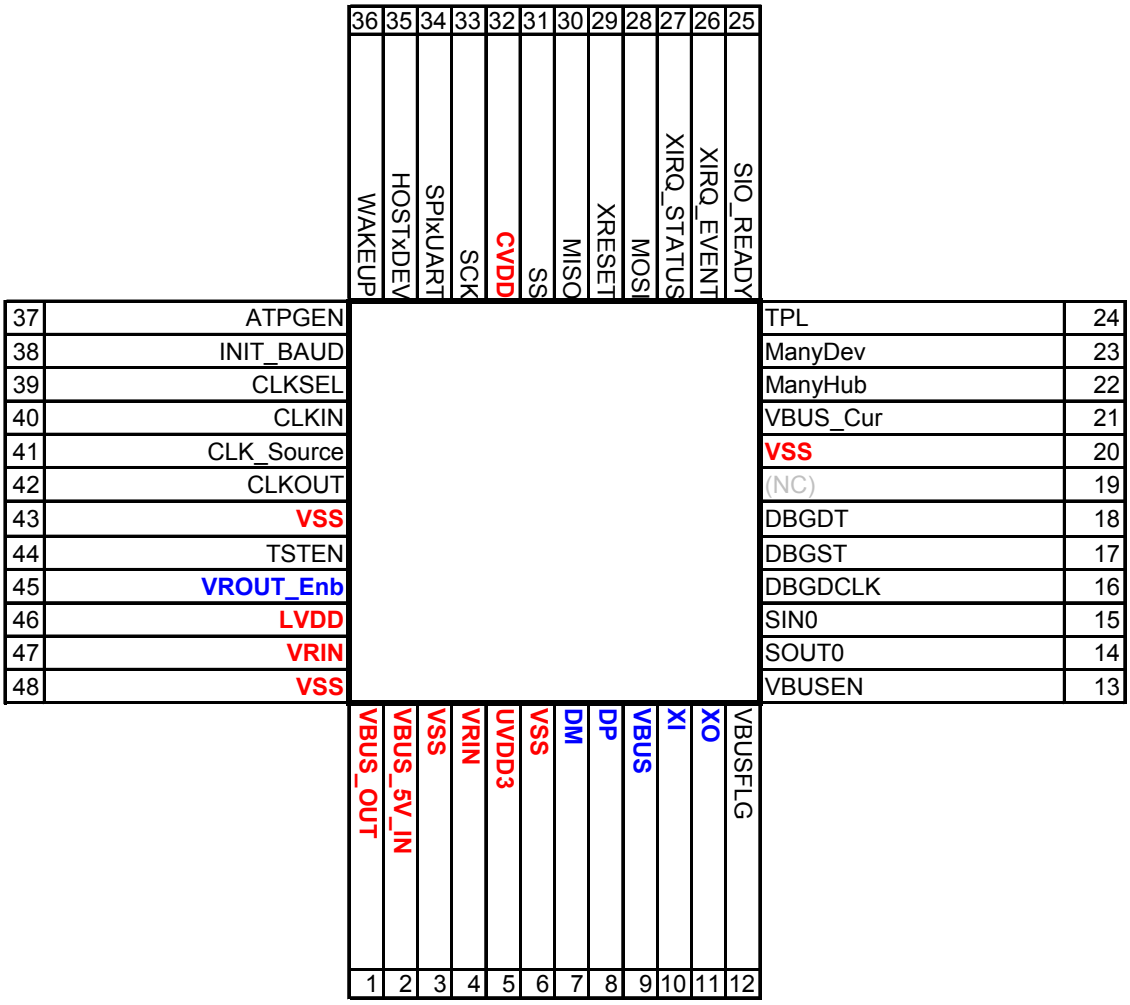



Figure 5.1 Package pin layout diagram (common to QFP and QFN)

# 6. Pin Functions

**GENERAL (CVDD system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 29 | XRESET | IN | - | Reset signal |
| - | 39 | CLKSEL | IN | - | Clock frequency selection<br>Set the frequency input from the clock source (CLKIN or XI pin).<br>1: 24 MHz 0: 12 MHz |
| - | 41 | CLK_Source | IN | - | Clock source selection<br>Set whether the clock source is input from the CLKIN or XI pin.<br>1: CLKIN 0: XI |
| - | 40 | CLKIN | IN | - | Clock input<br>12 MHz / 24MHz<br>If the clock input is from the XI pin, set this pin to Low. |
| - | 42 | CLKOUT | OUT | Low | Clock output<br>Refer to the *S1R72U06 Technical Manual* for information on how to change the clock output.<br>48 MHz / 24 MHz / 12 MHz / 6 MHz / 3 MHz / STOP |

**OSC (LVDD system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 10 | XI | IN | - | Internal oscillator circuit input<br>If the clock input is from the CLKIN pin, set this pin to Low.<br>12 MHz / 24 MHz |
| - | 11 | XO | OUT | - | Internal oscillator circuit output<br>If the clock input is from the CLKIN pin, leave this pin open. |

**TEST (LVDD, CVDD systems)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 44 | TSTEN | IN(PD) | - | Test pin (*1); not intended for use by user |
| - | 37 | ATPGEN | IN(PD) | - | Test pin (*1); not intended for use by user |

PD: Pull-down I/Os are used.

*1 This is pulled down inside the LSI. However, we recommend fixing it at Low on the circuit board.

**USB (UVDD3 system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 9 | VBUS | IN | - | VBUS input pin<br>VBUS input pin when S1R72U06 is used as USB device. Leave this pin open when using S1R72U06 as a USB host. |
| - | 8 | DP | BI | Hi-Z | USB data line Data+ |
| - | 7 | DM | BI | Hi-Z | USB data line Data- |

**VBUS (UVDD3 system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 12 | VBUSFLG | IN(PU) | - | USB power switch fault detection signal<br>1: Normal, 0: Error<br>CMOS Schmitt input<br>Use when external USB power switch is added.<br>Leave open when not used. |
| - | 13 | VBUSEN | OUT | Low | USB power switch control signal<br>Use when external USB power switch is added.<br>Leave open when not used. |

PU: Pull-up I/Os are used.

**Serial I/F (CVDD system): Main CPU**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 30 | MISO | Tri | High | Serial data output<br>(Hi-z is output when the SS pin is set to High even when using in UART mode.) |
| - | 28 | MOSI | IN | - | Serial data input |
| - | 31 | SS | IN | - | Slave selection<br>In SPI mode<br>(Can be used to control output from the MISO pin even when using in UART mode. If Hi-z output is not required, fix this pin at Low.) |
| - | 33 | SCK | IN | - | Serial clock<br>In SPI mode<br>(Fix at low when using in UART mode.) |
| - | 25 | SIO_READY | OUT | Low | Communication ready notification pin<br>Refer to the *S1R72U06 Technical Manual* for detailed instructions on using this pin. Leave open when not used. |
| - | 27 | XIRQ_STATUS | OUT | High | Status notification<br>Refer to the *S1R72U06 Technical Manual* for detailed instructions on using this pin. Leave open when not used. |
| - | 26 | XIRQ_EVENT | OUT | High | Event read request<br>Refer to the *S1R72U06 Technical Manual* for detailed instructions on using this pin. Leave open when not used. |

**Serial I/F (UVDD3 system): History Display**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 15 | SIN0 | IN | - | Asynchronous serial data IN<br>Serial data IN pin for history display. Refer to the *S1R72U06 Development Support Manual* for specifics of history display. Fix at High when not used. |
| - | 14 | SOUT0 | OUT | High | Asynchronous serial data OUT<br>Serial data OUT pin for history display. Refer to the *S1R72U06 Development Support Manual* for specifics of history display. Leave open when not used. |

**DEBUG I/F (UVDD3 system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 16 | DBGDCLK | OUT | High | Not used (*1) |
| - | 18 | DBGDT | BI(PU) | - | Not used (*2) |
| - | 17 | DBGST | OUT | Low | Not used (*1) |

PU: Pull-up I/Os are used.

*1 Leave open.

*2 This is pulled up in the LSI. However, an external pull-up of about 10 kΩ is recommended.

**GPI (CVDD system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 34 | SPIxUART | IN | - | Setting pin<br>0: UART mode<br>1: SPI mode |
| - | 35 | HOSTxDEVICE | IN | - | Setting pin<br>1: HOST mode, 0: DEVICE mode<br>Switching modes resets the LSI. |
| - | 36 | WAKEUP | IN | - | Wake-up pin<br>Used to resume from SLEEP state.<br>Rising edge activates the wake-up trigger. |
| - | 38 | INIT_BAUD | IN | - | Initial baud rate setting pin<br>1: 9600bps 0: 300bps<br>UART baud rate can be set to between 300 bps and 3 Mbps using the serial port setting. Refer to the *S1R72U06 Technical Manual* for detailed instructions on making serial port settings. |

**GPO (CVDD system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 24 | TPL | OUT | Low | Unsupported Device<br>1: Error, 0: -<br>Used for USB Compliance Testing. Leave open when not used. |
| - | 23 | ManyDev | OUT | Low | Too Many Devices<br>1: Error, 0: -<br>Used for USB Compliance Testing. Leave open when not used. |
| - | 22 | ManyHub | OUT | Low | Too Many Hubs<br>1: Error, 0: -<br>Used for USB Compliance Testing. Leave open when not used. |
| - | 21 | VBUS_Cur | OUT | Low | VBUS Over Current<br>1: Error, 0: -<br>Used for USB Compliance Testing. Leave open when not used. |

**Regulator (VRIN system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 4, 47 | VRIN | Power | - | Regulator input<br>Connect Cin = 1.0 μF to each pin.<br>Make sure to keep this open when not using the regulator. |
| - | 45 | VROUT_Enb | IN | - | Enables the regulator<br>Set this to the same level as VRIN when using the regulator.<br>Make sure to set this to Low when not using the regulator. |

**VBUS SW (VBUS_5V_IN system)**

| BGA | QFP | Name | I/O | RESET | Pin description |
|---|---|---|---|---|---|
| - | 2 | VBUS_5V_IN | Power | - | VBUS generation input<br>Voltage input pin for built-in VBUS supply function.<br>The power supply (VSWIN in 8.3.5) should be provided even when this function is not used. |
| - | 1 | VBUS_OUT | Power | - | VBUS output<br>VBUS output pin for built-in VBUS supply function.<br>Leave open when this function will not be used. |

**POWER**

| BGA | QFP | Name | Voltage | Pin description |
|---|---|---|---|---|
| - | 5 | UVDD3 | 3.3V | Power supply for USB<br>When using regulator: Connect Cout = 1.0 μF.<br>When not using regulator: Apply the voltage indicated to the left. |
| - | 46 | LVDD | 1.8V | Internal power supply, test power supply, OSC power supply<br>When using regulator: Connect Cout = 1.0 μF.<br>When not using regulator: Apply the voltage indicated to the left. |
| - | 32 | CVDD | 1.8 to 5.0V | Power supply for main CPU I/F |
| - | 3, 6, 20, 43, 48 | VSS | 0V | GND |

# 7. Commands

Communication with the main CPU is implemented via commands. For detailed information on commands, refer to the *S1R72U06 UART Interface Manual* and the *S1R72U06 SPI Interface Manual*.

# 8. Electrical Characteristics

## 8.1 Absolute Maximum Ratings

| Item | Code | Rating | Unit |
|---|---|---|---|
| Power supply voltage | CVDD<br>VRIN (*1) | -0.3 to 7.0 | V |
| | UVDD3 | -0.3 to 4.0 | V |
| | LVDD (*2) | -0.3 to 2.5 | V |
| Input voltage | VI (*3) | -0.3 to CVDD+0.5<br>-0.3 to UVDD3+0.5<br>-0.3 to LVDD+0.5 | V |
| | VBUS_5V_IN | -0.3 to 7.0 | V |
| Output voltage | VO (*3) | -0.3 to CVDD+0.5<br>-0.3 to UVDD3+0.5<br>-0.3 to LVDD+0.5 | V |
| | VBUS_OUT | VBUS_5V_IN+0.3 | V |
| Output current/pin | Iout | ±10 | mA |
| Storage temperature | Tstg | -65 to 150 | °C |

*1 VRIN≥UVDD3, VRIN≥LVDD

*2 CVDD, UVDD3≥LVDD

*3 Power supply voltages

## 8.2 Recommended Operating Conditions

| Item | Code | Min. | Typ. | Max. | Uni |
|---|---|---|---|---|---|
| Power supply voltage | CVDD | 1.65 | 1.80 to 5.00 | 5.50 | V |
| | VRIN | 3.00 | 3.30 to 5.00 | 5.50 | V |
| | UVDD3 | 3.00 | 3.30 | 3.60 | V |
| | LVDD | 1.65 | 1.80 | 1.95 | V |
| Input voltage | VI (*) | -0.3 | - | CVDD+0.3<br>UVDD3+0.3<br>LVDD+0.3 | V |
| Ambient temperature | $T_a$ | -40 | 25 | 85 | °C |

* Power supply voltages for each pin

**[Precautions for power ON sequence]**

Be careful of the power supply timing when providing an external power supply without using a built-in regulator. Refer to “8.4.1 Power supply input/cutoff timing” for more information.

## 8.3 DC Characteristics

### 8.3.1 Current consumption

| Item | | Code | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply current (*1) | | | | | | | |
| | Power supply current | IDDH0 | CVDD = 5.5V | - | 5 | - | mA |
| | | IDDH1 | UVDD3 = 3.6V | - | 5 *2 | - | mA |
| | | IDDL | LVDD = 1.95V | - | 25 *2 | - | mA |
| | | IDDR | VRIN = 5.5V | - | 30 *3 | - | mA |
| Power supply current (Static current) (*4) | | | | | | | |
| | Power supply current | IDDS | Max. condition of each power supply Fixed to power supply or GND | - | 50 | - | μA |
| Input leak | | | | | | | |
| | Input leakage current | IL | Max. condition of each power supply | -5 | - | 5 | μA |

*1 At recommended operating conditions (Ta = 25°C). Operating current for Seiko Epson evaluation board configuration.

*2 Operating current for Seiko Epson evaluation board configuration with external power supply and no built-in regulator.

*3 Operating current for Seiko Epson evaluation board configuration with built-in regulator.

*4 Static current when Ta = 25°C and when using regulator.

### 8.3.2 Input characteristics

| Item | Code | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input characteristics | Pin: | LVDD-system pin | | | | |
| "H" level input voltage | VIH1 | LVDD = 1.95V | 1.27 | - | - | V |
| "L" level input voltage | VIL1 | LVDD = 1.65V | - | - | 0.57 | V |
| Input characteristics (Schmitt) | Pin: | CVDD- and UVDD3-system pin | | | | |
| "H" level trigger voltage | VT1+ | CVDD = 5.5V<br>CVDD = 3.6V<br>CVDD = 1.95V<br>UVDD3 = 3.6V | - | - | 4.00<br>2.52<br>1.36<br>2.52 | V |
| "L" level trigger voltage | VT1- | CVDD = 4.5V<br>CVDD = 3.0V<br>CVDD = 1.65V<br>UVDD3 = 3.0V | 0.80<br>0.75<br>0.42<br>0.75 | - | - | V |
| Hysteresis voltage | ΔV1 | CVDD = 4.5V<br>CVDD = 3.0V<br>CVDD = 1.65V<br>UVDD3 = 3.0V | 0.30<br>0.30<br>0.17<br>0.30 | - | - | V |
| Schmitt input characteristics (USB: FS) | Pin: | DP, DM | | | | |
| "H" level trigger voltage | VTU+ | UVDD3 = 3.6V | - | - | 2.0 | V |
| "L" level trigger voltage | VTU- | UVDD3 = 3.0V | 0.8 | - | - | V |
| Input characteristics (USB: FS differential input) | Pin: | DP, DM pair | | | | |
| Differential input sensitivity | VDSU | UVDD3 = 3.0V<br>Differential input voltage: 0.8 to 2.5 V | 0.2 | - | - | V |
| Input characteristics | Pin: | VBUSFLG, DBGDT | | | | |
| Pull-up resistance | RPLU | VI = 0V (UVDD3 = 3.0V) | 52 | 160 | 384 | kΩ |
| Input characteristics | Pin: | ATPGEN | | | | |
| Pull-down resistance | RPLD | VI = CVDD（CVDD = 4.5V）<br>VI = CVDD（CVDD = 3.0V）<br>VI = CVDD（CVDD = 1.65V） | 32<br>52<br>200 | 100<br>160<br>600 | 240<br>384<br>1440 | kΩ |
| Input characteristics | Pin: | TSTEN | | | | |
| Pull-down resistance | RPLDL | VI = LVDD (LVDD = 1.65V) | 40 | 120 | 288 | kΩ |
| Input characteristics | Pin name: | VBUS | | | | |
| Pull-down resistance | RPLDB | VI = 5.0V | 100 | 125 | 165 | kΩ |

### 8.3.3 Output characteristics

($V_{SS}$=0V)

| Item | Code | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output characteristics | Pin: | SIO_READY, XIRQ_EVENT, XIRQ_STATUS, TPL, ManyDev, ManyHUB, VBUS_Cur, VBUSEN | | | | |
| "H" level output voltage | VOH1 | CVDD = 4.5V (IOH = -2.0mA)<br>CVDD = 3.0V (IOH = -1.4mA)<br>CVDD = 1.65V (IOH = -0.6mA)<br>UVDD3 = 3.0V (IOH = -1.4mA) | CVDD – 0.4<br>CVDD – 0.4<br>CVDD – 0.4<br>UVDD3 – 0.4 | - | - | V |
| "L" level output voltage | VOL1 | CVDD = 4.5V (IOH = 2.0mA)<br>CVDD = 3.0V (IOH = 1.4mA)<br>CVDD = 1.65V (IOH = 0.6mA)<br>UVDD3 = 3.0V (IOH = 1.4mA) | - | - | 0.4<br>0.4<br>0.4<br>0.4 | V |
| Output characteristics | Pin: | MISO, SOUT0, CLKOUT | | | | |
| "H" level output voltage | VOH2 | CVDD = 4.5V (IOH = -4.0mA)<br>CVDD = 3.0V (IOH = -2.8mA)<br>CVDD = 1.65V (IOH = -1.2mA)<br>UVDD3 = 3.0V (IOH = -2.8mA) | CVDD – 0.4<br>CVDD – 0.4<br>CVDD – 0.4<br>UVDD3 – 0.4 | - | - | V |
| "L" level output voltage | VOL2 | CVDD = 4.5V (IOH = 4.0mA)<br>CVDD = 3.0V (IOH = 2.8mA)<br>CVDD = 1.65V (IOH = 1.2mA)<br>UVDD3 = 3.0V (IOH = 2.8mA) | - | - | 0.4<br>0.4<br>0.4<br>0.4 | V |
| Output characteristics (USB: FS) | Pin: | DP, DM | | | | |
| "H" level output voltage | VOHUF | UVDD3 = 3.0V | 2.8 | - | - | V |
| "L" level output voltage | VOLUF | UVDD3 = 3.6V | - | - | 0.3 | V |
| Output characteristics | Pin: | CVDD-system pin | | | | |
| OFF-STATE leakage current | IOZ | CVDD = 5.5V<br>VOH = CVDD<br>VOL = VSS | -5 | - | 5 | μA |

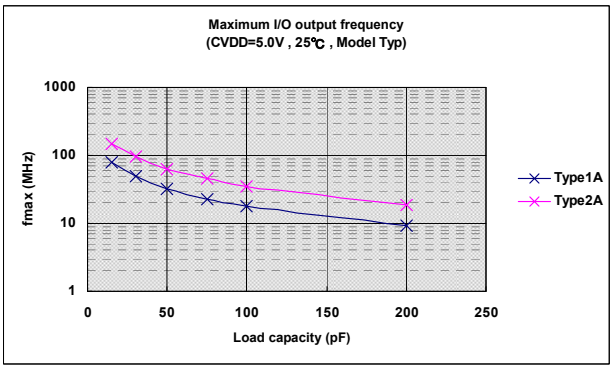
○ Fmax-Cl

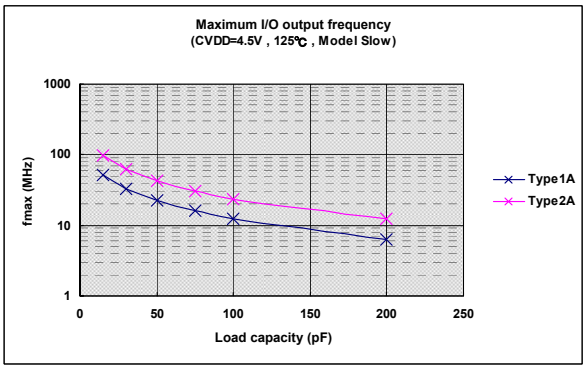
<Output buffer types>

Type1A: SIO_READY, XIRQ_EVENT, XIRQ_STATUS, TPL, ManyDev, ManyHUB, VBUS_Cur, VBUSEN

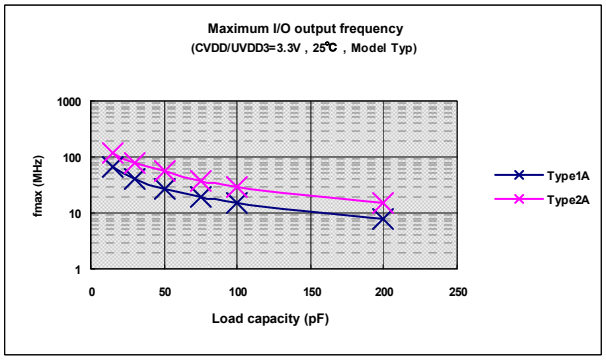
Type2A: MISO, SOUT0, CLKOUT

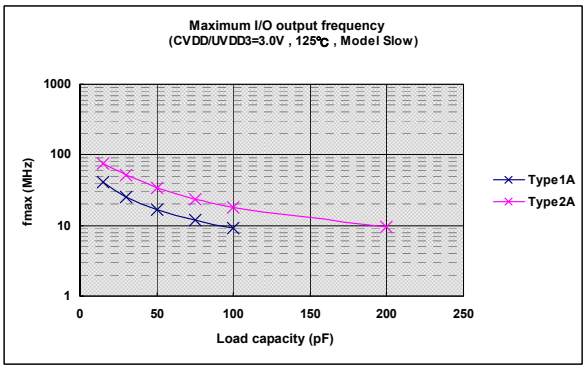
■ Using 5.0 V IO voltage



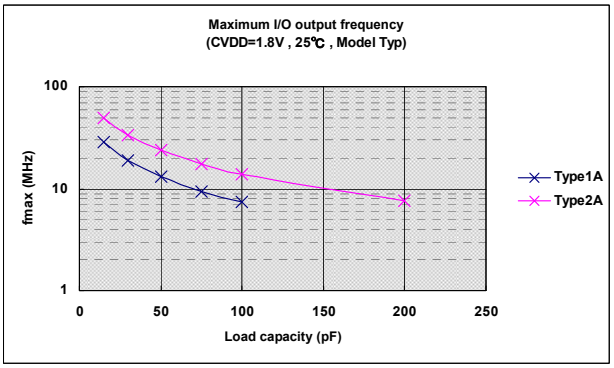



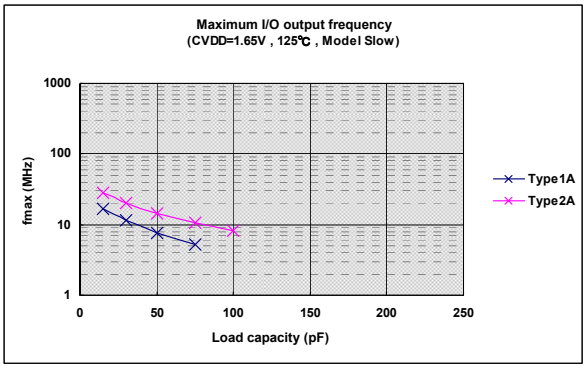

■ Using 3.3 V IO voltage




■ Using 1.8 V IO voltage



### 8.3.4 Pin capacitance

| Item | | Code | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Pin capacitance | | Pin name: | All input pins | | | | |
| | Input pin capacitance | CI | f = 1MHz | - | - | 8 | pF |
| Pin capacitance | | Pin name: | All output pins | | | | |
| | Output pin capacitance | CO | f = 1MHz | - | - | 8 | pF |
| Pin capacitance | | Pin name: | All output pins except DP and DM | | | | |
| | Input/output pin capacitance | CB | f = 1MHz | - | - | 8 | pF |
| Pin capacitance | | Pin name: | DP, DM | | | | |
| | Input/output pin capacitance (USB) | CBU | f = 1MHz | - | - | 15 | pF |

### 8.3.5 VBUS supply function characteristics

| Item | Code | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input voltage | VSWIN | | 3.0 | 5.0 | 5.5 | V |
| On resistance | RSWON | VBUS_5V_IN = 5.0V<br>VBUS_5V_IN = 3.0V | - | 2.4<br>3.5 | 4.0<br>- | Ω |
| Off leakage current | ISWOFF | VBUS_5V_IN = 5.0V<br>VBUS_5V_IN = 3.0V | - | 10<br>10 | 100<br>100 | nA |
| Overcurrent detection | ISWLMT | VBUS_5V_IN = 5.0V<br>VBUS_5V_IN = 3.0V | 21<br>- | 26<br>17 | 35<br>- | mA |
| Overcurrent response time | TSWOFF | Overcurrent → VBUS Off | 300 | | | μs |

### 8.3.6 Fail-safe cell

The S1R72U06 uses fail-safe cells for certain pins. Fail-safe cells have the following advantages:

- They prevent input leakage currents when a power supply is applied to input pins or input/output pins in the input state, even if the signal input exceeds the power supply voltage. (Note that a leakage current of approximately 30 μA will occur for pins with pull-up resistance.)
- No input leakage current occurs when the power supply is cut off, even when an external input signal is applied.

Note that while signals with a voltage level exceeding the operating voltage can be received, the signal voltage that can be applied to the fail-safe cell cannot exceed the absolute maximum rating.

<Fail-safe fitted pins>

MISO, MOSI, SCK, SS, SIO_READY, XIRQ_EVENT, XIRQ_STATUS, SPIxUART, HOSTxDEVICE, WAKEUP, INIT_BAUD, TPL, ManyDev, ManyHUB, VBUS_Cur, SIN0, SOUT0, VBUSFLG, VBUSEN, CLKOUT, CLKIN, CLK_Source, CLKSEL, DBGDCLK, DBGDT, DBGST, XRESET, ATPGEN

## 8.4 AC Characteristics

### 8.4.1 Power supply input/cutoff timing

**A. Power supply input/cutoff timing (for LVDD⇒HVDD / HVDD⇒LVDD: recommended conditions)**

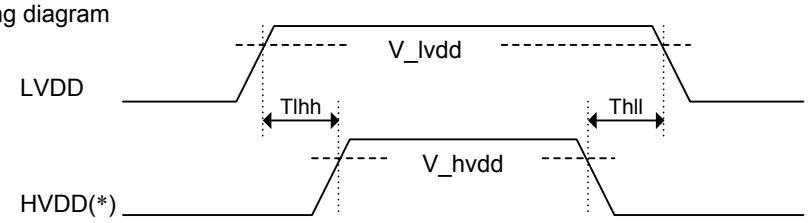
Timing parameters

| Item | Code | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| HVDD power supply input timing | Tlhh | 0 | - | 10 | sec |
| HVDD cutoff timing | Thll | 0 | - | 10 | sec |

Voltage parameters

| Item | Code | Voltage conditions | | Unit |
|---|---|---|---|---|
| | | Input | Cutoff | |
| LVDD initial voltage | V_lvdd | LVDD_min | LVDD_min | V |
| HVDD initial voltage | V_hvdd | HVDD_min | HVDD_min | V |

Timing diagram




**B. Power supply input/cutoff timing (for HVDD LVDD / LVDD⇒HVDD)**

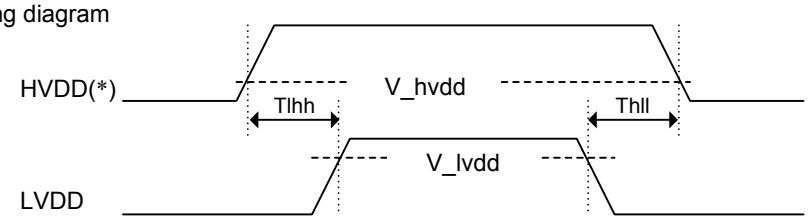
Timing parameters

| Item | Code | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| LVDD power supply input timing | Tlhh | 0 | - | 1 | sec |
| LVDD cutoff timing | Thll | 0 | - | 1 | sec |

Voltage parameters

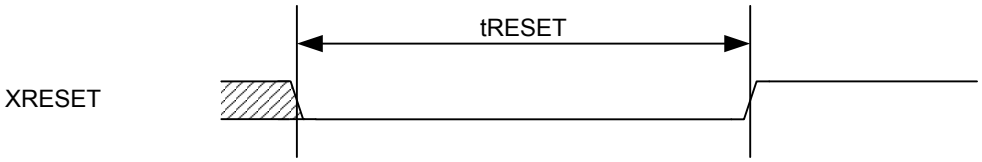
| Item | Code | Voltage conditions | | Unit |
|---|---|---|---|---|
| | | Input | Cutoff | |
| LVDD initial voltage | V_lvdd | LVDD_min | LVDD_min | V |
| HVDD initial voltage | V_hvdd | 0.1 | 0.1 | V |

Timing diagram



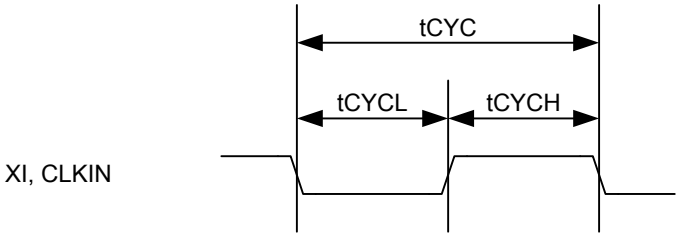

* HVDD refers to USB UVDD3 or interface CVDD.
* For LVDD⇒HVDD timing, refer to A for input and B for cutoff.
  For HVDD⇒LVDD timing, refer to B for input and A for cutoff.

### 8.4.2 Reset timing




| Code | Description | min | typ | max | Unit |
|---|---|---|---|---|---|
| tRESET | Reset pulse width | 40 | - | - | ns |

### 8.4.3 Clock timing




| Code | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tCYC | Clock cycle (CLKSEL = "L") | - | 12.000 | - | MHz |
| tCYC | Clock cycle (CLKSEL = "H") | - | 24.000 | - | MHz |
| tCYCL<br>tCYCH | Clock duty | 45 | 50 | 55 | % |

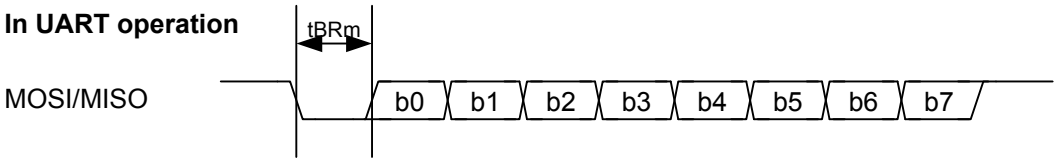
* The clock source selected must satisfy the accuracy requirements under USB standards. FS: 2,500 ppm, LS: 15,000 ppm

### 8.4.4 USB I/F timing

Complies with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard.

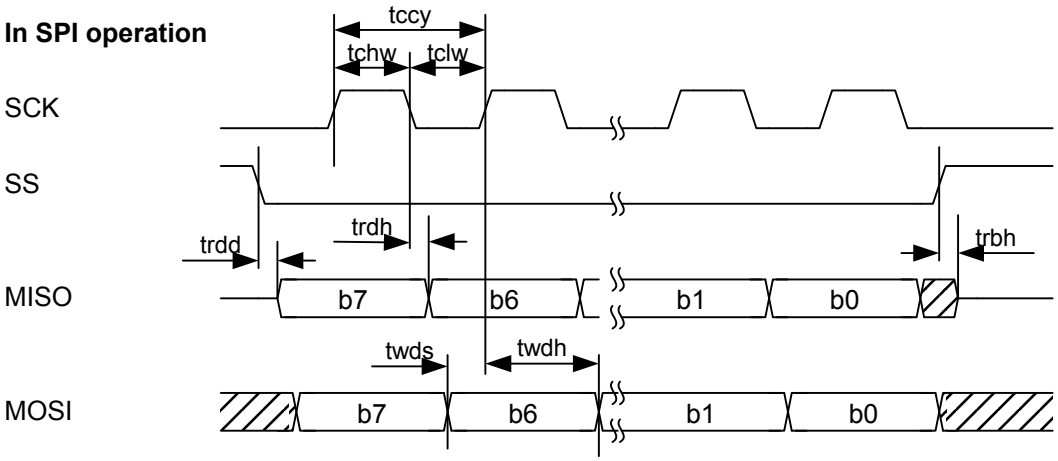
### 8.4.5 Serial I/F (main CPU) timing

**In UART operation**



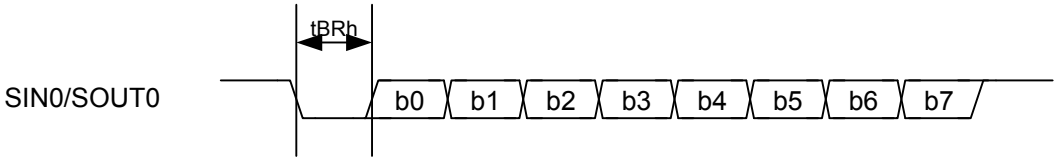

| Code | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tBRm | Baud rate | 300 | - | 3M | bps |

**In SPI operation**




| Code | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tccy | Clock cycle | - | - | 6M | Hz |
| tchw | Clock High width | 50 | - | - | ns |
| tclw | Clock Low width | 50 | - | - | ns |
| trdd | Data output start delay | 2 | - | 20 | ns |
| trdh | Data output switchover delay | - | - | 35 | ns |
| trbh | Data output hold | - | - | 20 | ns |
| twds | Received data setup | 10 | - | - | ns |
| twdh | Received data hold | 5 | - | - | ns |

### 8.4.6 Serial I/F (history display) timing



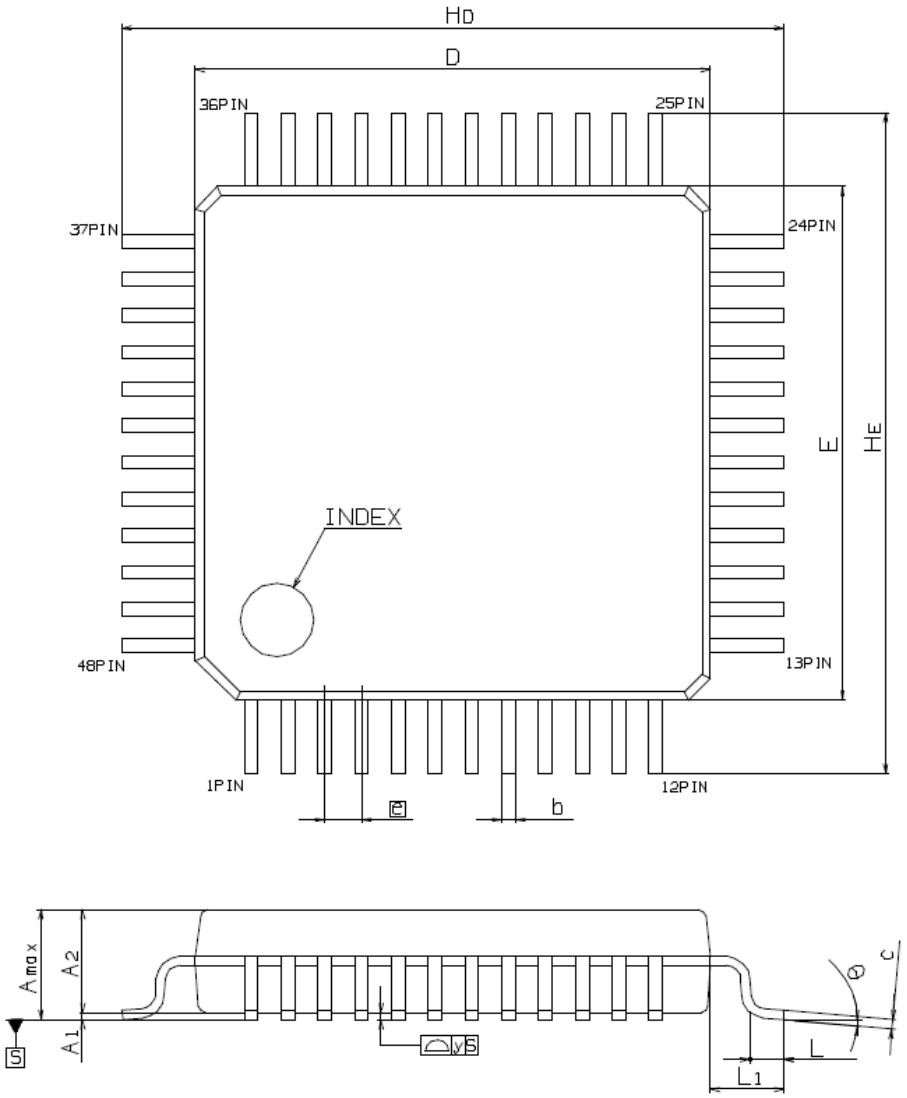

| Code | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tBRh | Baud rate | - | 38400 | - | bps |

# 9. Connection Examples

Refer to the *S1R72U06 Evaluation Board Manual*.

# 10. External Dimensions Diagrams

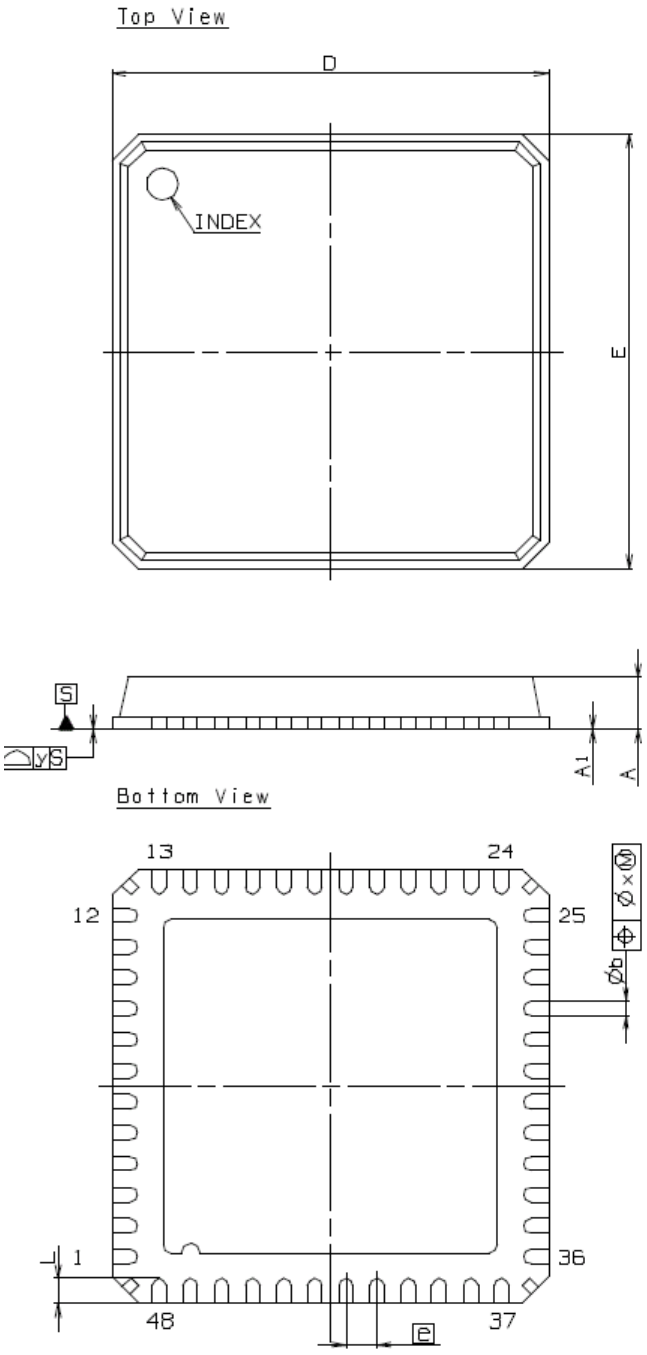
## 10.1 QFP12-48




| Symbol | Dimension in Millimters | | |
|---|---|---|---|
| | Min | Nom | Max |
| E | - | 7 | - |
| D | - | 7 | - |
| $A_{max}$ | - | - | 1.7 |
| $A_1$ | - | 0.1 | - |
| $A_2$ | - | 1.4 | - |
| e | - | 0.5 | - |
| b | 0.13 | - | 0.27 |
| c | 0.09 | - | 0.2 |
| θ | 0° | - | 10° |
| L | 0.3 | - | 0.7 |
| $L_1$ | - | 1 | - |
| $H_E$ | - | 9 | - |
| $H_D$ | - | 9 | - |
| y | - | - | 0.08 |

1 = 1mm

## 10.2 QFN7-48




| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | - | 7 | - |
| E | - | 7 | - |
| A | - | - | 1 |
| A1 | 0 | - | - |
| b | 0.17 | - | 0.3 |
| e | - | 0.5 | - |
| L | 0.3 | - | 0.5 |
| x | - | - | 0 1 |
| y | - | - | 0 08 |

1 = 1mm

# 11. Product Codes

| Product code | Description |
|---|---|
| S1R72U06F12E100 | QFP12-48 package |
| S1R72U06F07E100 | QFN7-48 package |

# Revision History

Attachment-1

| Rev. No. | Date | Page | Category | Contents |
|---|---|---|---|---|
| Rev.1.00 | 06/05/2009 | All pages | New | Newly established |
| Rev.1.10 | 09/07/2009 | P8 | Amend | Amend I/O and processing method when function is not used<br>Before : IN(PU) Leave Open<br>After : IN Fix at High |
| | | P14 | Remove | Remove SIN0 Pin from the object of RPLU |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

EPSON

# International Sales Operations

## AMERICA

**EPSON ELECTRONICS AMERICA, INC.**
2580 Orchard Parkway,
San Jose, CA 95131, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

## EUROPE

**EPSON EUROPE ELECTRONICS GmbH**
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

## ASIA

**EPSON (CHINA) CO., LTD.**
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

**SHANGHAI BRANCH**
7F, Block B, Hi-Tech Bldg., 900 Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

**SHENZHEN BRANCH**
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

**EPSON HONG KONG LTD.**
20/F, Harbour Centre, 25 Harbour Road,
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

**EPSON TAIWAN TECHNOLOGY & TRADING LTD.**
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

**EPSON SINGAPORE PTE., LTD.**
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

**SEIKO EPSON CORP.**
**KOREA OFFICE**
50F, KLI 63 Bldg., 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

**SEIKO EPSON CORP.**
**SEMICONDUCTOR OPERATIONS DIVISION**

**IC Sales Dept.**
**IC International Sales Group**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

Document Code: 411682202
First Issue June 2009
Revised September 2009 in JAPAN