

# 1

## PRODUCT OVERVIEW

### OVERVIEW

The S3C72N2/C72N4 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With features such as, LCD direct drive capability, 8-bit timer/counter, and watch timer, the S3C72N2/C72N4 offers an excellent design solution for a wide variety of applications that require LCD functions.

Up to 16 pins of the 64-pin QFP package, it can be dedicated to I/O. Four vectored interrupts provide fast response to internal and external events. In addition, the S3C72N2/C72N4 's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

### OTP

The S3C72N2/C72N4 microcontroller is also available in OTP (One Time Programmable) version, S3P72N4 . The S3P72N4 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P72N4 is comparable to S3C72N2/C72N4, both in function and in pin configuration.

## FEATURES

### Memory

- 288 × 4-bit RAM
- 2048 × 8-bit ROM (S3C72N2)
- 4096 × 8-bit ROM (S3C72N4)

### I/O Pins

- Input only: 4 pins
- I/O: 12 pins
- Output: 8 pins sharing with segment driver outputs

### LCD Controller/Driver

- Maximum 16-digit LCD direct drive capability
- 32 segment, 4 common pins
- Display modes: Static, 1/2 duty (1/2 bias)  
1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

### 8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

### 8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output

### Watch Timer

- Real-time and interval time measurement
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

### Bit Sequential Carrier

- Support 16-bit serial data transfer in arbitrary format

### Interrupts

- Two internal vectored interrupts
- Two external vectored interrupts
- Two quasi-interrupts

### Memory-Mapped I/O Structure

- Data memory bank 15

### Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main or sub system oscillation stops)

### Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal or external oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

### Instruction Execution Times

- 0.95, 1.91, 15.3  $\mu$ s at 4.19 MHz (main)
- 122  $\mu$ s at 32.768 kHz (subsystem)

### Operating Temperature

- -40 °C to 85 °C

### Operating Voltage Range

- 2.0 V to 5.5 V at 4.19 MHz
- 1.8 V to 5.5 V at 3 MHz

### Package Type

- 64-pin QFP

BLOCK DIAGRAM

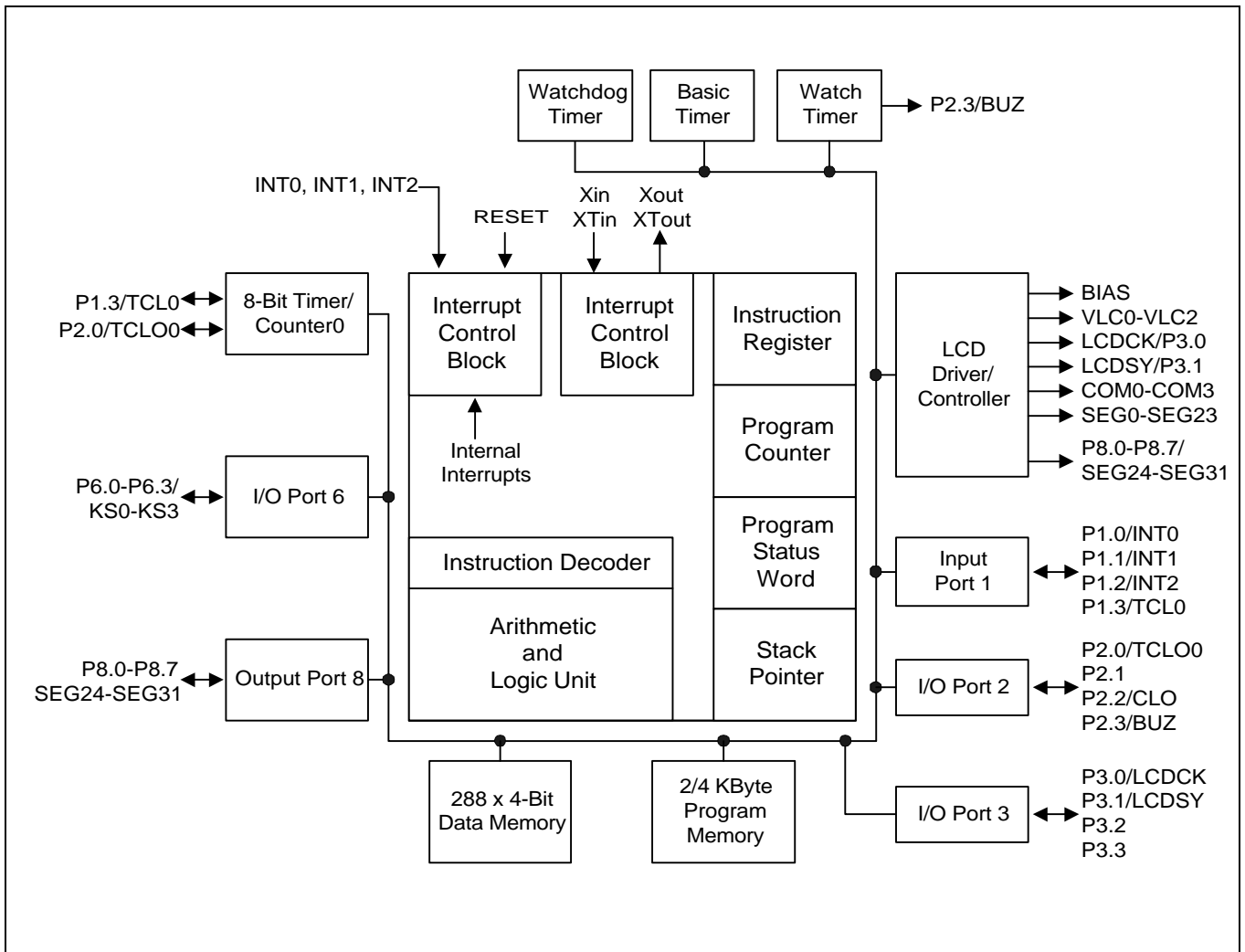


Figure 1-1. S3C72N2/C72N4 Simplified Block Diagram

PIN ASSIGNMENTS

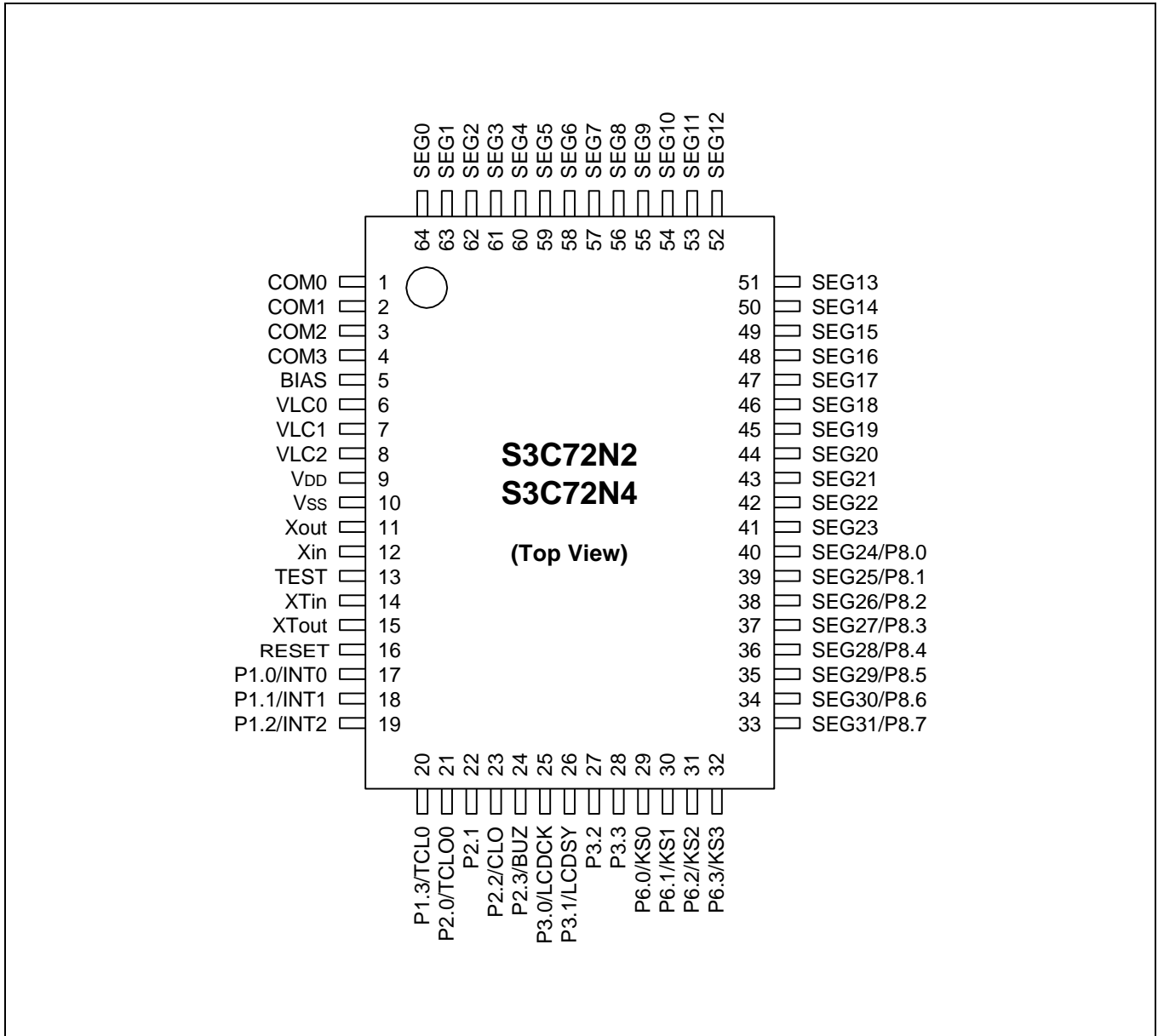


Figure 1-2. S3C72N2/C72N4 64-QFP Pin Assignment

## PIN DESCRIPTIONS

Table 1-1. S3C72N2/C72N4 Pin Descriptions

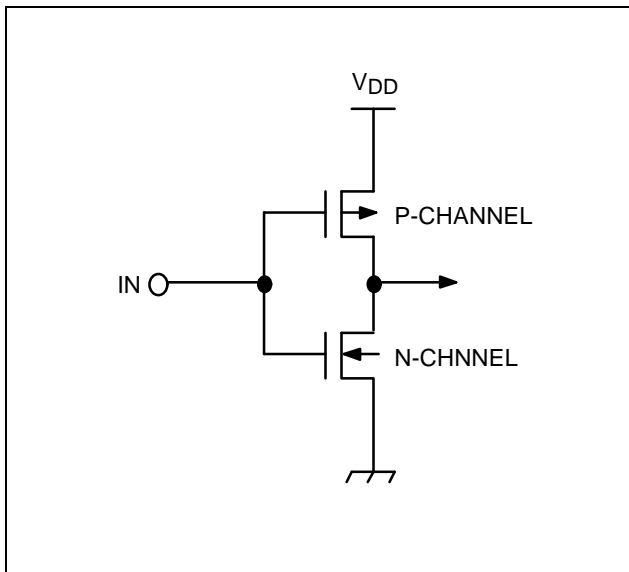
Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test is possible. 4-bit pull-up resistors are software assignable.	17 18 19 20	INT0 INT1 INT2 TCL0	Input	A-4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable.	21 22 23 24	TCLO0 – CLO BUZ	Input	D
P3.0 P3.1 P3.2 P3.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Each individual pin can be specified as input or output. 4-bit pull-up resistors are software assignable.	25 26 27 28	LCDCK LCDSY	Input	D
P6.0–P6.3	I/O	4-bit I/O ports. Pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable.	29–32	KS0–KS3	Input	D
P8.0–P8.7	O	Output port for 1-bit data (for use as CMOS driver only)	40–33	SEG24– SEG31	Output	H-1
SEG0–SEG23	O	LCD segment signal output	64–41	–	Output	H
SEG24–SEG31	O	LCD segment signal output	40–33	P8.0–P8.7	Output	H-1
COM0–COM3	O	LCD common signal output	1–4	–	Output	H
V <sub>LC0</sub> –V <sub>LC2</sub>	–	LCD power supply. Built-in voltage dividing resistors	6–8	–	–	–
BIAS	–	LCD power control	5	–	–	–
LCDCK	I/O	LCD clock output for display expansion	25	P3.0	Input	D

Table 1-1. S3C72N2/C72N4 Pin Descriptions (Continued)

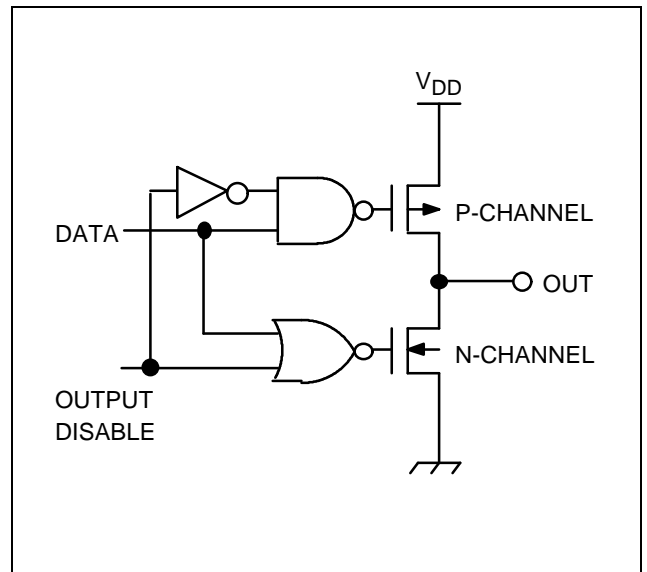
Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
LCDSY	I/O	LCD synchronization clock output for LCD display expansion	26	P3.1	Input	D
TCL0	I	External clock input for timer/counter 0	20	P1.3	Input	A-4
TCLO0	I/O	Timer/counter 0 clock output	21	P2.0	Input	D
INT0 INT1	I	External interrupt. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	17 18	P1.0 P1.1	Input	A-4
INT2	I	Quasi-interrupt with detection of rising edge signals.	19	P1.2	Input	A-4
KS0–KS3	I/O	Quasi-interrupt input with falling edge detection.	29–32	P6.0–P6.3	Input	D
CLO	I/O	CPU clock output	23	P2.2	Input	D
BUZ	I/O	2, 4, 8 or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32.768 kHz subsystem clock.	24	P2.3	Input	D
X <sub>IN</sub> , X <sub>OUT</sub>	–	Crystal, ceramic or RC oscillator pins for main system clock. (For external clock input, use X <sub>IN</sub> and input X <sub>IN</sub> 's reverse phase to X <sub>OUT</sub> )	12,11	–	–	–
XT <sub>IN</sub> , XT <sub>OUT</sub>	–	Crystal oscillator pins for subsystem clock. (For external clock input, use XT <sub>IN</sub> and input XT <sub>IN</sub> 's reverse phase to XT <sub>OUT</sub> )	14,15	–	–	–
V <sub>DD</sub>	–	Main power supply	9	–	–	–
V <sub>SS</sub>	–	Ground	10	–	–	–
RESET	–	Reset signal	16	–	Input	B
TEST	–	Test signal input (must be connected to V <sub>SS</sub> )	13	–	–	–

**NOTE:** Pull-up resistors for all I/O ports automatically disabled if they are configured to output mode.

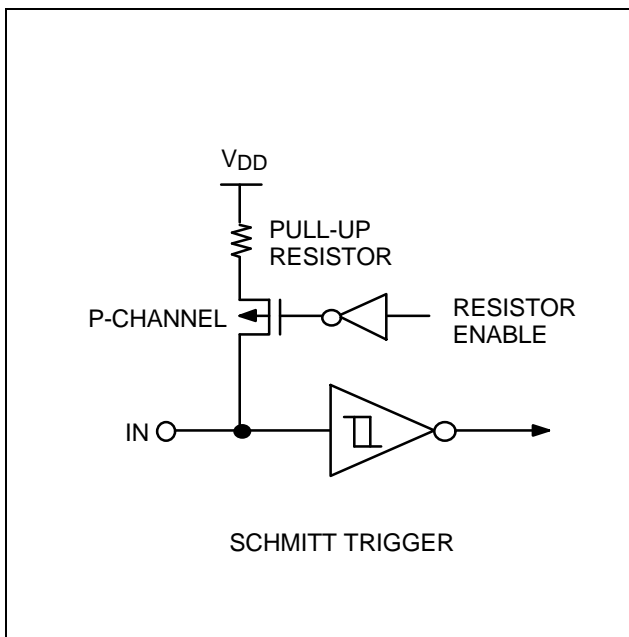
**PIN CIRCUIT DIAGRAMS**



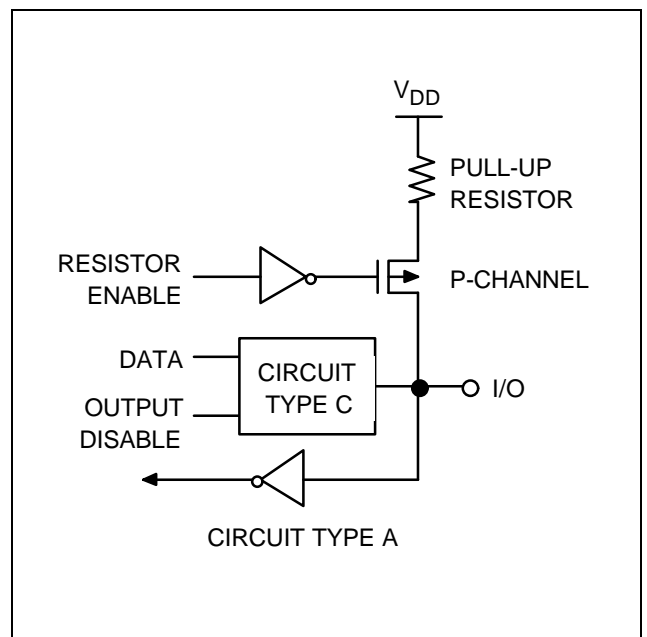
**Figure 1-3. Pin Circuit Type A**



**Figure 1-5. Pin Circuit Type C**



**Figure 1-4. Pin Circuit Type A-4 (P1)**



**Figure 1-6. Pin Circuit Type D (P2, P3, and P6)**

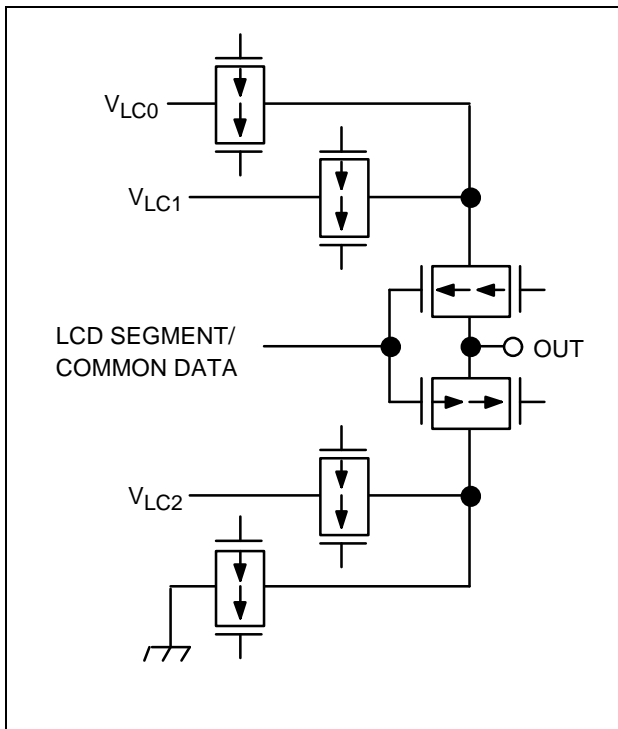


Figure 1-7. Pin Circuit Type H (SEG/COM)

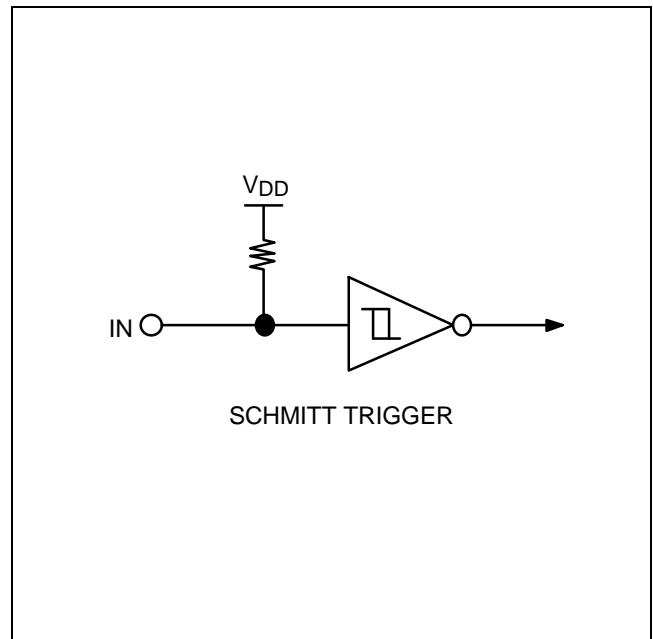


Figure 1-9. Pin Circuit Type B (RESET)

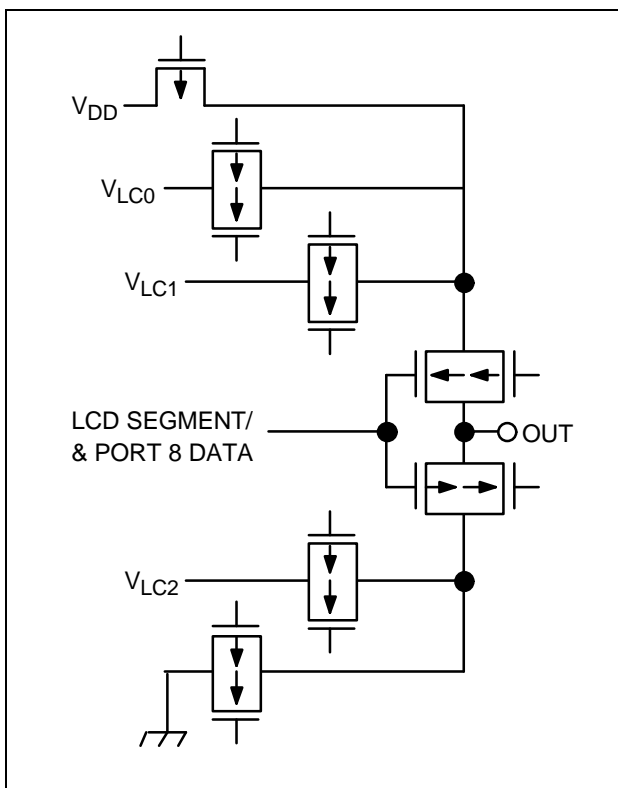


Figure 1-8. Pin Circuit Type H-1 (P8)



# 13

## ELECTRICAL DATA

### OVERVIEW

In this section, information on S3C72N2/C72N4 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

#### STANDARD ELECTRICAL CHARACTERISTICS

- Absolute maximum ratings
- D.C. electrical characteristics
- Main system clock oscillator characteristics
- Subsystem clock oscillator characteristics
- I/O capacitance
- A.C. electrical characteristics
- Operating voltage range

#### MISCELLANEOUS TIMING WAVEFORMS

- A.C timing measurement point
- Clock timing measurement at  $X_{IN}$
- Clock timing measurement at  $XT_{IN}$
- TCL0 timing
- Input timing for RESET
- Input timing for external interrupts

#### STOP MODE CHARACTERISTICS AND TIMING WAVEFORMS

- RAM data retention supply voltage in stop mode
- Stop mode release timing when initiated by RESET
- Stop mode release timing when initiated by an interrupt request

Table 13-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$ 

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	$V_{DD}$	–	– 0.3 to + 6.5	V
Input Voltage	$V_{IH1}$	All I/O ports	– 0.3 to $V_{DD} + 0.3$	
Output Voltage	$V_O$		– 0.3 to $V_{DD} + 0.3$	
Output Current High	$I_{OH}$	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output Current Low	$I_{OL}$	One I/O port active	+ 30 (Peak value)	
			+ 15 (note)	
		Total value for ports 2 and 3	+ 60 (Peak value) + 20 (note)	
		Total value for port 6	+ 50 + 20 (note)	
Operating Temperature	$T_A$	–	– 40 to + 85	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	–	– 65 to + 150	

**NOTE:** The values for Output Current Low ( $I_{OL}$ ) are calculated as Peak Value  $\times \sqrt{\text{Duty}}$ .

Table 13-2. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	$V_{IH1}$	All input pins except those specified below for $V_{IH2}$ , $V_{IH3}$	$0.7 V_{DD}$	–	$V_{DD}$	V
	$V_{IH2}$	Ports 1, 6, and RESET	$0.8 V_{DD}$	–	$V_{DD}$	
	$V_{IH3}$	$X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	$V_{DD} - 0.1$	–	$V_{DD}$	
Input low voltage	$V_{IL1}$	Ports 2 and 3	–	–	$0.3 V_{DD}$	V
	$V_{IL2}$	Ports 1, 6 and RESET	–	–	$0.2 V_{DD}$	
	$V_{IL3}$	$X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	–	–	0.1	
Output high voltage	$V_{OH1}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OH} = -1\text{ mA}$ Ports 2, 3, 6 and BIAS	$V_{DD} - 1.0$	–	–	V
	$V_{OH2}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OH} = -100\text{ }\mu\text{A}$ Port 8 only	$V_{DD} - 2.0$	–	–	

Table 13-2. D.C. Electrical Characteristics (Continued)

 $(T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Output low voltage	$V_{OL1}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OL} = 15\text{ mA}$ , Ports 2, 3, 6	–	0.4	2	V	
	$V_{OL2}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OL} = 100\text{ }\mu\text{A}$ ; Port 8 only	–	–	1		
Input high leakage current	$I_{LIH1}$	$V_{IN} = V_{DD}$ All input pins except those specified below for $I_{LIH2}$	–	–	3	$\mu\text{A}$	
	$I_{LIH2}$	$V_{IN} = V_{DD}$ $X_{IN}$ , $X_{OUT}$ and $XT_{IN}$			20		
Input low leakage current	$I_{LIL1}$	$V_{IN} = 0\text{ V}$ All input pins except $X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	–	–	–3		
	$I_{LIL2}$	$V_{IN} = 0\text{ V}$ $X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$			–20		
Output high leakage current	$I_{LOH1}$	$V_{OUT} = V_{DD}$ All output pins	–	–	3	$\mu\text{A}$	
	$I_{LOL}$	$V_{OUT} = 0\text{ V}$ All output pins			–3		
Pull-up resistor	$R_{L1}$	$V_{IN} = 0\text{ V}$ ; $V_{DD} = 5\text{ V}$ Ports 1, 2, 3, 6	25	50	100	$\text{K}\Omega$	
		$V_{DD} = 3\text{ V}$	50	100	200		
	$R_{L2}$	$V_{IN} = 0\text{ V}$ ; $V_{DD} = 5\text{ V}$ RESET	100	250	400		
		$V_{DD} = 3\text{ V}$	200	500	800		
LCD voltage dividing resistor	$R_{LCD}$	$T_A = 25\text{ }^\circ\text{C}$	120	170	220		
COM output impedance	$R_{COM}$	$V_{DD} = 5\text{ V}$	–	3	6		
		$V_{DD} = 3\text{ V}$		5	15		
SEG output impedance	$R_{SEG}$	$V_{DD} = 5\text{ V}$	3	6			
		$V_{DD} = 3\text{ V}$	5	15			
COM output voltage deviation	$V_{DC}$	$V_{DD} = 5\text{ V}$ ( $V_{LC0-COMi}$ ) $I_o = \pm 15\text{ }\mu\text{A}$ ( $i = 0-3$ )	–	$\pm 45$	$\pm 90$		mV

Table 13-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SEG output voltage deviation	V <sub>DS</sub>	V <sub>DD</sub> = 5 V (VLC0-SEGi) I <sub>o</sub> = ± 15μA (i= 0-31)	–	± 45	± 90	mV
VLC0 Output voltage	VLC0	T <sub>A</sub> = 25 °C	0.6V <sub>DD</sub> – 0.2	0.6V <sub>DD</sub>	0.6V <sub>DD</sub> + 0.2	V
VLC1 Output voltage	VLC1	T <sub>A</sub> = 25 °C	0.4V <sub>DD</sub> – 0.2	0.4V <sub>DD</sub>	0.4V <sub>DD</sub> + 0.2	
VLC2 Output voltage	VLC2	T <sub>A</sub> = 25 °C	0.2V <sub>DD</sub> – 0.2	0.2V <sub>DD</sub>	0.2V <sub>DD</sub> + 0.2	

Table 13-2. D.C. Electrical Characteristics (Concluded)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

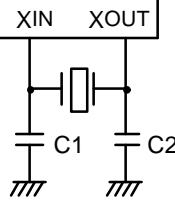
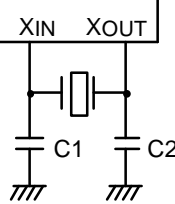
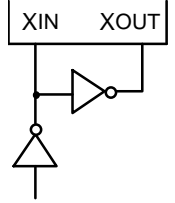
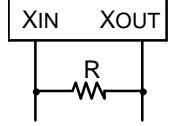
Parameter	Symbol	Conditions	Min	Typ	Max	Units			
Supply Current (1)	I <sub>DD1</sub> (2)	Main operating: V <sub>DD</sub> = 5 V ± 10% CPU = fx/4 SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V <sub>DD</sub> = 3 V ± 10%	6.0 MHz	-	3.5	8	mA		
			4.19 MHz		2.5	5.5			
	I <sub>DD2</sub> (2)	Main idle mode; V <sub>DD</sub> = 5 V ± 10% CPU = fx/4 SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V <sub>DD</sub> = 3 V ± 10%	6.0 MHz	-	1	2.5			
			4.19 MHz		0.9	2			
	I <sub>DD3</sub>	Sub operating: V <sub>DD</sub> = 3 V ± 10% CPU = fxt/4, SCMOD = 1001B 32 kHz crystal oscillator	6.0 MHz	-	15	30		μA	
			4.19 MHz		0.5	1.0			
I <sub>DD4</sub>			Sub idle mode: V <sub>DD</sub> = 3 V ± 10% CPU = fxt/4, SCMOD = 1001B 32 kHz crystal oscillator		6.0 MHz	-	6		15
					4.19 MHz		0.4		0.8
I <sub>DD5</sub>	Stop mode: V <sub>DD</sub> = 5V ± 10% CPU=fxt/4, SCMOD = 1101B	-	0.5	3					
I <sub>DD6</sub> (3)	Stop mode: V <sub>DD</sub> = 5 V ± 10% CPU = fx/4, SCMOD = 0100B								

**NOTES:**

- D.C. electrical values for supply current (I<sub>DD1</sub> to I<sub>DD6</sub>) do not include current drawn through internal pull-up resistors and through LCD voltage dividing resistors.
- Data includes the power consumption for sub-system clock oscillation.
- When the system clock mode register, SCMOD, is set to 0100B, the sub-system clock oscillation stops. The main-system clock oscillation stops by the STOP instruction.

Table 13-3. Main System Clock Oscillator Characteristics

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

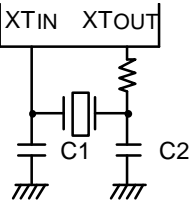
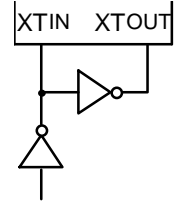
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	Stabilization occurs when V <sub>DD</sub> is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	V <sub>DD</sub> = 4.5 V to 5.5 V	–	–	10	ms
		V <sub>DD</sub> = 1.8 V to 4.5 V	–	–	30		
External Clock		X <sub>IN</sub> input frequency (1)	–	0.4	–	6.0	MHz
		X <sub>IN</sub> input high and low level width (t <sub>XH</sub> , t <sub>XL</sub> )	–	83.3	–	–	ns
RC Oscillator		Frequency (1)	V <sub>DD</sub> = 5 V R = 20 KΩ, V <sub>DD</sub> = 5 V R = 39 KΩ, V <sub>DD</sub> = 3 V	0.4	– 2.0 1.0	2	MHz

**NOTES:**

- Oscillation frequency and X<sub>IN</sub> input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 13-4. Subsystem Clock Oscillator Characteristics

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V <sub>DD</sub> = 4.5 V to 5.5 V	–	1.0	2	s
			V <sub>DD</sub> = 1.8 V to 4.5 V	–	–	10	
External Clock		XT <sub>IN</sub> input frequency (1)	–	32	–	100	KHz
		XT <sub>IN</sub> input high and low level width (t <sub>XTL</sub> , t <sub>XTH</sub> )	–	5	–	15	μs

**NOTES:**

- Oscillation frequency and XT<sub>IN</sub> input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

Table 13-5. Input/Output Capacitance

(T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C <sub>IN</sub>	f = 1 MHz; Unmeasured pins are returned to V <sub>SS</sub>	–	–	15	pF
Output capacitance	C <sub>OUT</sub>		–	–	15	pF
I/O capacitance	C <sub>IO</sub>		–	–	15	pF

Table 13-6. A.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t <sub>CY</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.67	–	64	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	0.95	–	64	
		With subsystem clock (fxt)	114	122	125	
TCL0 input frequency	f <sub>TIO</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0	–	1.5	MHz
		V <sub>DD</sub> = 1.8 V to 5.5 V			1	MHz
TCL0 input high, low width	t <sub>TIHO</sub> , t <sub>TILO</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.48	–	–	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.8			
Interrupt input high, low width	t <sub>INTH</sub> , t <sub>INTL</sub>	INT0	(2)	–	–	μs
		INT1, INT2, KS0–KS3	10			
RESET Input Low Width	t <sub>RSL</sub>	Input	10	–	–	μs

**NOTES:**

1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.
2. Minimum value for INT0 is based on a clock of 2t<sub>CY</sub> or 128/fx as assigned by the IMOD0 register setting.



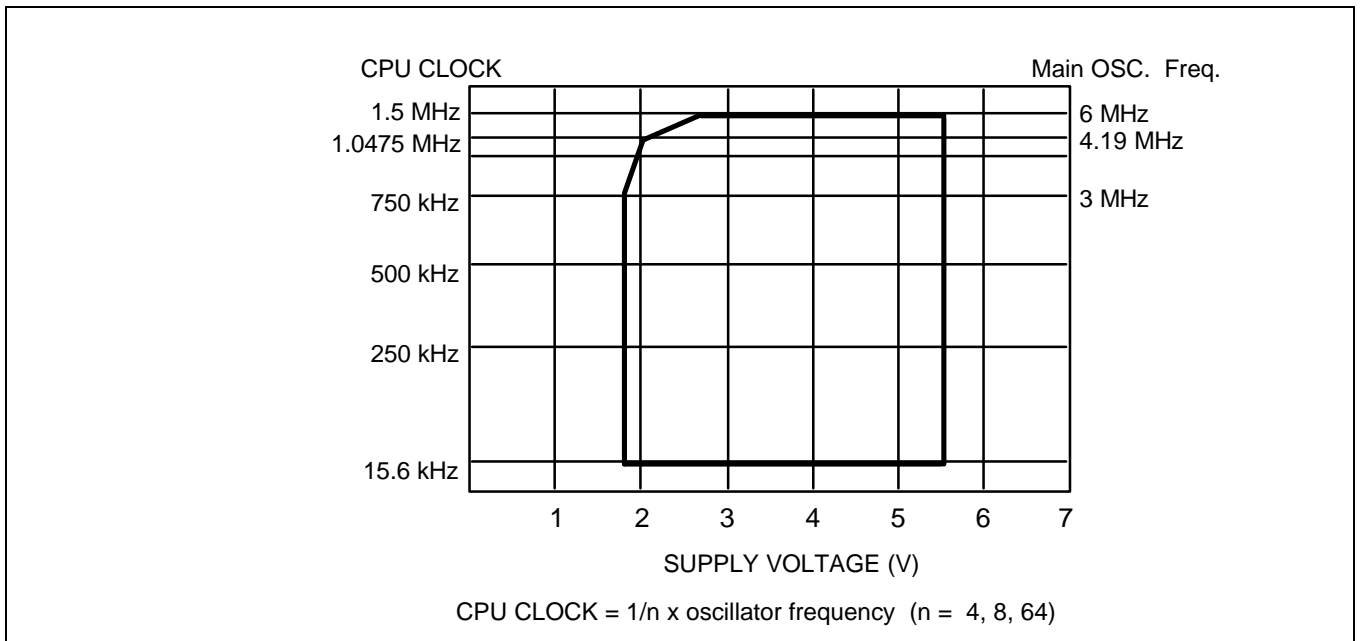


Figure 13-1. Standard Operating Voltage Range

Table 13-7. RAM Data Retention Supply Voltage in Stop Mode

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDDR}$	Normal operation	1.5	–	6.5	V
Data retention supply current	$I_{DDDR}$	$V_{DDDR} = 2.0\text{ V}$	–	0.1	1	$\mu\text{A}$
Release signal set time	$t_{SREL}$	Normal operation	0	–	–	$\mu\text{s}$
Oscillator stabilization wait time (1)	$t_{WAIT}$	Released by RESET	–	$2^{17} / f_x$	–	ms
		Released by interrupt	–	(2)	–	

**NOTES:**

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

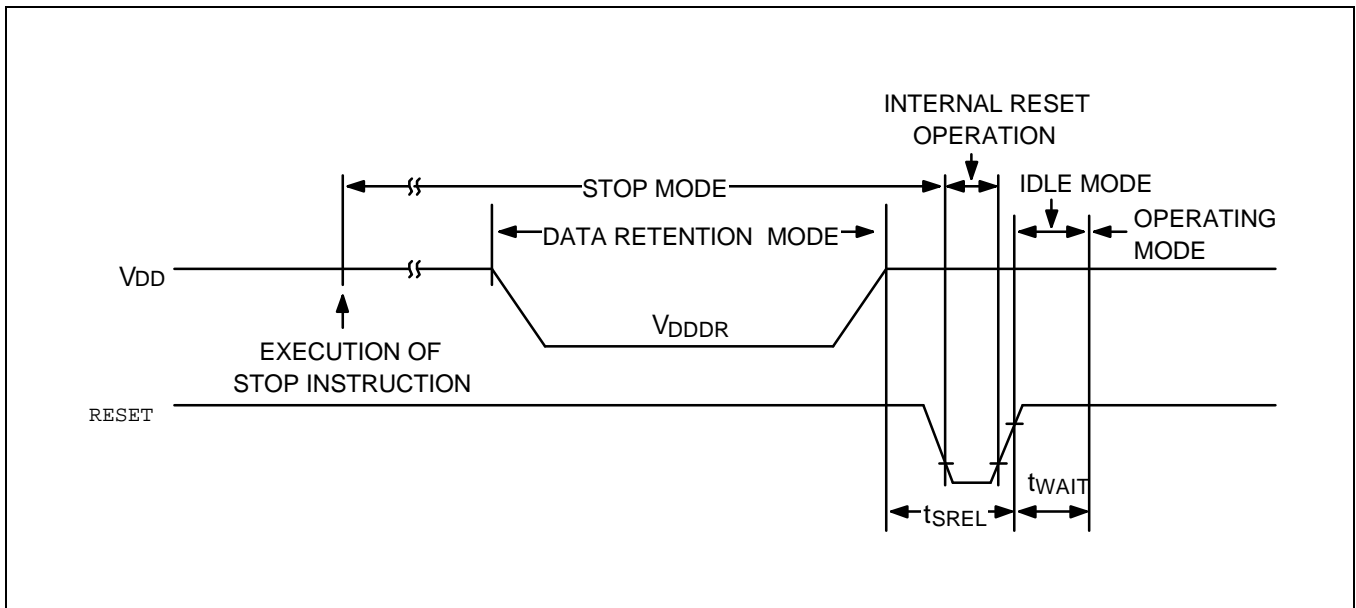


Figure 13-2. Stop Mode Release Timing When Initiated By RESET

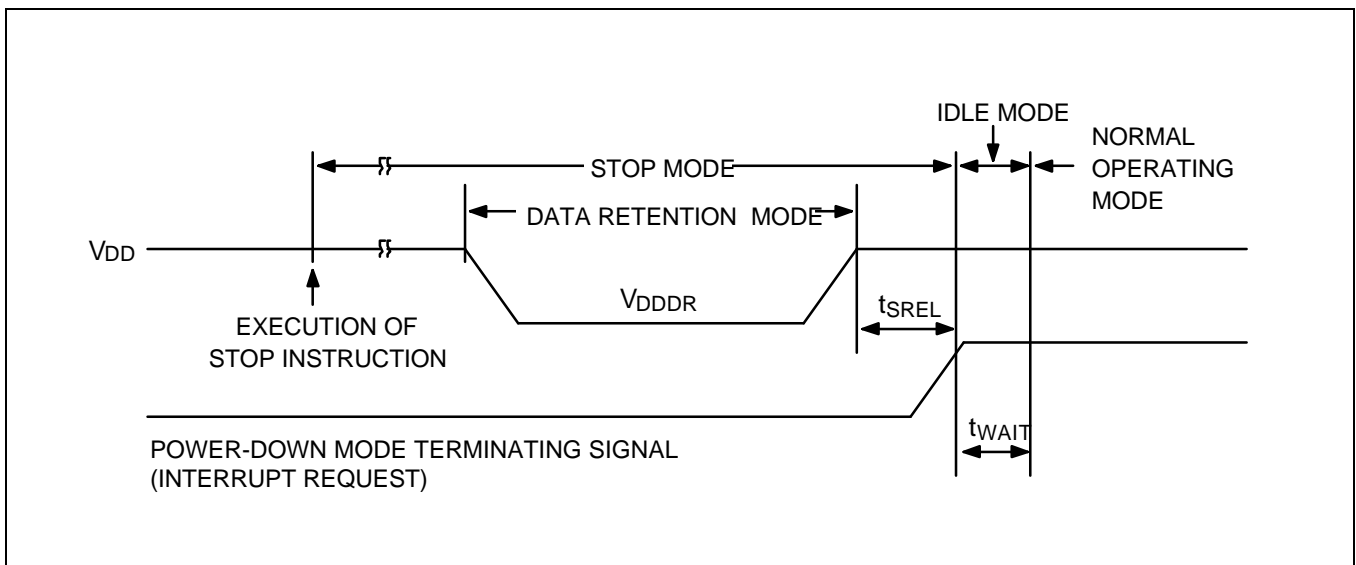


Figure 13-3. Stop Mode Release Timing When Initiated By Interrupt Request

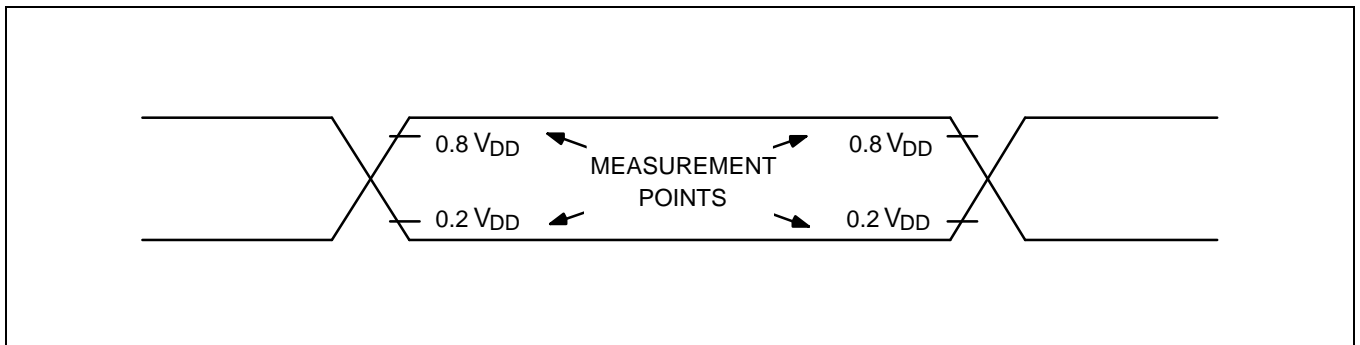


Figure 13-4. A.C. Timing Measurement Points (Except for  $X_{in}$  and  $XT_{in}$ )

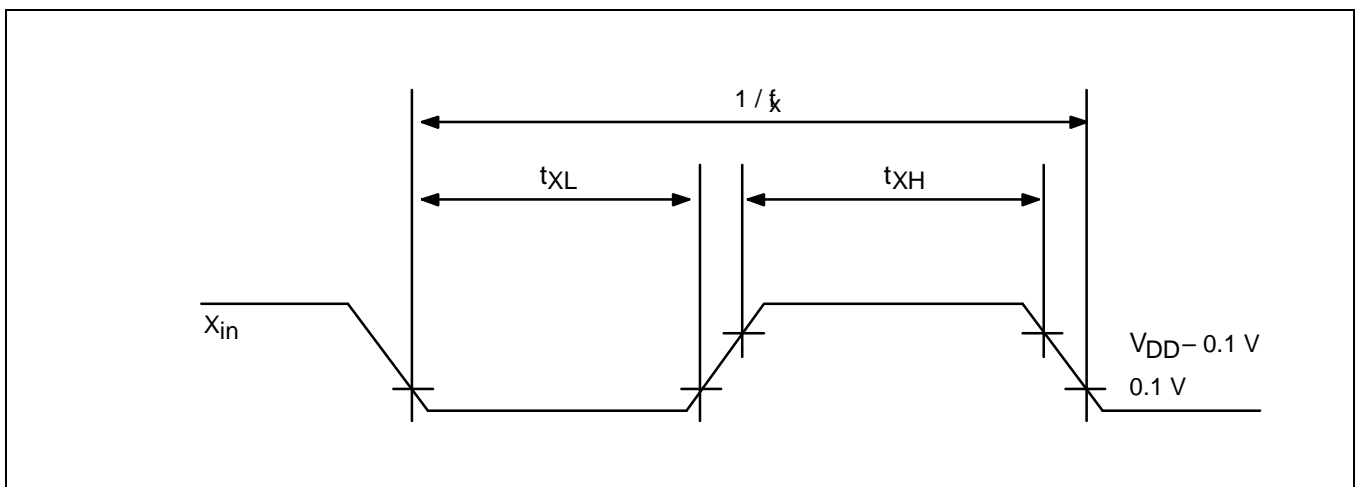


Figure 13-5. Clock Timing Measurement at  $X_{in}$

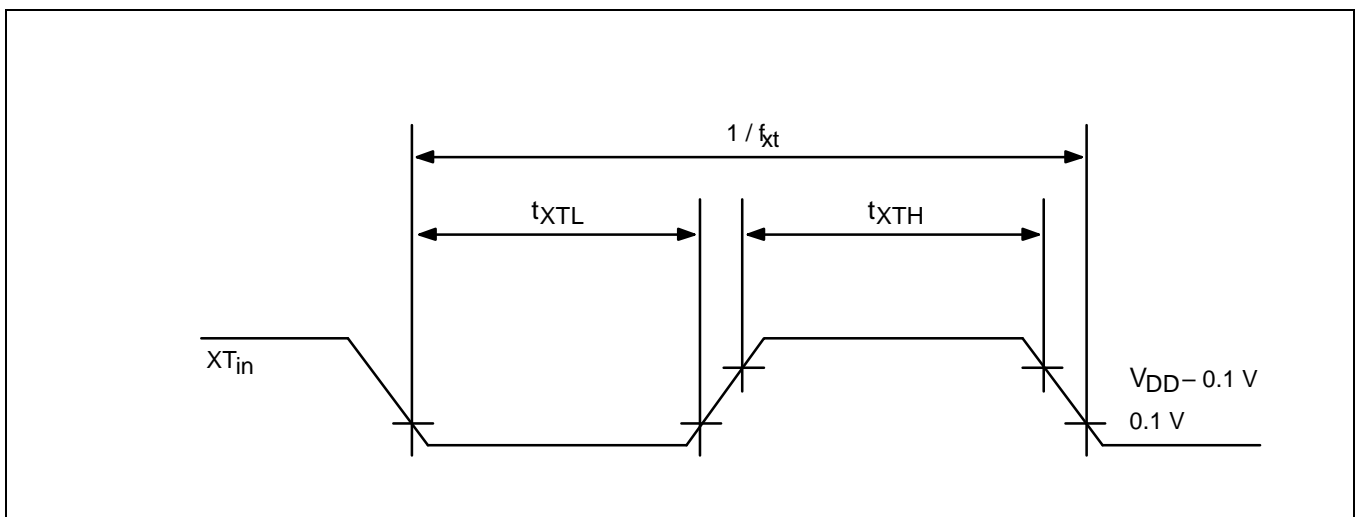


Figure 13-6. Clock Timing Measurement at  $XT_{in}$

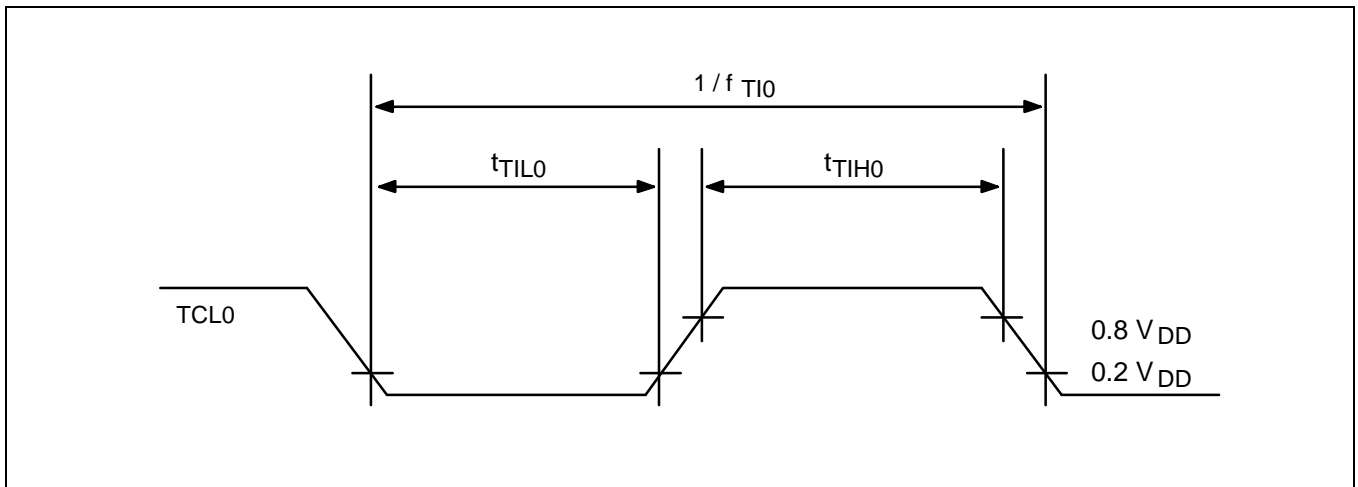


Figure 13-7. TCL0 Timing

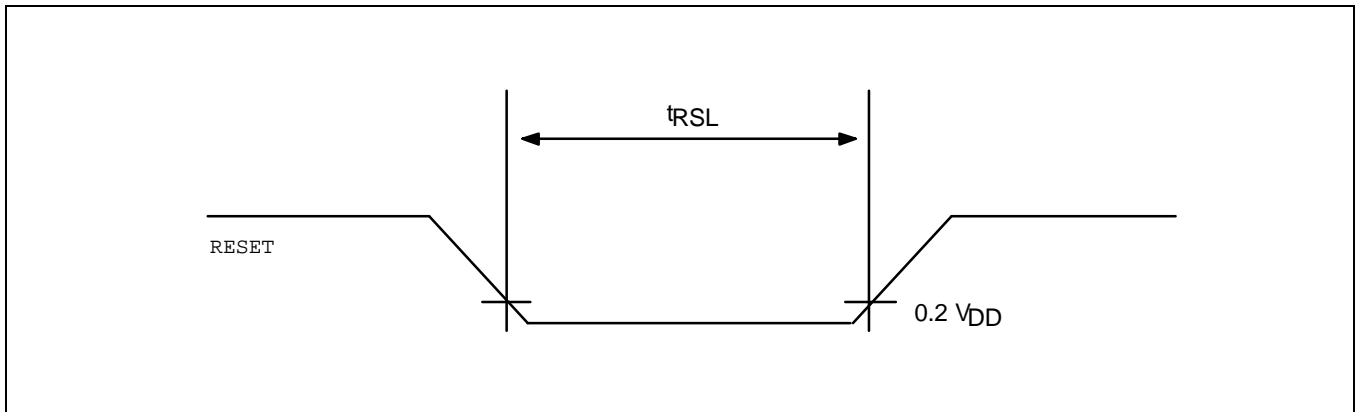


Figure 13-8. Input Timing for RESET Signal

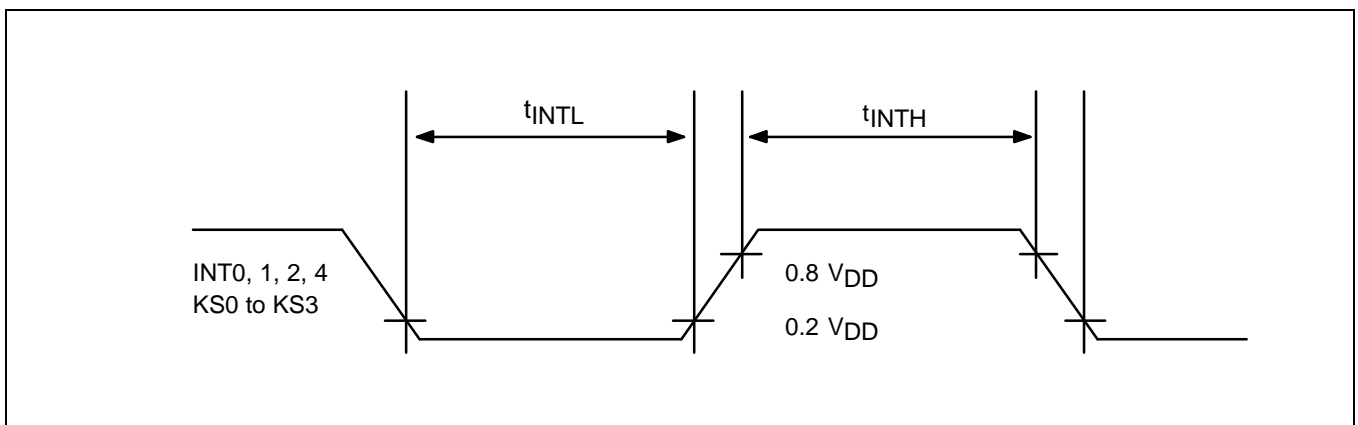


Figure 13-9. Input Timing for External Interrupts and Quasi-Interrupts

# 14 MECHANICAL DATA

## OVERVIEW

The S3C72N2/C72N4 microcontroller is available in a 64-pin QFP package (Samsung: 64-QFP-1420F). Package dimensions are shown in Figure 14-1.

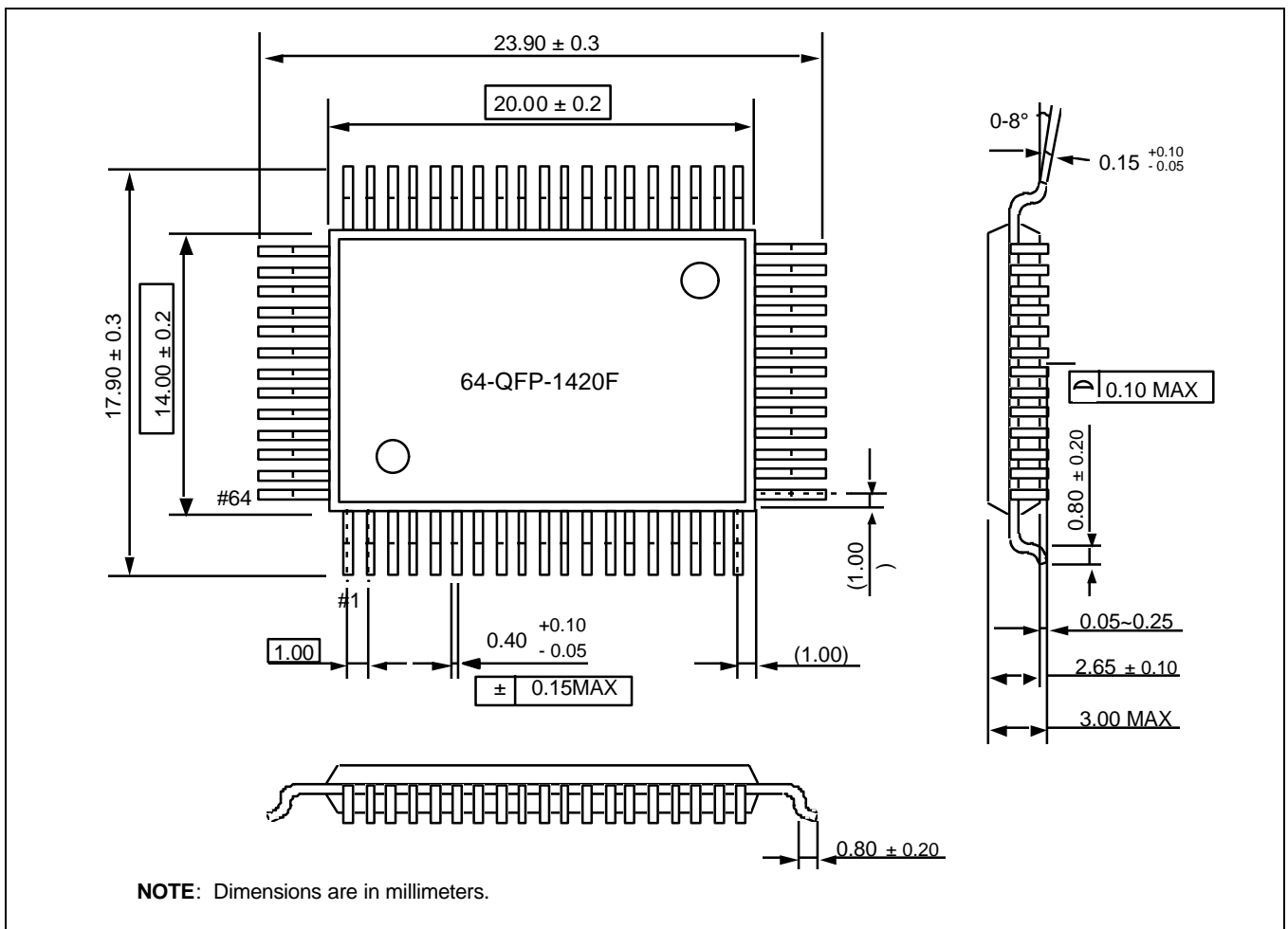


Figure 14-1. 64-QFP-1420F Package Dimensions

# 15

## S3P72N4 OTP

### OVERVIEW

The S3P72N4 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72N2/C72N4 microcontroller. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by a serial data format.

The S3P72N4 is fully compatible with the S3C72N2/C72N4, both in function and in pin configuration. Because of its simple programming requirements, the S3P72N4 is ideal for use as an evaluation chip for the S3C72N4.

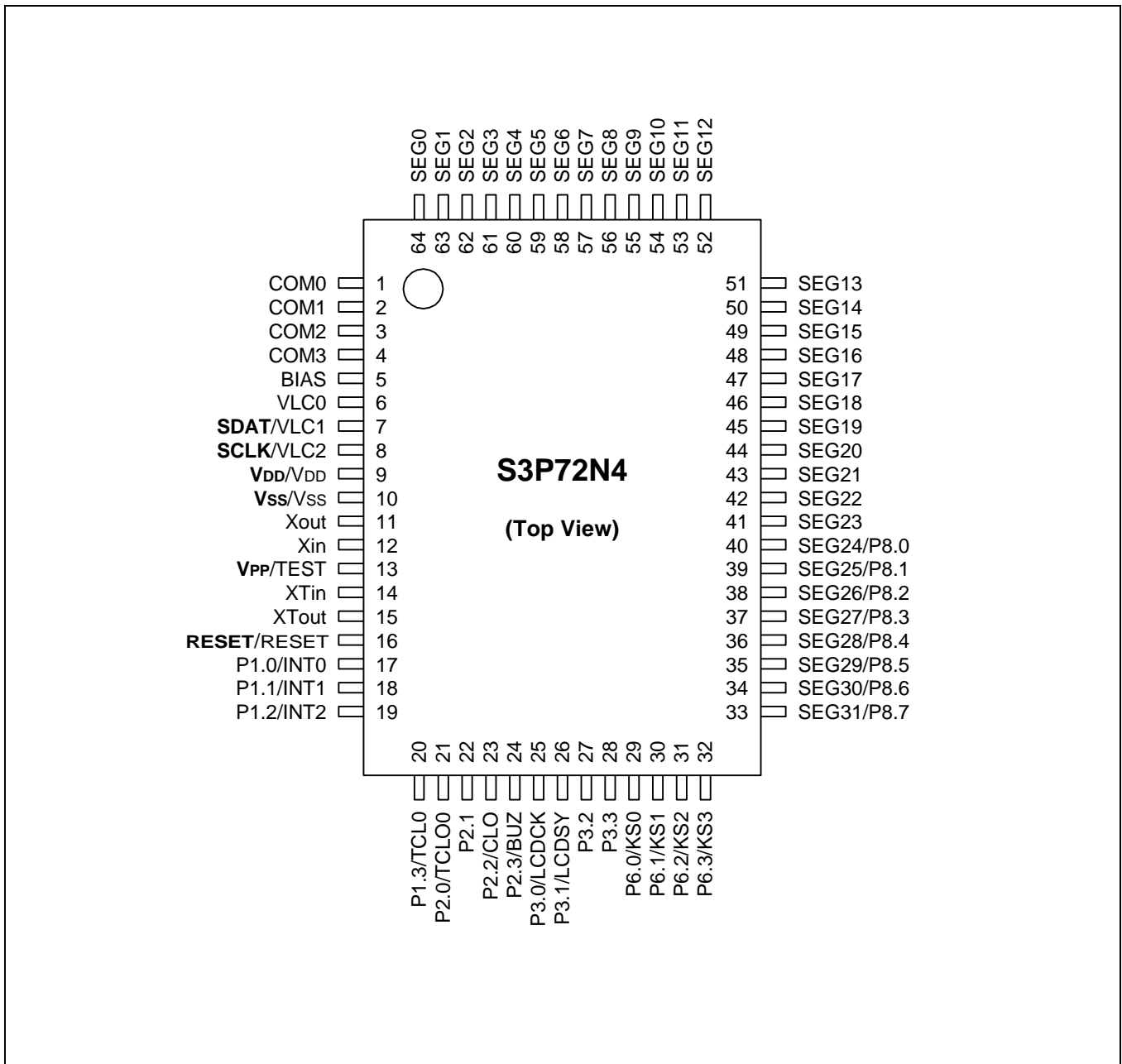


Figure 15-1. S3P72N4 Pin Assignments (64-QFP)

Table 15-1. Pin Descriptions Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
V <sub>LC1</sub>	SDAT	7	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
V <sub>LC2</sub>	SCLK	8	I/O	Serial clock pin. Input only pin.
TEST	V <sub>PP</sub> (TEST)	13	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	16	I	Chip initialization
V <sub>DD</sub> / V <sub>SS</sub>	V <sub>DD</sub> / V <sub>SS</sub>	9/10	I	Logic power supply pin. V <sub>DD</sub> should be tied to +5 V during programming.

Table 15-2. Comparison of S3P72N4 and S3C72N2/C72N4 Features

Characteristic	S3P72N4	S3C72N2/C72N4
Program Memory	4-Kbyte EPROM	2-K / 4-Kbyte mask ROM
Operating Voltage (V <sub>DD</sub> )	2.0 V to 5.5 V at 4.19 MHz 1.8 V to 5.5 V at 3 MHz	2.0 V to 5.5 V at 4.19 MHz 1.8 V to 5.5 V at 3 MHz
OTP Programming Mode	V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST) = 12.5 V	–
Pin Configuration	64 QFP	64 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

## OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>pp</sub> (TEST) pin of the S3P72N4, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-3. Operating Mode Selection Criteria

V <sub>DD</sub>	V <sub>pp</sub> (TEST)	REG/MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

**NOTE:** "0" means low level; "1" means high level.



Table 15-4. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	$V_{IH1}$	All input pins except those specified below for $V_{IH2}$ , $V_{IH3}$	$0.7 V_{DD}$	–	$V_{DD}$	V
	$V_{IH2}$	Ports 1, 6, and RESET	$0.8 V_{DD}$	–	$V_{DD}$	
	$V_{IH3}$	$X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	$V_{DD} - 0.1$	–	$V_{DD}$	
Input low voltage	$V_{IL1}$	Ports 2 and 3	–	–	$0.3 V_{DD}$	V
	$V_{IL2}$	Ports 1, 6 and RESET	–	–	$0.2 V_{DD}$	
	$V_{IL3}$	$X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	–	–	0.1	
Output high voltage	$V_{OH1}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OH} = -1\text{ mA}$ Ports 2, 3, 6 and BIAS	$V_{DD} - 1.0$	–	–	V
	$V_{OH2}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OH} = -100\text{ }\mu\text{A}$ Port 8 only	$V_{DD} - 2.0$	–	–	
Output low voltage	$V_{OL1}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OL} = 15\text{ mA}$ , Ports 2, 3, 6	–	0.4	2	V
	$V_{OL2}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OL} = 100\text{ }\mu\text{A}$ ; Port 8 only	–	–	1	
Input high leakage current	$I_{LIH1}$	$V_{IN} = V_{DD}$ All input pins except those specified below for $I_{LIH2}$	–	–	3	$\mu\text{A}$
	$I_{LIH2}$	$V_{IN} = V_{DD}$ $X_{IN}$ , $X_{OUT}$ and $XT_{IN}$	–	–	20	
Input low leakage current	$I_{LIL1}$	$V_{IN} = 0\text{ V}$ All input pins except $X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	–	–	–3	$\mu\text{A}$
	$I_{LIL2}$	$V_{IN} = 0\text{ V}$ $X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	–	–	–20	
Output high leakage current	$I_{LOH1}$	$V_{OUT} = V_{DD}$ All output pins	–	–	3	$\mu\text{A}$
Output low leakage current	$I_{LOL}$	$V_{OUT} = 0\text{ V}$ All output pins	–	–	–3	$\mu\text{A}$

Table 15-4. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pull-up resistor	R <sub>L1</sub>	V <sub>IN</sub> = 0 V; V <sub>DD</sub> = 5 V Ports 1, 2, 3, 6	25	50	100	KΩ
		V <sub>DD</sub> = 3 V	50	100	200	
	R <sub>L2</sub>	V <sub>IN</sub> = 0 V; V <sub>DD</sub> = 5 V RESET	100	250	400	
		V <sub>DD</sub> = 3 V	200	500	800	
LCD voltage dividing resistor	R <sub>LCD</sub>	T <sub>A</sub> = 25 °C	120	170	220	
COM output impedance	R <sub>COM</sub>	V <sub>DD</sub> = 5 V	-	3	6	
		V <sub>DD</sub> = 3 V		5	15	
SEG output impedance	R <sub>SEG</sub>	V <sub>DD</sub> = 5 V		3	6	
		V <sub>DD</sub> = 3 V		5	15	
COM output voltage deviation	V <sub>DC</sub>	V <sub>DD</sub> = 5 V (VLC0-COMi) I <sub>o</sub> = ± 15μA (i= 0-3)	-	± 45	± 90	mV
SEG output voltage deviation	V <sub>DS</sub>	V <sub>DD</sub> = 5 V (VLC0-SEGi) I <sub>o</sub> = ± 15μA (i= 0-31)	-	± 45	± 90	mV
VLC0 Output voltage	VLC0	T <sub>A</sub> = 25 °C	0.6V <sub>DD</sub> - 0.2	0.6V <sub>DD</sub>	0.6V <sub>DD</sub> + 0.2	V
VLC1 Output voltage	VLC1	T <sub>A</sub> = 25 °C	0.4V <sub>DD</sub> - 0.2	0.4V <sub>DD</sub>	0.4V <sub>DD</sub> + 0.2	
VLC2 Output voltage	VLC2	T <sub>A</sub> = 25 °C	0.2V <sub>DD</sub> - 0.2	0.2V <sub>DD</sub>	0.2V <sub>DD</sub> + 0.2	

Table 15-4. D.C. Electrical Characteristics (Concluded)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units		
Supply Current (1)	I <sub>DD1</sub> (2)	Main operating: V <sub>DD</sub> = 5 V ± 10% CPU = fx/4 SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	-	3.5 2.5	8 5.5	mA	
		V <sub>DD</sub> = 3 V ± 10%	6.0 MHz 4.19 MHz		1.6 1.2	4 3		
	I <sub>DD2</sub> (2)	Main idle mode; V <sub>DD</sub> = 5 V ± 10% CPU = fx/4 SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	-	1 0.9	2.5 2		
		V <sub>DD</sub> = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.4	1.0 0.8		
	I <sub>DD3</sub>	Sub operating: V <sub>DD</sub> = 3 V ± 10% CPU = fxt/4, SCMOD = 1001B 32 kHz crystal oscillator		-	15	30		μA
	I <sub>DD4</sub>	Sub idle mode: V <sub>DD</sub> = 3 V ± 10% CPU = fxt/4, SCMOD = 1001B 32 kHz crystal oscillator		-	6	15		
I <sub>DD5</sub>	Stop mode: V <sub>DD</sub> = 5 V ± 10% CPU=fxt/4, SCMOD = 1101B							
I <sub>DD6</sub> (3)	Stop mode: V <sub>DD</sub> = 5 V ± 10% CPU = fx/4, SCMOD = 0100B		-	0.5	3			

**NOTES:**

- D.C. electrical values for supply current (I<sub>DD1</sub> to I<sub>DD6</sub>) do not include current drawn through internal pull-up resistors and through LCD voltage dividing resistors.
- Data includes the power consumption for sub-system clock oscillation.
- When the system clock mode register, SCMOD, is set to 0100B, the sub-system clock oscillation stops. The main-system clock oscillation stops by the STOP instruction.

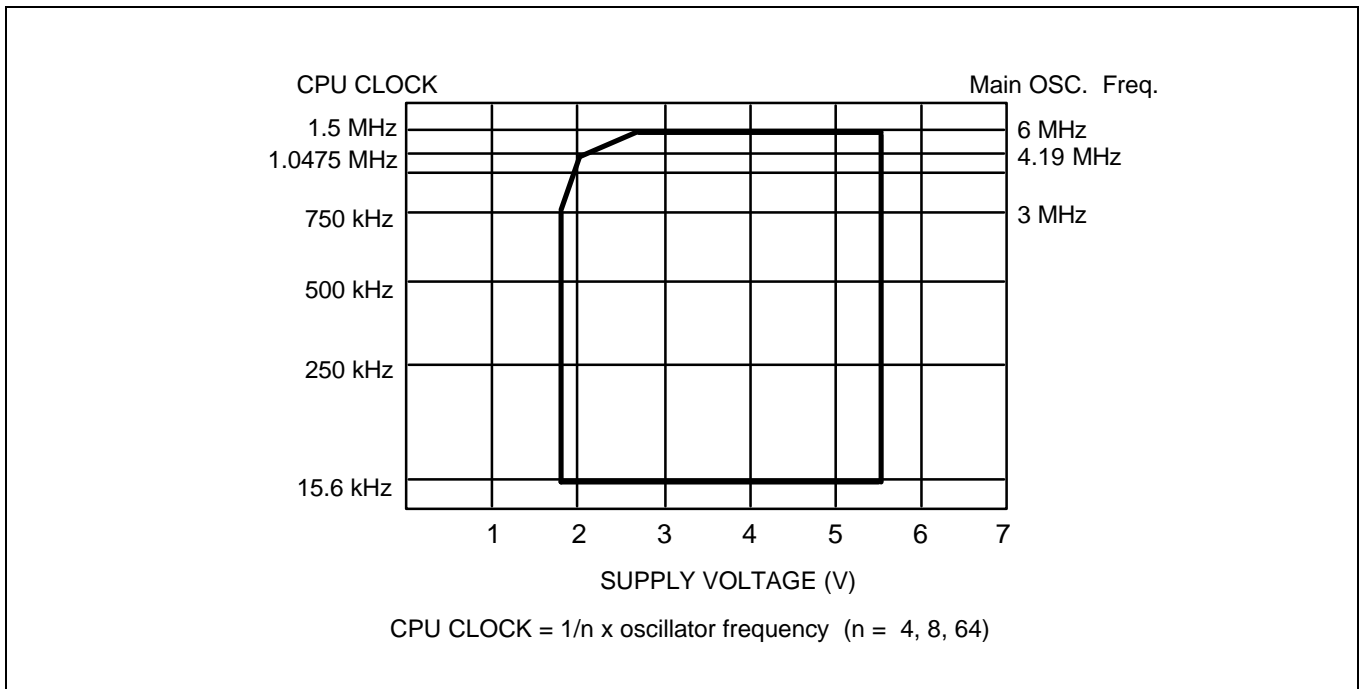
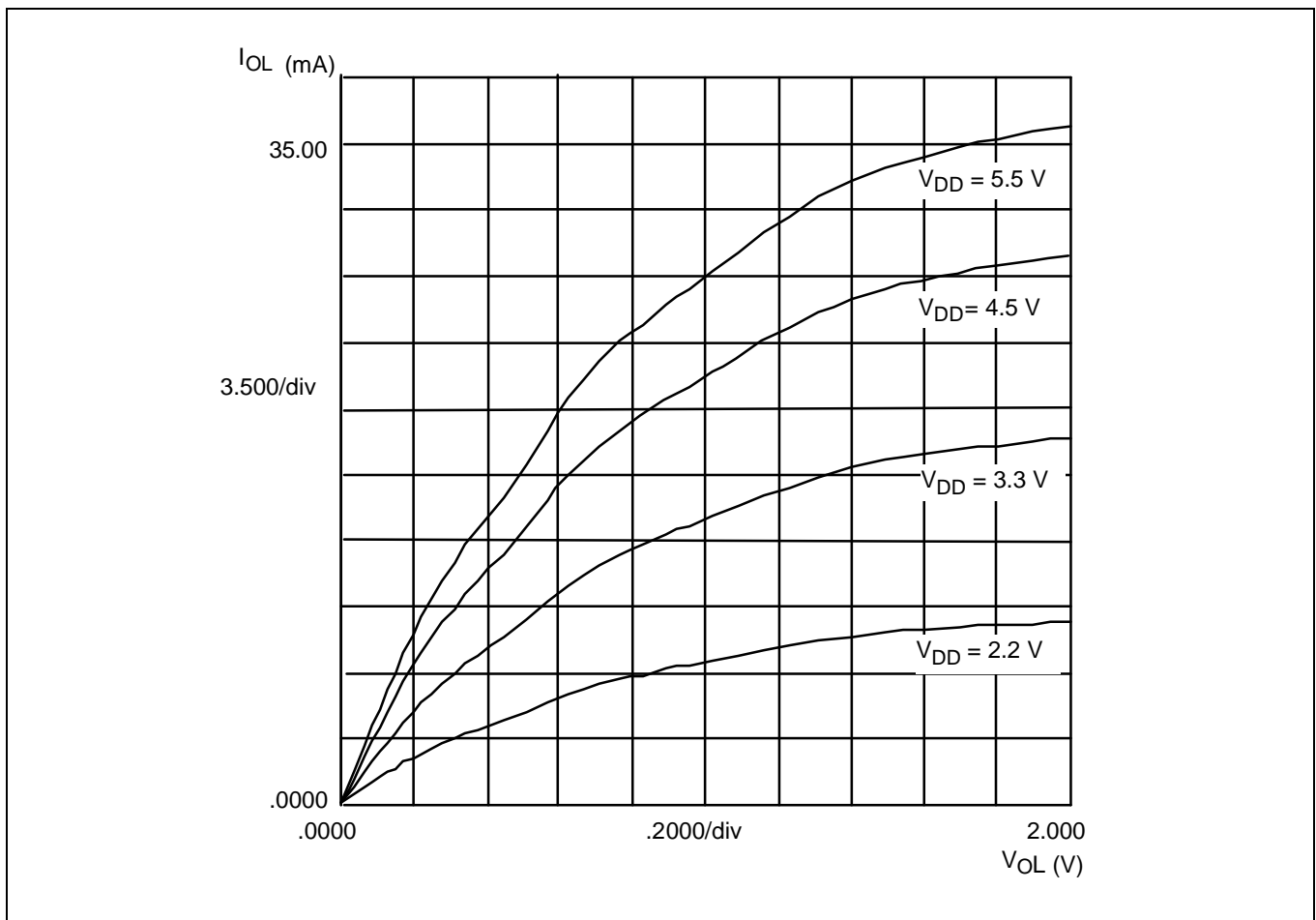


Figure 15-2. Standard Operating Voltage Range

Figure 15-3. Port 2  $I_{OL}$  vs  $V_{OL}$  Curve