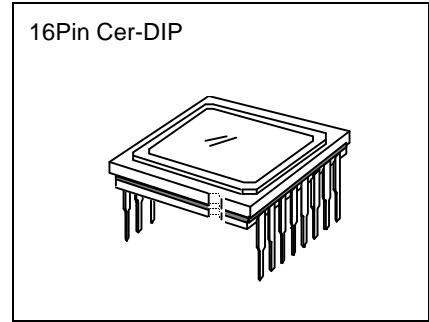


INTRODUCTION

The S5F325NU02 is an interline transfer CCD area image sensor developed for EIA 1/3 inch optical format video cameras, surveillance cameras, object detectors and image pattern recognizers. High sensitivity is achieved through the on-chip micro lenses and HAD (Hole Accumulated Diode) photosensors. This chip features a field integration read out system and an electronic shutter with variable charge storage time.



FEATURES

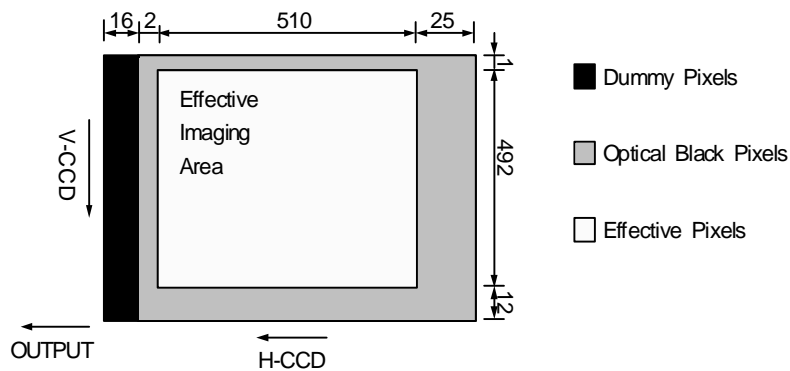
- High Sensitivity
- Optical Size 1/3 inch Format
- Low Dark Current
- Horizontal Register 5V Drive
- 16pin Ceramic DIP Package
- Field Integration Read Out System
- No DC Bias on Reset Gate

ORDERING INFORMATION

| Device | Package | Operating |
|-----------------|-----------------|-----------------|
| S5F325NU02-LAB0 | 16Pin Cer - DIP | -10 °C – +60 °C |

STRUCTURE

- Number of Total Pixels: 537(H) × 505(V)
- Number of Effective Pixels: 510(H) × 492(V)
- Chip Size: 6.00mm(H) × 4.95mm(V)
- Unit Pixel Size: 9.60 μm(H) × 7.50 μm(V)
- Optical Blacks & Dummies: Refer to Figure Below
Vertical 1 Line (Even Field Only)



BLOCK DIAGRAM

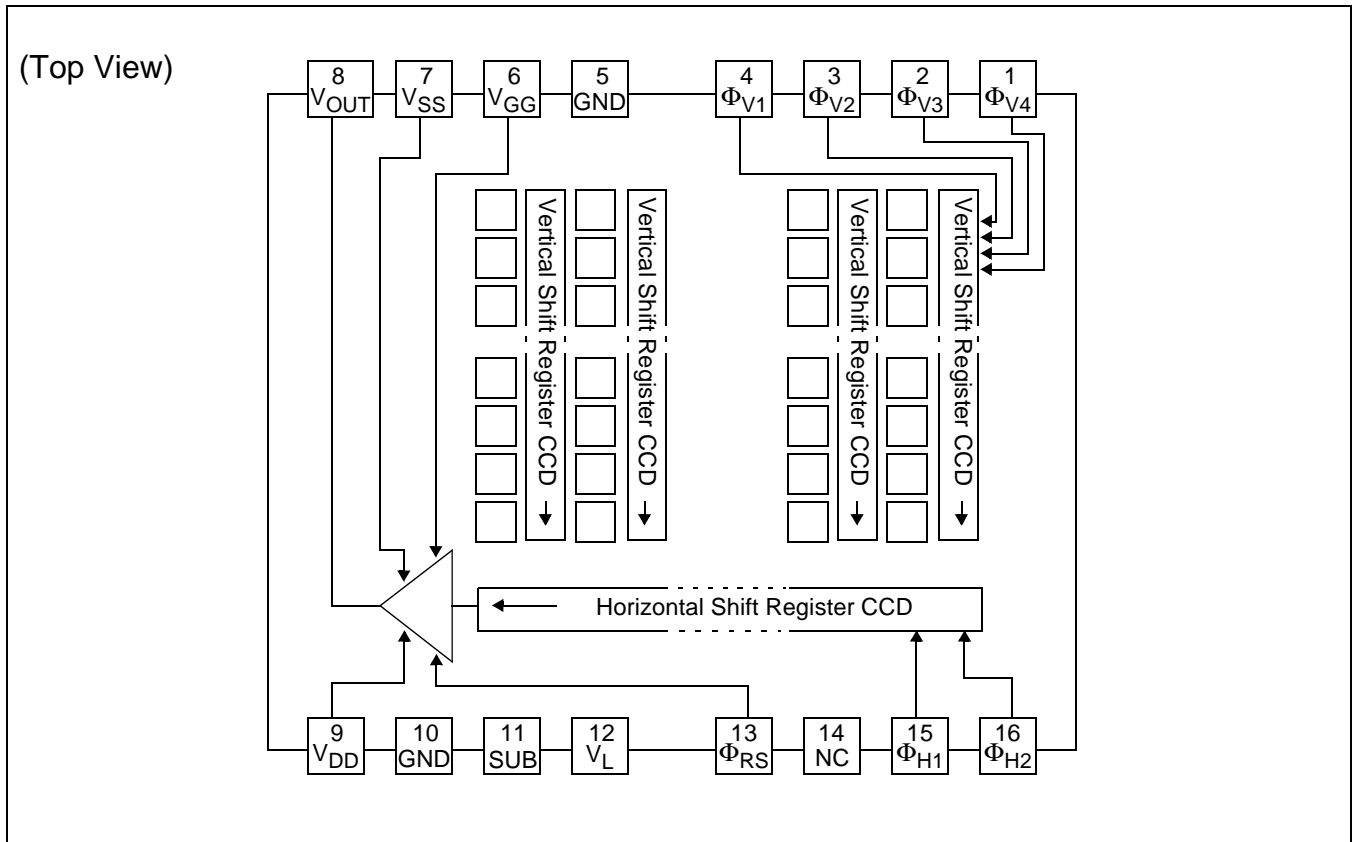


Figure 1. Block Diagram

PIN DESCRIPTION

Table 1. Pin Description

| Pin | Symbol | Description | Pin | Symbol | Description |
|-----|-------------|-------------------------------|-----|-------------|---------------------------------|
| 1 | Φ_{V4} | Vertical CCD transfer clock 4 | 9 | V_{DD} | Output stage drain bias |
| 2 | Φ_{V3} | Vertical CCD transfer clock 3 | 10 | GND | Ground |
| 3 | Φ_{V2} | Vertical CCD transfer clock 2 | 11 | SUB | Substrate bias |
| 4 | Φ_{V1} | Vertical CCD transfer clock 1 | 12 | V_L | Protection circuit bias |
| 5 | GND | Ground | 13 | Φ_{RS} | Charge reset clock |
| 6 | V_{GG} | Output stage gate bias | 14 | NC | No connection |
| 7 | V_{SS} | Output stage source bias | 15 | Φ_{H1} | Horizontal CCD transfer clock 1 |
| 8 | V_{OUT} | Signal output | 16 | Φ_{H2} | Horizontal CCD transfer clock 2 |

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾**Table 2. Absolute Maximum Ratings**

| Characteristics | Symbols | Min. | Max. | Unit |
|---|--|------|-------------------|------|
| Substrate voltage | SUB - GND | -0.3 | 55 | V |
| Supply voltage | $V_{DD}, V_{OUT}, V_{SS} - GND$ | -0.3 | 18 | V |
| | $V_{DD}, V_{OUT}, V_{SS} - SUB$ | -55 | 10 | V |
| Vertical clock input voltage | $\Phi_{V1}, \Phi_{V2}, \Phi_{V3}, \Phi_{V4} - GND$ | -10 | 20 | V |
| | $\Phi_{V1}, \Phi_{V2}, \Phi_{V3}, \Phi_{V4} - V_L$ | -0.3 | 30 | V |
| | $\Phi_{V1}, \Phi_{V2}, \Phi_{V3}, \Phi_{V4} - SUB$ | -55 | 10 | V |
| Horizontal clock input voltage | $\Phi_{H1}, \Phi_{H2} - GND$ | -0.3 | 10 | V |
| | $\Phi_{H1}, \Phi_{H2} - SUB$ | -55 | 17 | V |
| Voltage difference between vertical and horizontal clock input pins | $\Phi_{V1}, \Phi_{V2}, \Phi_{V3}, \Phi_{V4}$ | | 15 | V |
| | | | 27 ⁽²⁾ | V |
| | Φ_{H1}, Φ_{H2} | | 17 | V |
| | $\Phi_{H1}, \Phi_{H2} - \Phi_{V4}$ | -17 | 17 | V |
| Output clock input voltage | $\Phi_{RS}, V_{GG} - GND$ | -0.3 | 15 | V |
| | $\Phi_{RS}, V_{GG} - SUB$ | -55 | 10 | V |
| Protection circuit bias voltage | $V_L - SUB$ | -55 | 10 | V |
| Operating temperature | T_{OP} | -10 | 60 | °C |
| Storage temperature | T_{STG} | -30 | 80 | °C |

NOTES:

1. The device can be destroyed, if the applied voltage or temperature is higher than the absolute maximum rating voltage or temperature.
2. When the clock width is less than 10 μ sec and the clock duty factor is less than 0.1%.

DC CHARACTERISTICS

Table 3. DC Characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|--|------------------|---------------------------------|------|-------|------|--------|
| Output stage drain bias | V_{DD} | 14.55 | 15.0 | 15.45 | V | |
| Output stage gate voltage | V_{GG} | 1.75 | 2.0 | 2.25 | V | |
| Output stage source voltage | V_{SS} | Ground through 680Ω | | | V | ±5% |
| Substrate voltage adjustment range | V_{SUB} | 7.0 | | 14.5 | V | |
| Fluctuation voltage range after substrate voltage adjusted | ΔV_{SUB} | -3 | | 3 | % | |
| Protection circuit bias voltage | V_L | The lowest vertical clock level | | | | |
| Output stage drain current | I_{DD} | | 2.5 | | mA | |

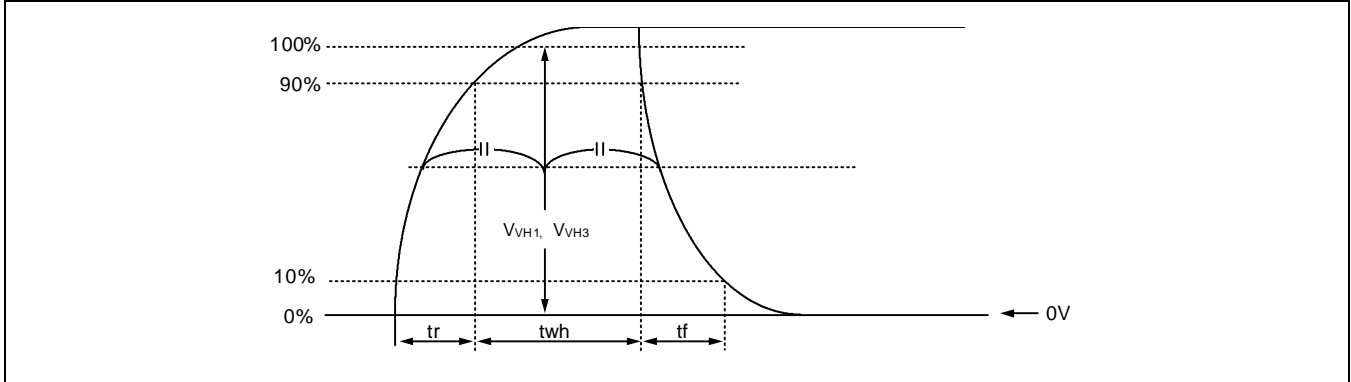
CLOCK VOLTAGE CONDITIONS

Table 4. Clock Voltage Conditions

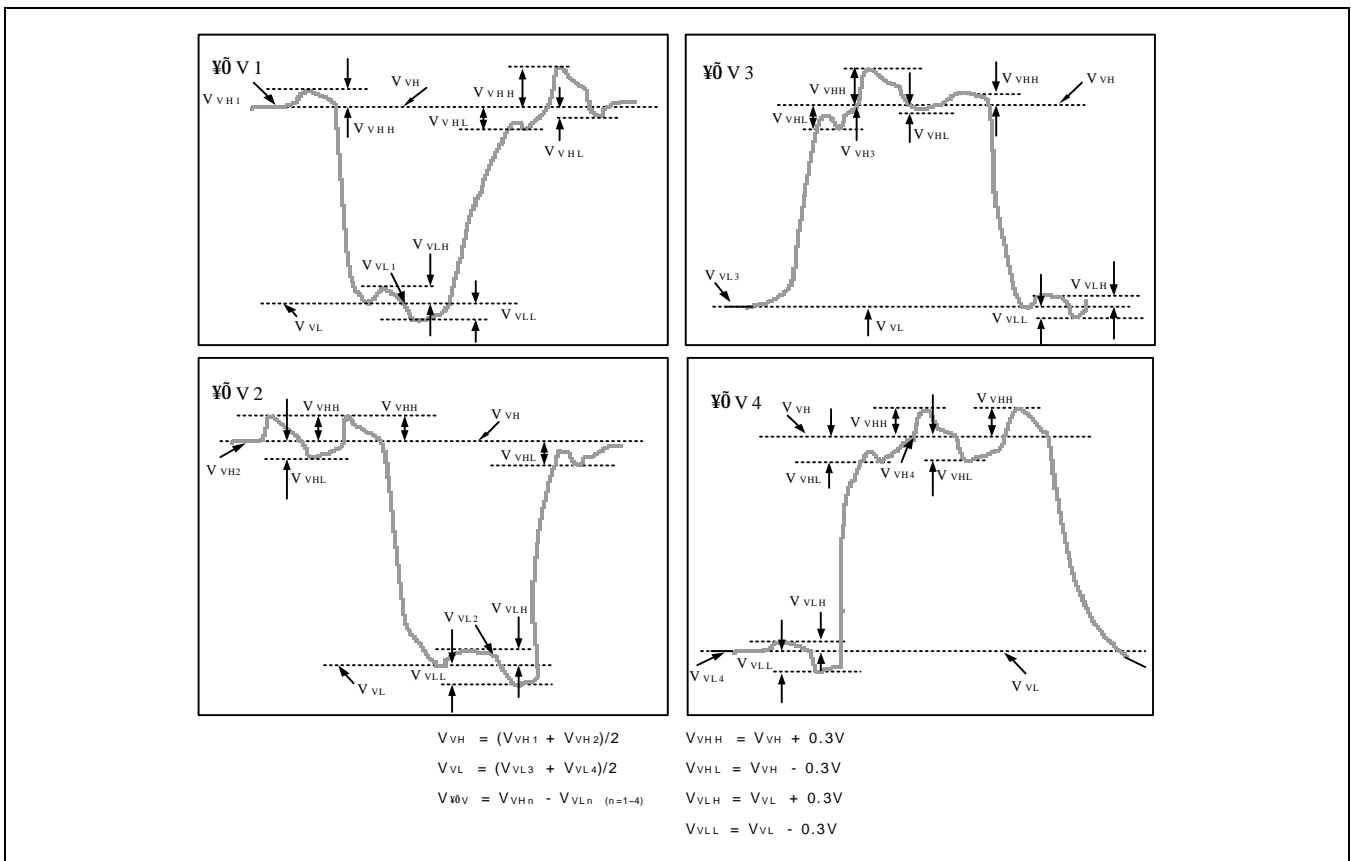
| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-----------------------------------|------------------------|-------|------|-------|------|------------|
| Read-out clock voltage | V_{VH1}, V_{VH3} | 14.55 | 15.0 | 15.45 | V | High level |
| Vertical transfer clock voltage | $V_{VM1} \sim V_{VM4}$ | -0.2 | 0.0 | 0.2 | V | Middle |
| | $V_{VL1} \sim V_{VL4}$ | -9.5 | -9.0 | -8.5 | V | Low |
| Horizontal transfer clock voltage | V_{HH1}, V_{HH2} | 4.75 | 5.0 | 5.25 | V | High |
| | V_{HL1}, V_{HL2} | -0.2 | 0.0 | 0.2 | V | Low |
| Charge reset clock voltage | V_{RSH} | 4.75 | 5.0 | 5.25 | V | High |
| | V_{RSL} | -0.2 | 0.0 | 0.2 | V | Low |
| Substrate clock voltage | $V_{\phi SUB}$ | 20 | 23.0 | 25 | V | Shutter |

DRIVE CLOCK WAVEFORM CONDITIONS

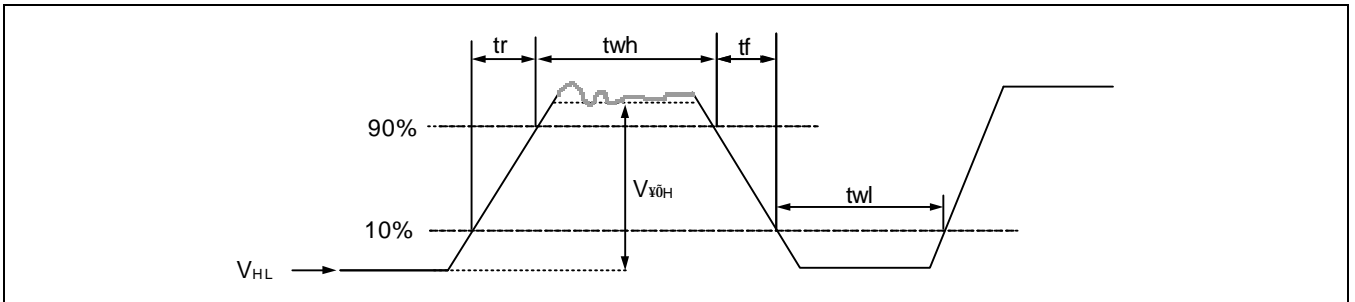
Read Out Clock Waveform



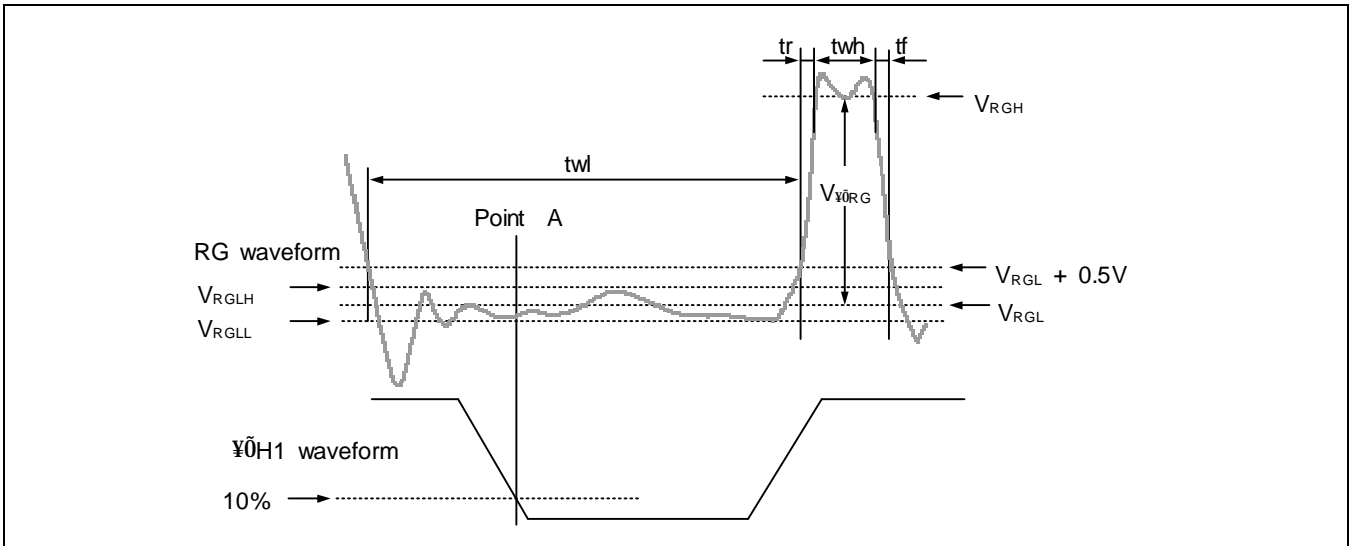
Vertical Transfer Clock Waveform



Horizontal Transfer Clock Waveform Diagram



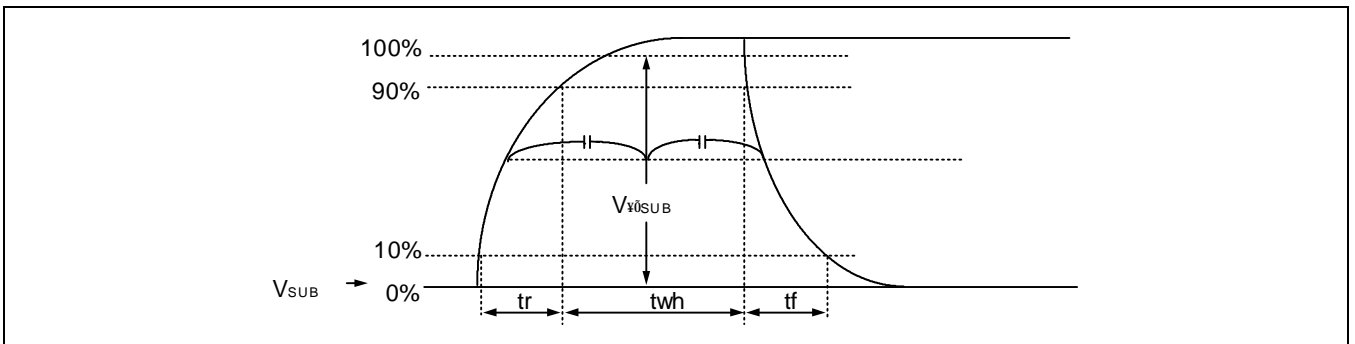
Reset Gate Clock Waveform Diagram



V_{RGLH} is the maximum value and V_{RGL} is the minimum value of the coupling waveform in the period from Point A in the diagram about to R_G rise

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2, V_{FRG} = V_{RGH} - V_{RGL}$$

Substrate Clock Waveform



CLOCK EQUIVALENT CIRCUIT CONSTANT

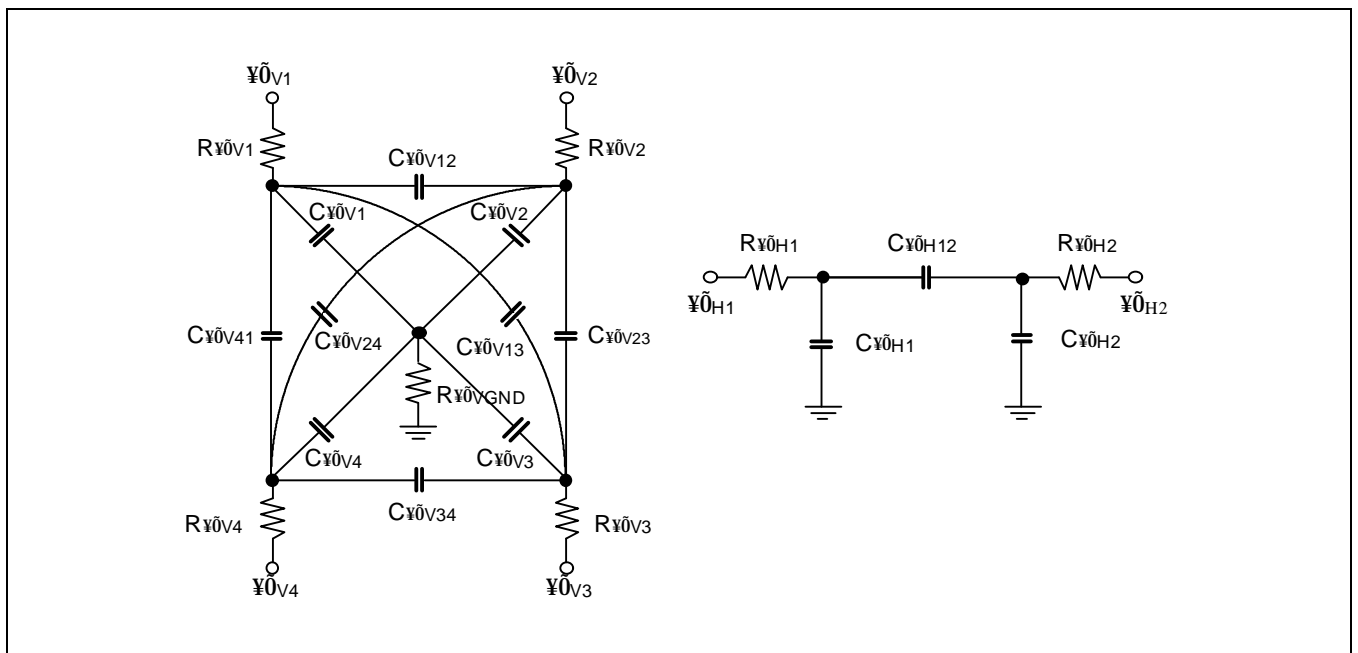
Table 5. Clock Equivalent Circuit Constant

| Item | Symbol | twh | | | twl | | | tr | | | tf | | | Unit |
|------------------|--|------|------|------|------|------|------|------|------|------|------|------|------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Read-out clock | Φ_{VH} | | 2.5 | | | | | | 0.5 | | | 0.5 | | μ s |
| Vertical clock | Φ_{V1}, Φ_{V2} Φ_{V3}, Φ_{V4} | | | | | | | | | | 15 | | 250 | ns |
| Horizontal clock | Φ_{H1} | 37 | 41 | | 38 | 42 | | | 12 | 15 | | 10 | 15 | ns |
| | Φ_{H2} | 37 | 41 | | 38 | 42 | | | 12 | 15 | | 10 | 15 | ns |
| Reset clock | Φ_{RG} | 11 | 15 | | 75 | 79 | | | 6.5 | | | 4.5 | | ns |
| Substrate clock | Φ_{SUB} | 1.5 | 2.0 | | | | | | | 0.5 | | | 0.5 | μ s |

EQUIVALENT CIRCUIT PARAMETERS

Table 6. Equivalent Circuit Parameters

| Item | Symbol | Typ. | Unit | Remark |
|---|--------------------------------|-------|----------|--------|
| Capacitance between vertical transfer clock and GND | $C_{\Phi V1}, C_{\Phi V3}$ | 1,300 | pF | |
| | $C_{\Phi V2}, C_{\Phi V4}$ | 1,300 | pF | |
| Capacitance between vertical transfer clocks | $C_{\Phi V12}, C_{\Phi V34}$ | 600 | pF | |
| | $C_{\Phi V23}, C_{\Phi V41}$ | 230 | pF | |
| | $C_{\Phi V13}$ | 120 | pF | |
| | $C_{\Phi V24}$ | 90 | pF | |
| Capacitance between horizontal transfer clock and GND | $C_{\Phi H1}, C_{\Phi H2}$ | 38 | pF | |
| Capacitance between horizontal transfer clocks | $C_{\Phi H12}$ | 38 | pF | |
| Capacitance between substrate clock and GND | $C_{\Phi SUB}$ | 1120 | pF | |
| Vertical transfer clock serial resistor | $R_{\Phi V1} \sim R_{\Phi V4}$ | 40 | Ω | |
| Vertical transfer clock ground resistor | $R_{\Phi VGND}$ | 15 | Ω | |
| Horizontal transfer clock serial resistor | $R_{\Phi H1}, R_{\Phi H2}$ | 10 | Ω | |
| Reset gate clock serial resistor | $R_{\Phi RS}$ | 100 | Ω | |



OPERATING CHARACTERISTICS

Device Temperature = 25 °C

Table 7. Operating Characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------|------------|-------|-------|-------|--------|--------|
| Sensitivity | S | 95 | 105 | | mV/lux | 1 |
| Saturation signal | Y_{SAT} | 600 | | | mV | 2 |
| Smear | SM | | 0.007 | 0.015 | % | 3 |
| Blooming margin | BM | 1,000 | | | times | 4 |
| Uniformity | U | | | 20 | % | 5 |
| Dark signal (NOTE) | D | | | 2 | mV | 6 |
| Dark shading (NOTE) | ΔD | | | 2 | mV | 7 |
| Image lag | Y_{LAG} | | | 0.5 | % | 8 |
| Flicker | F_Y | | | 1 | % | 9 |

NOTE: Test Temperature = 60 °C

TEST CONDITION

1. Use a light source with color temperature of 3,200K hallogen lamp and CM-500S for IR cut filter.
The light source is adjusted in accordance with the average value of Y signals indicated in each item.
2. Through the following tests the substrate voltage should be set to the value while the device condition should be kept within the range of the bias and clock conditions.

TEST METHODS

1. Measure the light intensities (L) when the averaged illuminance output value (Y) is the standard illuminance output value, 150mV (Y_A) and when half of 150mV ($1/2 Y_A$).

$$S = \frac{Y_A - \frac{1}{2}Y_A}{L_{Y_A} - L_{\frac{1}{2}Y_A}}$$

2. Adjust the light intensity to 15 times of the value with which Y is Y_A , then measure the averaged illuminance output value ($Y = Y_{SAT}$).

3. Adjust the light intensity to 500 times of the value with which Y is Y_A , then remove the read-out clock and drain the signal in photosensors by the electronic shutter operation in all the respective horizontal blanking times with the other clocks unchanged. Measure the maximum illuminance output value (Y_{SM}).

$$SM = \frac{Y_{SM}}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100(\%)$$

4. Adjust the light intensity to 1,000 times of the value with which Y is Y_A , then inspect whether there is blooming phenomenon or not.

5. Measure the maximum and minimum illuminance output value (Y_{MAX} , Y_{MIN}) when the light intensity is adjusted to make Y to be Y_A .

$$U = \frac{Y_{MAX} - Y_{MIN}}{Y_A} \times 100(\%)$$

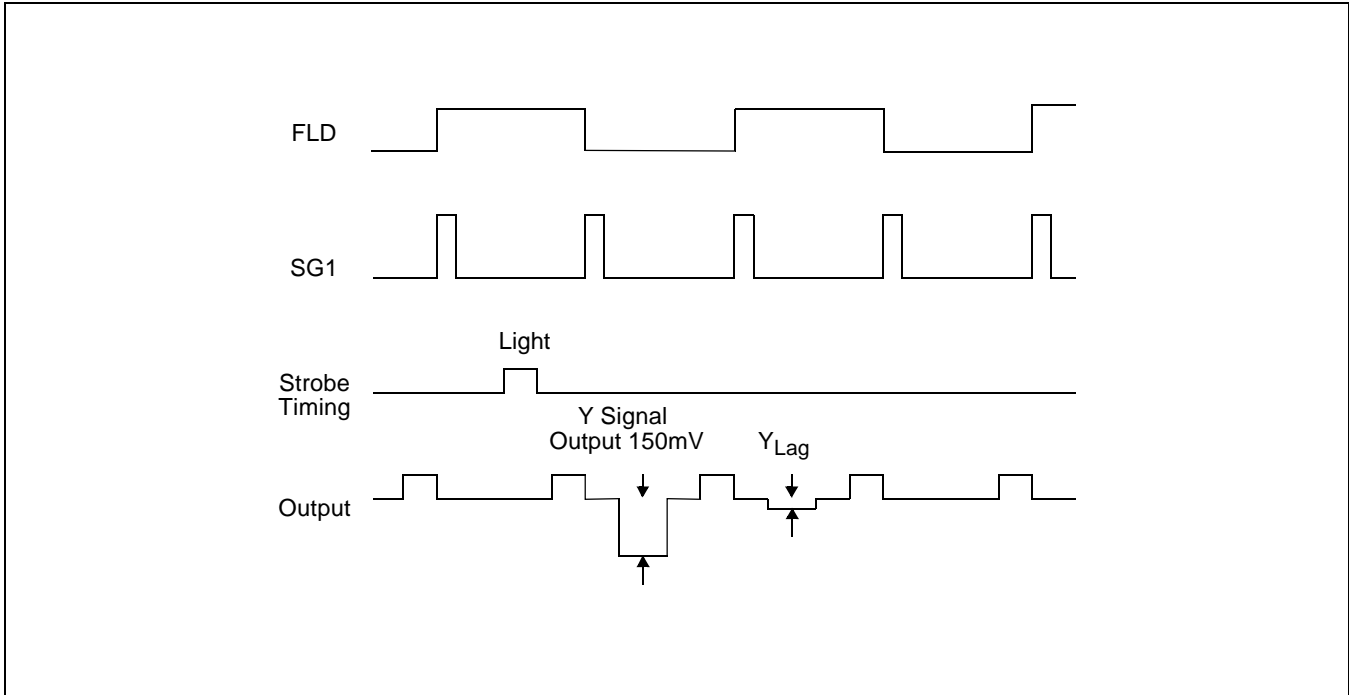
6. Measure Y_D with the horizontal idling time transfer level as reference, when the device ambient temperature is 60 °C and all of the light sources are shielded.

7. Follow test method 6, measure the maximum (D_{MAX}) and minimum illuminance output (D_{MIN}).

$$\Delta D = D_{MAX} - D_{MIN}$$

8. Adjust the light intensity of Y signal output value by strobe light to 150mV (Y_A), calculate by below formula with measuring the image lag signal which is generated by below timing diagram.

$$Y_{LAG} = (Y_{lag}/150) \times 100(\%)$$



9. Adjust the light intensity of Y signal average value to 150mV (Y_A), calculate by below formula with measuring the signal differences (ΔY_f [mV]) between fields.

$$F_Y = (\Delta Y_f / Y_A) \times 100(\%)$$

SPECTRAL RESPONSE CHARACTERISTICS

Excluding Light Source Characteristics

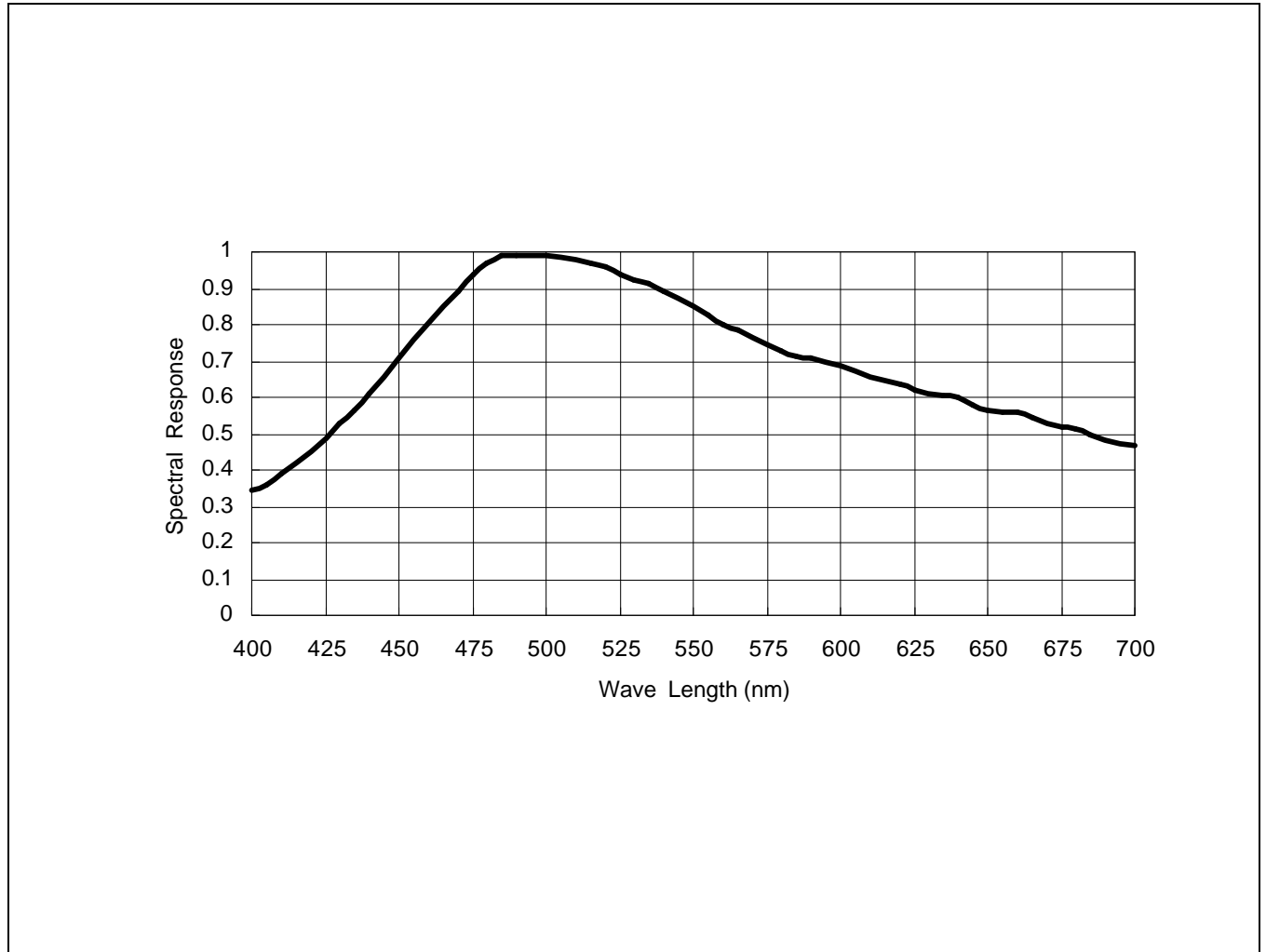


Figure 2. Spectral Response Characteristics

APPLICATION CIRCUITS

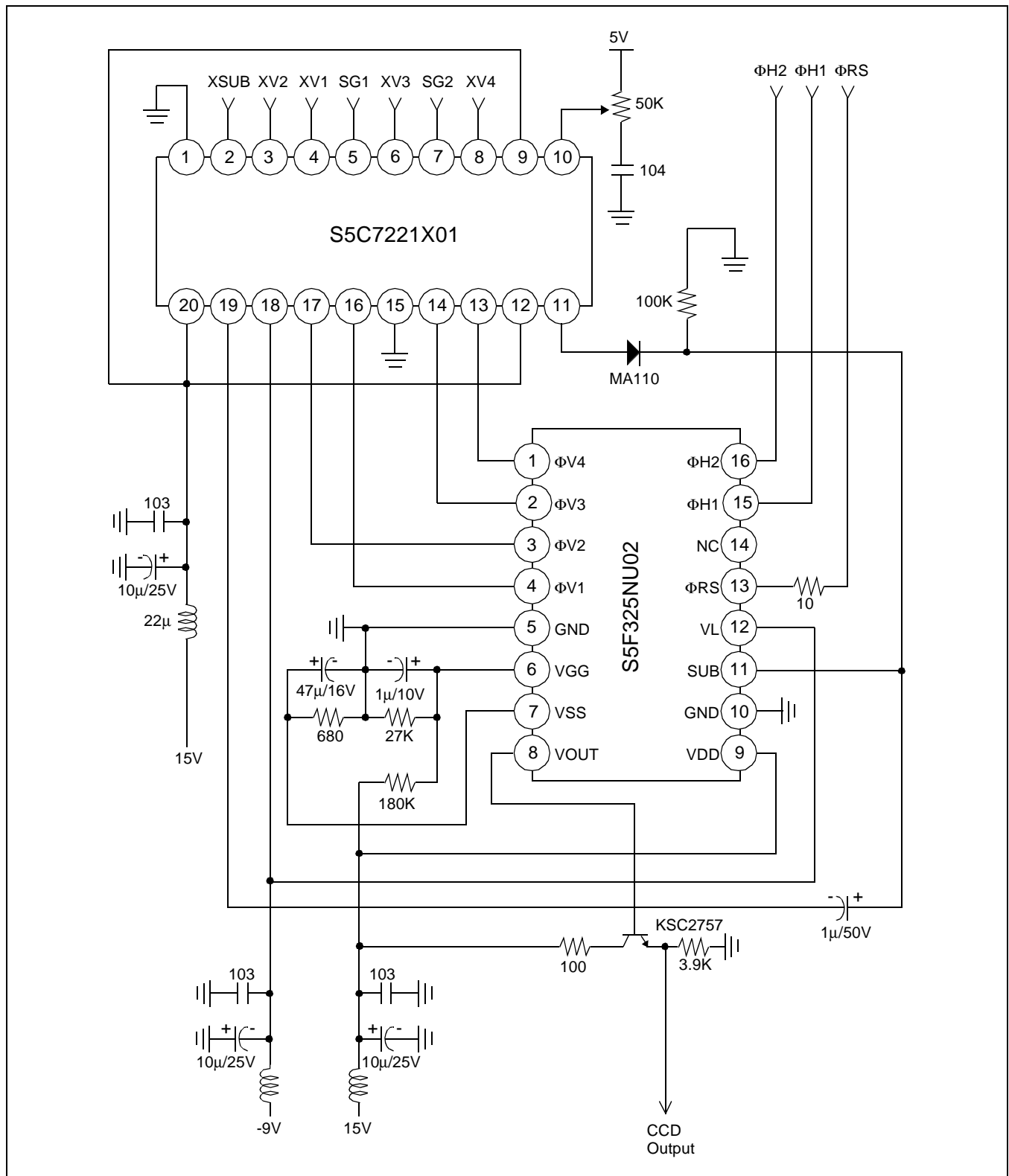


Figure 3. Application Circuits

READ-OUT CLOCK TIMING CHART

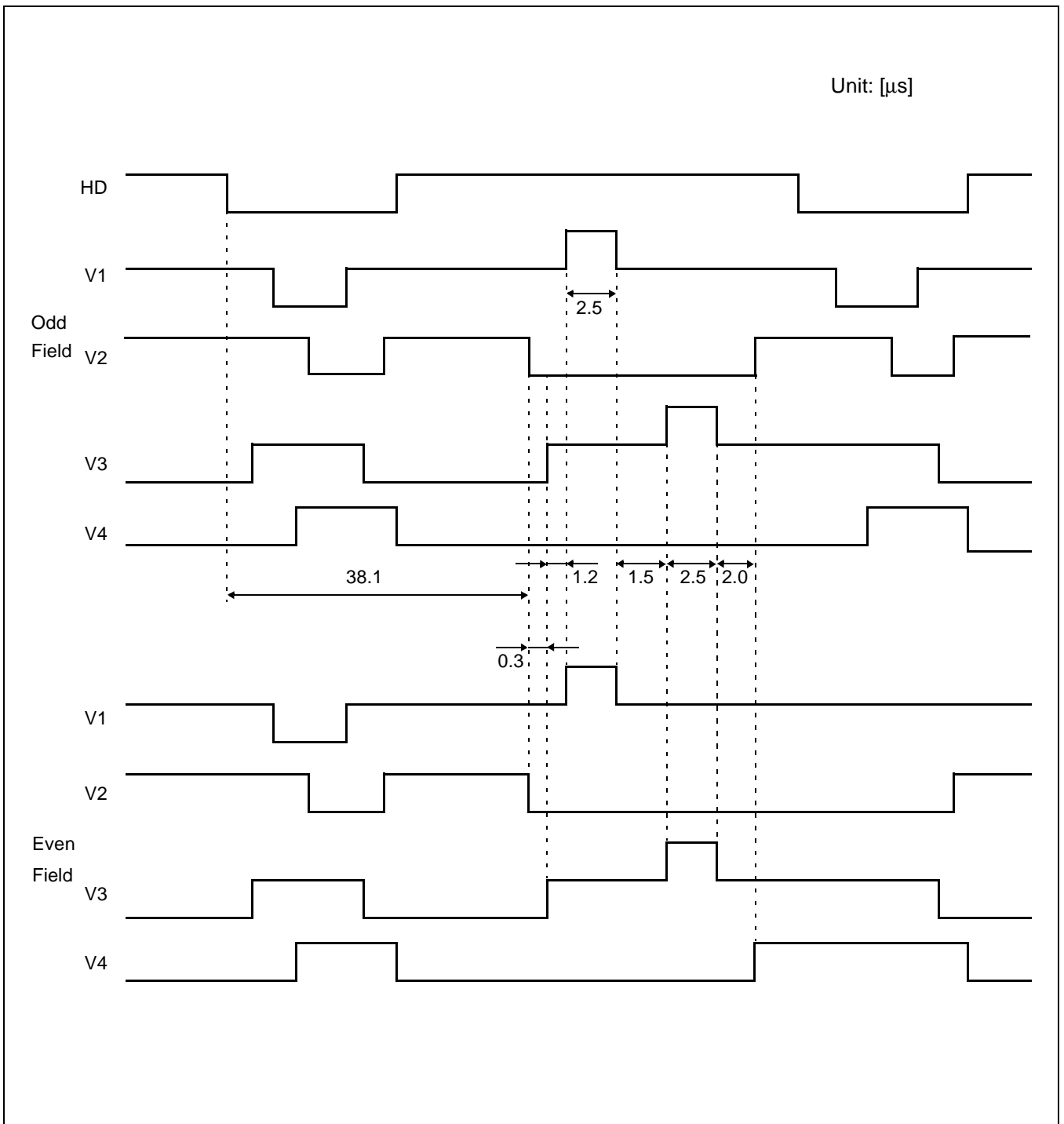


Figure 4. Read-out Clock Timing Chart

CLOCK TIMING CHART (VERTICAL SYNC.)

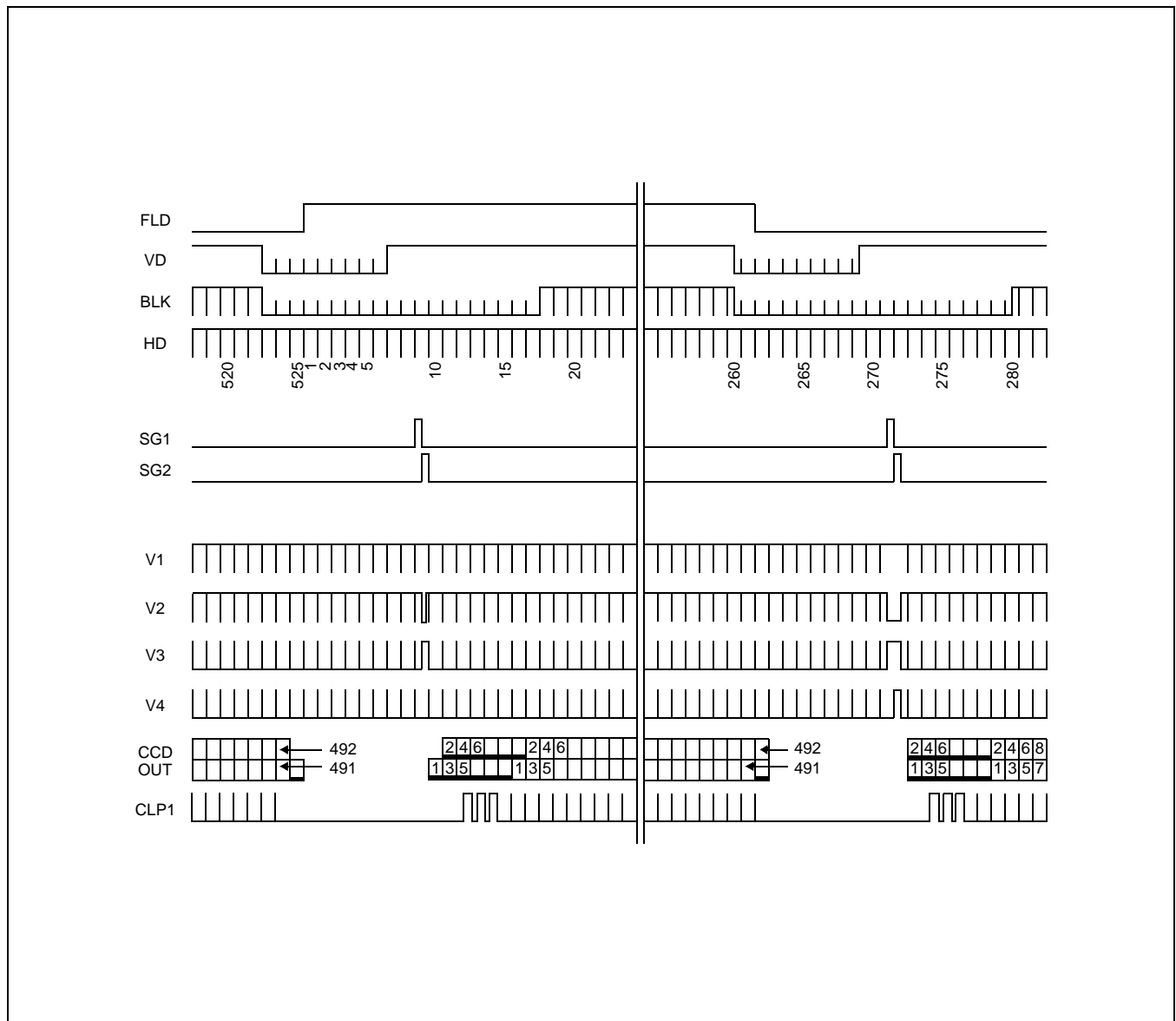


Figure 5. Clock Timing Chart (Vertical Sync.)

CLOCK TIMING CHART (HORIZONTAL SYNC.)

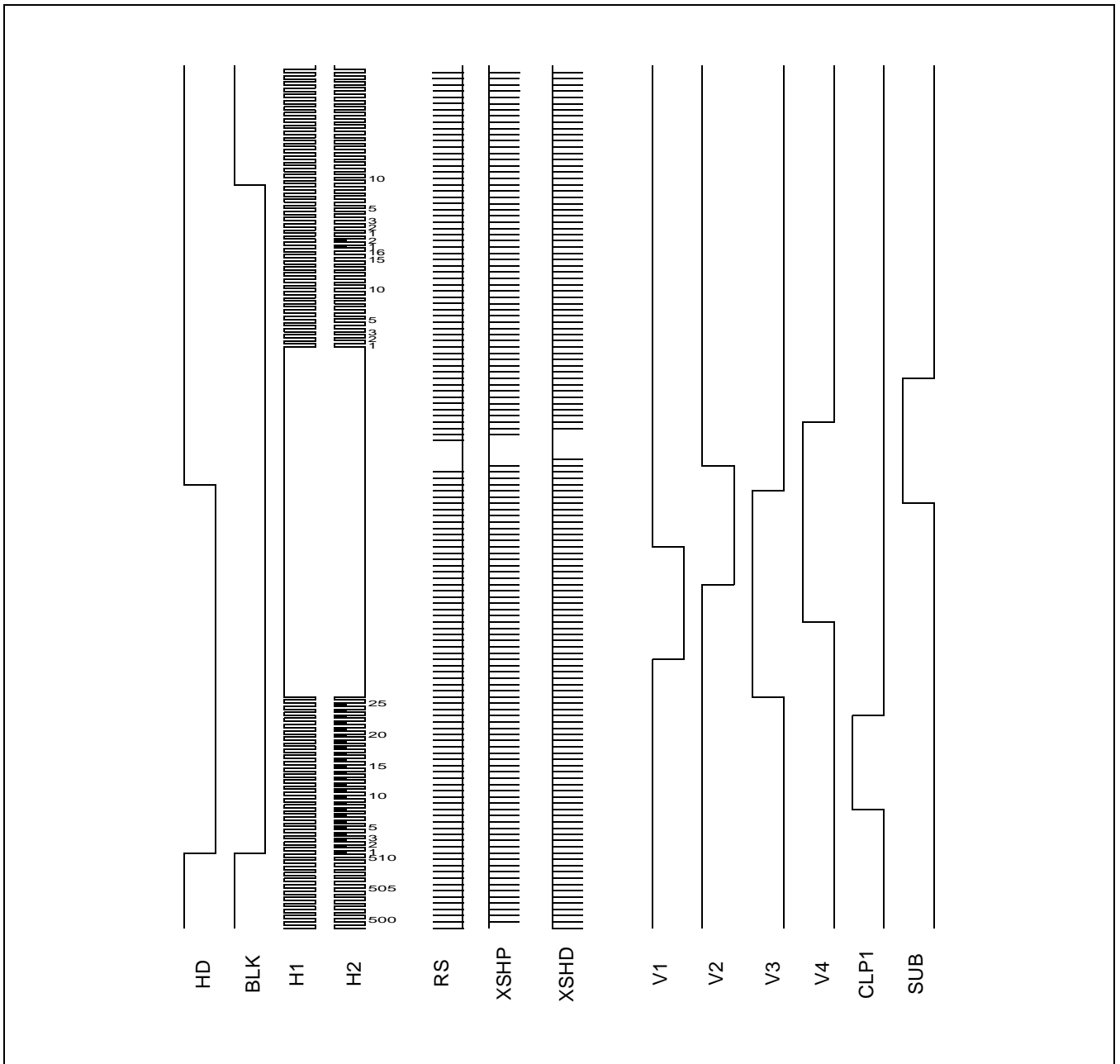


Figure 6. Clock Timing Chart (Horizontal Sync.)

PACKAGE DIMENSIONS

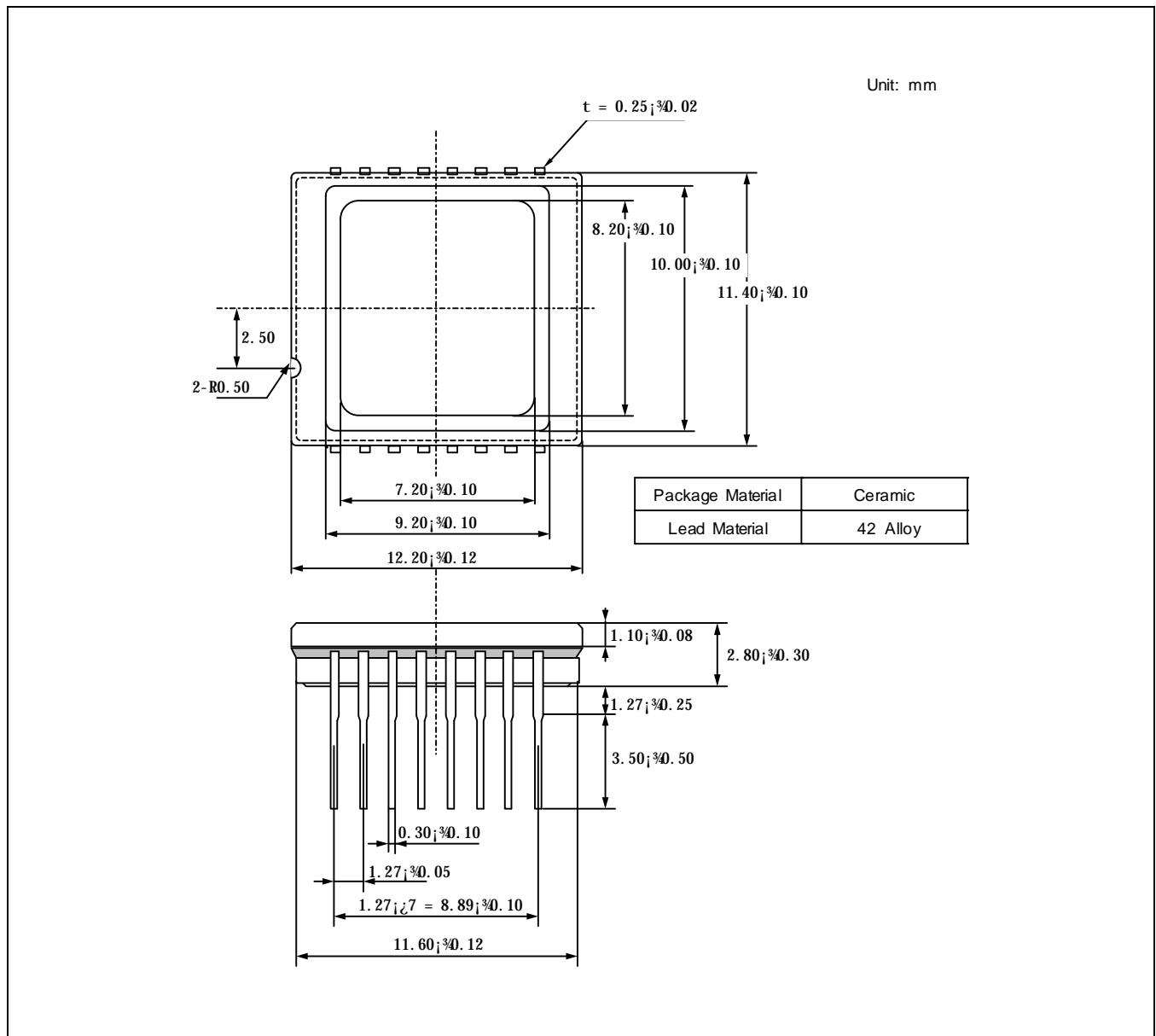


Figure 7. Package Dimensions

HANDLING INSTRUCTIONS

- **Static Charge Prevention**

CCD image sensors can be easily damaged by static discharge. Before handling, be sure to take the following protective measures.

 - Use non chargeable gloves, clothes or material. Also use conductive shoes.
 - When handling directly, use an earth band.
 - Install a conductive mat on the floor or working table to prevent generation of static electricity.
 - Ionized air is recommended for discharging when handling CCD image sensor.
 - For the shipment of mounted substrates, use boxes treated for the prevention of static charges.
- **Soldering**
 - Make sure the package temperature does not exceed 80 °C.
 - Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
 - To dismount an imaging device, do not use a solder suction equipment. When using an electronic desoldering tool, use a thermal controller of the zero cross on/off type and connect to ground.
- **Dust and Dirt Protection**
 - Operate in the clean environments (around class 1000 will be appropriate).
 - Do not either touch glass plates by hand or have object come in contact with glass surface. Should dirt stick to a glass surface blow it off with an air blow(for dirt stuck through static electricity ionized air is recommended).
 - Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
 - Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
 - When a protective tape is applied before shipping, just before use remove the tape applied electrostatic protection. Do not reuse the tape.
- Do not expose to strong light (sun rays) for long period, color filter are discolored.
- Exposure to high temperature or humidity will affect the characteristics. accordingly avoid storage or usage in such conditions.
- CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.