INTRODUCTION

KS1454 is a DVDP (Digital Video Disc Player) 1-chip LSI which includes the digital servo and DSP(Digital Signal Processor) features.
Servo Block performs the digital servo function, which controls disc speed and pick-up location as it retrieves signals from the disc (CD,VCD,DVD). Servo block contains the wide capture PLL.
DSP block receives the EFM signal as an input and performs buffer control for demodulated data output while EFM demodulation and error corrections are being carried out.

FEATURES

MICOM

— 8bit parallel interface

— Built-in direct memory access (DVD/CD)

PLL

— Built-in wide capture range (± 50%) PLL

— Built-in EFM slice

— Built-in F/V converter for RF EQ adjustment of DAC method

— Charge-pump PWM control method

— FD/PD gain adjustment

— Built-in wide range VCO(20 - 100MHz)

SERVO

— CD/CD-ROM 1,2x, DVD 1x compatible digital servo IC.

— complete automatic adjusting FEATURE.
(Focus/Tracking Loop's Input Gain, Offset, Balance, Loop Gain)

— Each servo loop has a digital filter, reducing the number of external parts.

— Built-in AGC FEATURE that responds optimally to various disc types.

— High speed moving control(built-in SLED FG Encoder).

— Built-in speed controlling search algorithm.

— Built-in 10bit A/D Converter and 10bit D/A Converter.

— Various filter characteristics and internal constants can be set from MICOM.

— Built-in defect and shock response.

— Built-in 16bit track counter.

— Chooses the best method from multiple search algorithm.

— Servo operation improved by widening the range through high speed sampling of 151.2kHz

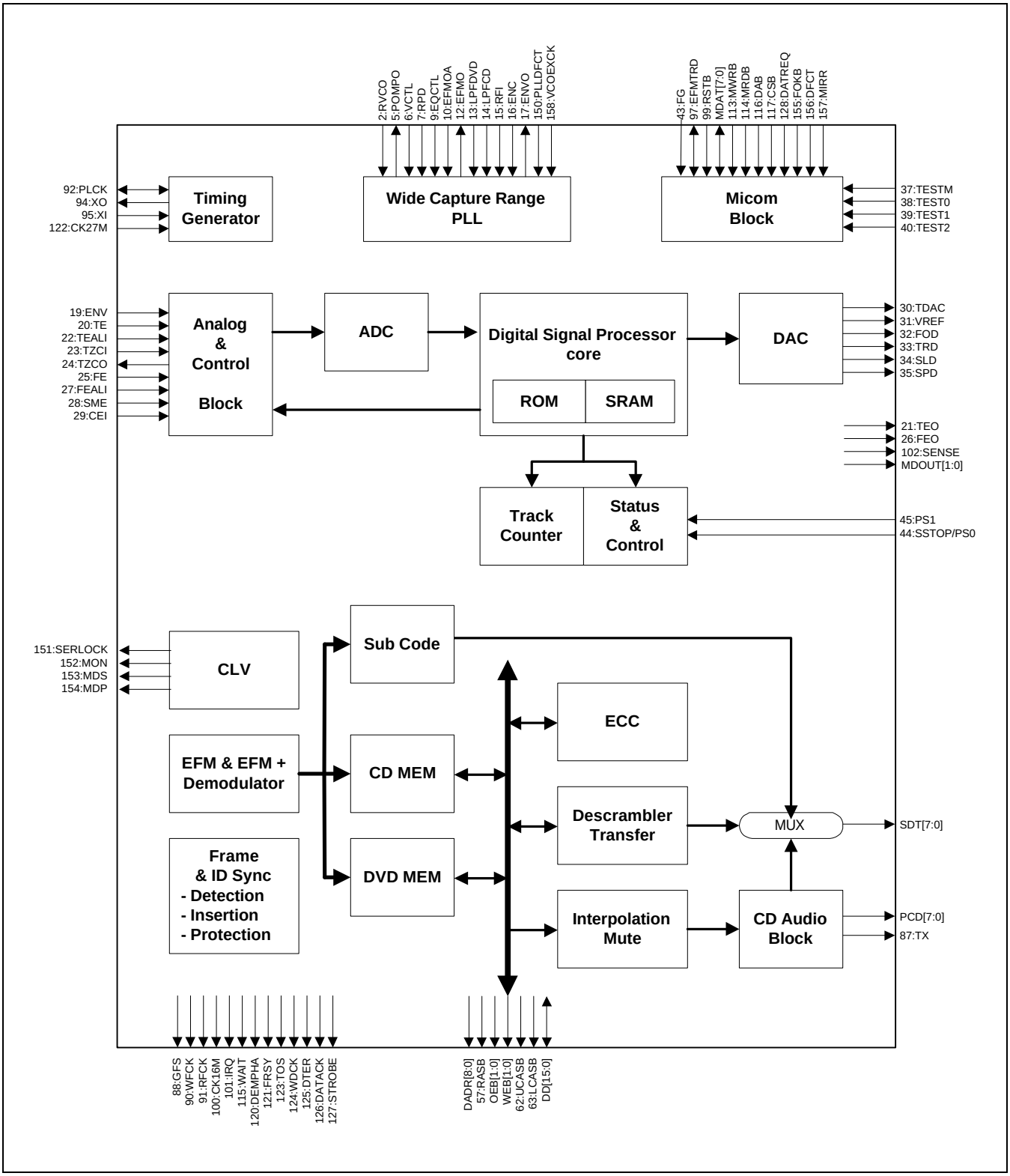
DSP

- External PLCK input (in Test mode)
- EFM/EFM+ demodulator
- Sync protection/insertion
- CIRC/RS-PC Error correction (4/16 Erasure Correction)
- 4-16 MBits DRAM interface
  (external component for error correction/Track Buffer)
- Descramble
- ID Error correction
- Main data error detection(EDC)
- DSI detection and DSI data output
- A/V Decoder Parallel Interface
- Built-in CD-DA Decoder
- Subcode data serial output
- Spindle servo control signal generation
- DVD/CD/VCD playback
- CD data serial/parallel output
- CLV feature
- CD/VCD repeat correction feature

TECHNOLOGY

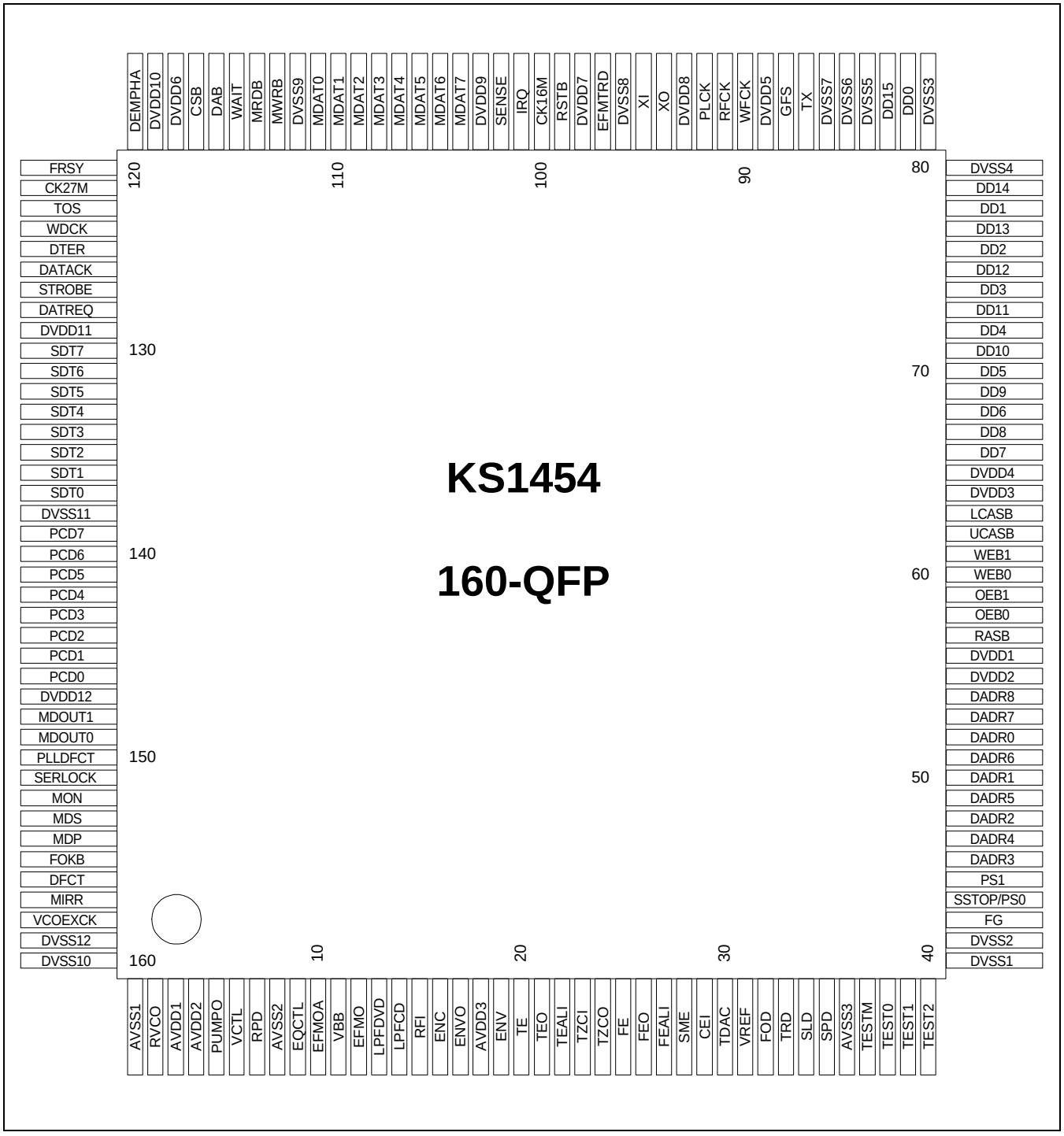
- Internal 3.3V operation and 3.3V external interface. (Analog Block)
- Internal 3.3V operation and 5V external interface. (Digital Block)
- Package 160-QFP

BLOCK DIAGRAM



PIN DIAGRAM & PIN DISCRIPTION

PIN DIAGRAM



PIN DESCRIPTION

Pin No.	Name	Interface	I/O	Description
1	AVSS1	Power	S	VSS for PLL Analog
2	RVCO	PLL	I	Register Pin for VCO Gain
3	AVDD1	Power	S	VDD for PLL Analog (3.3V)
4	AVDD2	Power	S	VDD for PLL VCO (3.3V)
5	PUMPO	PLL	O	Charge Pump Output
6	VCTL	PLL	I	Control Voltage for VCO
7	RPD	PLL	I	Gain Adjust Register for Phase Detector
8	AVSS2	Power	S	VSS for PLL VCO
9	EQCTL	Analog	O	EQ Control Signal
10	EFMOA	Analog	I	EFM Offset Adjustment
11	VBB	Power	S	Bulk Bias for PLL
12	EFMO	Analog	O	EFM Output Signal
13	LPFDVD	Analog	I	Asymmetric Input Signal for DVD
14	LPFCD	Analog	I	Asymmetric Input Signal for CD
15	RFI	RF	I	RF Input Signal
16	ENC	RF	I	RF Envelope DC Drawing Output
17	ENVO	RF	O	RF Envelope Detection Output
18	AVDD3	Power	S	VDD for Servo/ADC/DAC Analog (3.3v)
19	ENV	RF	I	RF Envelope Input
20	TE	RF	I	Tracking Error Signal Input
21	TEO	RF	O	TE AMP Output
22	TEALI	RF	I	TEO after Tracking Anti-aliasing Filter
23	TZCI	RF	I	TE Signal for Tracking Zero Cross Input
24	TZCO	RF	O	Tracking Zero Cross Output
25	FE	RF	I	Focus Error Signal Input
26	FEO	RF	O	FE AMP Output
27	FEALI	RF	I	FEO after Tracking Anti-aliasing Filter
28	SME	DSP	I	Spindle Error Input
29	CEI	RF	I	Center Position Servo Input
30	TDAC	Monitor	O	Servo RAM Monitor / Jump Pulse AREA Window Pulse Output
31	VREF	Driver	O	Reference Voltage Output
32	FOD	Driver	O	Focus Actuator Drive Signal Output
33	TRD	Driver	O	Tracking Actuator Drive Signal Output
34	SLD	Driver	O	Sled Motor Drive Signal Output
35	SPD	Driver	O	Spindle Motor Drive Signal Output
36	AVSS3	Power	S	VSS for Servo/ADC/DAC Analog
37	TESTM	TEST	I	Normal Play "Low"
38	TEST0	TEST	I	
39	TEST1	TEST	I	
40	TEST2	TEST	I	

Pin No.	Name	Interface	I/O	Description
41	DVSS1	Power	S	VSS for Digital Circuit
42	DVSS2	Power	S	VSS for Digital Circuit
43	FG	Driver	I	Reference Signal for CAV
44	SSTOP/PS0	Motor	I	Limit Switch / Sled Motor Position Sensor Input 0
45	PS1	Motor	I	Sled Motor Position Sensor Input 1
46	DADR3	DRAM	O	DRAM Address Bus
47	DADR4	DRAM	O	
48	DADR2	DRAM	O	
49	DADR5	DRAM	O	
50	DADR1	DRAM	O	
51	DADR6	DRAM	O	
52	DADR0	DRAM	O	
53	DADR7	DRAM	O	
54	DADR8	DRAM	O	
55	DVDD2	Power	S	VDD for Digital Circuit (3.3V)
56	DVDD1	Power	S	VDD for Digital Circuit (5V)
57	RASB	DRAM	O	DRAM Row Address Strobe
58	OEB0	DRAM	O	DRAM Output Enable 0
59	OEB1	DRAM	O	DRAM Output Enable 1 (DADR9 in 16M MODE)
60	WEB0	DRAM	O	DRAM Write Enable 0 (4M,8M,16M)
61	WEB1	DRAM	O	DRAM Write Enable 1 (8M ONLY)
62	UCASB	DRAM	O	DRAM Upper Column Address Strobe
63	LCASB	DRAM	O	DRAM Low Column Address Strobe
64	DVDD3	Power	S	VDD for Digital Circuit (5V)
65	DVDD4	Power	S	VDD for Digital Circuit (3.3V)
66	DD7	DRAM	B	DRAM Data Bus
67	DD8	DRAM	B	
68	DD6	DRAM	B	
69	DD9	DRAM	B	
70	DD5	DRAM	B	
71	DD10	DRAM	B	
72	DD4	DRAM	B	
73	DD11	DRAM	B	
74	DD3	DRAM	B	
75	DD12	DRAM	B	
76	DD2	DRAM	B	
77	DD13	DRAM	B	
78	DD1	DRAM	B	
79	DD14	DRAM	B	
80	DVSS4	Power	S	VSS for Digital Circuit

Pin No.	Name	Interface	I/O	Description
81	DVSS3	Power	S	VSS for Digital Circuit
82	DD0	DRAM	B	DRAM Data Bus
83	DD15	DRAM	B	
84	DVSS5	Power	S	VSS for Digital Circuit
85	DVSS6	Power	S	VSS for Digital Circuit
86	DVSS7	Power	S	VSS for Digital Circuit
87	TX	TX	O	Digital Output for Audio
88	GFS	Monitor	O	Good Frame Sync Detect State Output (O.K is "High")
89	DVDD5	Power	S	VDD for Digital Circuit (3.3V)
90	WFCK	Monitor	O	Write Frame Pulse
91	RFCK	Monitor	O	Reference Frame Pulse
92	PLCK	Monitor	B	EFM Data Recovery Clock
93	DVDD8	Power	S	VDD for Digital Circuit (3.3V)
94	XO	Clock	O	System Clock Signal Output
95	XI	Clock	I	System Clock Signal Input (33.8688MHz)
96	DVSS8	Power	S	VSS for Digital Circuit
97	EFMTRD	Monitor	B	Latched EFM Output Signal or external EFM Input Signal
98	DVDD7	Power	S	VDD for Digital Circuit (3.3V)
99	RSTB	MICOM	I	System Reset Signal Input
100	CK16M	Function	O	XI (pin 95) Devide Clock (16.9344MHz)
101	IRQ	MICOM	O	Interrupt Request for MICOM
102	SENSE	MICOM	O	Internal Status Monitor
103	DVDD9	Power	S	VDD for Digital Circuit (3.3V)
104	MDAT7	MICOM	B	MICOM Data Bus
105	MDAT6	MICOM	B	
106	MDAT5	MICOM	B	
107	MDAT4	MICOM	B	
108	MDAT3	MICOM	B	
109	MDAT2	MICOM	B	
110	MDAT1	MICOM	B	
111	MDAT0	MICOM	B	
112	DVSS9	Power	S	VSS for Digital Circuit
113	MWRB	MICOM	I	MICOM Write Clock Signal Input
114	MRDB	MICOM	I	MICOM Read Clock Signal Input
115	WAIT	MICOM	O	MICOM Read / Write Access Wait (when wait is "Low")
116	DAB	MICOM	I	MICOM DATA/ADDRS Select (H: Data, L: Address)
117	CSB	MICOM	I	MICOM Chip Select
118	DVDD6	Power	S	VDD for Digital Circuit (5V)
119	DVDD10	Power	S	VDD for Digital Circuit (5V)
120	DEMPHA	Audio DAC	O	De-emphasis (ON state is "High")

Pin No.	Name	Interface	I/O	Description
121	FRSY	MPEG	O	Frame Sync Output
122	CK27M	Clock	I	System Clock Input for 26.16MHz
123	TOS	MPEG	O	Top of Sector
124	WDCK	MPEG	O	Word Data Clock
125	DTER	MPEG	O	DVD Data Error Output
126	DATACK	MPEG	O	Data Acknowledge Signal Output
127	STROBE	MPEG	O	Data Strobe (Clock) Output
128	DATREQ	MPEG	I	Data Request Form A/V Decoder or ROM Decoder
129	DVDD11	Power	S	VDD for Digital Circuit (3.3V)
130	SDT7	MPEG	B	DVD DATA7 / Subcode Serial Clock (SBCK)
131	SDT6	MPEG	O	DVD DATA6 / Subcode Block Sync (S0S1)
132	SDT5	MPEG	O	DVD DATA5 / Subcode Frame Sync (WFSY)
133	SDT4	MPEG	O	DVD DATA4 / Subcode Serial Data (SBDT)
134	SDT3	MPEG	O	DVD DATA3 / CD DATA Error-Flag (C2P0)
135	SDT2	MPEG	O	DVD DATA2 / CD DATA Bit-Clock (BLCK)
136	SDT1	MPEG	O	DVD DATA1 / CD DATA L/R Clock (LRCK)
137	SDT0	MPEG	O	DVD DATA0 / CD DATA Bit-stream(CDATA)
138	DVSS11	Power	S	VSS for Digital Circuit
139	PCD7	MPEG	B	CD DATA 7 / Test Input Pin7
140	PCD6	MPEG	B	CD DATA 6 / Test Input Pin6
141	PCD5	MPEG	B	CD DATA 5 / Test Input Pin5
142	PCD4	MPEG	B	CD DATA 4 / Test Input Pin4
143	PCD3	MPEG	B	CD DATA 3 / Test Input Pin3
144	PCD2	MPEG	B	CD DATA 2 / Test Input Pin2
145	PCD1	MPEG	B	CD DATA 1 / Test Input Pin1
146	PCD0	MPEG	B	CD DATA 0 / Test Input Pin0
147	DVDD12	Power	S	VDD for Digital Circuit (3.3V)
148	MDOUT1	MICOM	O	Mode Data1 Out Controlled by MICOM
149	MDOUT0	MICOM	O	Mode Data0 Out Controlled by MICOM
150	PLLDFCT	Monitor	I	RF Defect Signal Input
151	SERLOCK	Monitor	O	LOCK Signal for Servo
152	MON	CLV	O	Spindle Motor ON/OFF Control Output
153	MDS	CLV	O	Spindle Motor Speed Control Signal(3.3V Digital Output)
154	MDP	CLV	O	Spindle Motor Phase Control Signal(3.3V Digital Output)
155	FOKB	RF	I	Focus OK Signal Input
156	DFCT	RF	I	Defect Detection Signal Input
157	MIRR	RF	I	Mirror Signal Input
158	VCOEXCK	PLL	I	VCO External Clock
159	DVSS12	Power	S	VSS for Digital Circuit
160	DVSS10	Power	S	VSS for Digital Circuit

PIN NUMBER CHARACTERISTIC

	Item	Pin Number	operation Voltage
Analog Block	Input	2, 6, 7, 10, 13, 14, 15, 16, 19, 20, 22, 23, 25, 27, 28, 29	0 - 3.3V
	Output	5, 9, 12, 17, 21, 24, 26, 30, 31, 32, 33, 34, 35	0 - 3.3V
	Source Voltage	3, 4, 18	3.3V
	Source Bulk Bias	11	Bulk (P-sub)
	Source GND	1, 8, 36	0V
Digital Block	Input	122, 158	0 - 5V CMOS
		37, 38, 39, 40	0 - 5V CMOS Pull-Down
		128	0- 5V TTL
		43, 44, 45 150, 155, 156, 157	0 - 5V CMOS Schmitt
		99, 113, 114, 116, 117	0 - 5V TTL Schmitt Pull-up
	Output	46, 47, 48, 49 50, 51, 52, 53, 54, 57, 58, 59 60, 61, 62, 63, 88, 90, 91, 100, 102, 120, 121, 123, 124, 125, 126, 127 131, 132, 133, 134, 135, 136, 137 148, 149, 151, 152	0 - 5V TTL
		101, 115	0 - 5V TTL Open-Drain
		87	0 - 5V TTL Tri-State
		153, 154	0 - 3.3V Tri-State
	Bi-directional Buffer	92, 97, 130, 139, 140, 141, 142, 143, 144, 145, 146	0 - 5V CMOS Tri-State
		66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 82, 83 104, 105, 106, 107, 108, 109, 110, 111	0 - 5V TTL Tri-State
	Oscillators	95	-
		94	-
	Source Voltage	56, 64, 118, 119	5V
		55, 65, 89, 93, 98, 103, 129, 147	3.3V
	Source GND	41, 42, 80, 81, 84, 85, 86, 96, 112, 138, 159, 160	0V

BI-DIRECTION PIN CONTROL

The following bi-directional pins have different input/output status depending on the internal IC setup.

— CMOS Bi-direction pins

The following pins are input when MICOM Command ($1C) is set as x111 xxxx.
Pin Number : 92, 97

The following pins are output when MICOM Command ($1C) is set as x000 xxxx.
Pin Number : 92, 97

— TTL Bi-direction pins

The following pins are input when MWRB (113) = "L" and MRDB (114) = "H".
Pin Number : 104, 105, 106, 107, 108, 109, 110, 111

The following pins are output when MWRB (113) = "H" and MRDB (114) = "L".
Pin Number : 104, 105, 106, 107, 108, 109, 110, 111

The following pins are used as DRAM Data Bus.
Pin Number : 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 82, 83

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Digital Input/Output Pin (V_{DD} = 5.0V ± 10%, VSS = 0V, Ta = 0 to +70°C)

Symbol	Item	SPEC			Condition	Unit
		Min	Typ	Max		
VIH	High level Input Voltage					
	CMOS Interface Level	3.5	-	-		V
	TTL Interface Level	2.0	-	-		
VIL	Low level Input Voltage					
	CMOS Interface Level	-	-	1.5		V
	TTL Interface Level	-	-	0.8		
VT	Switching Threshold	-	2.45	-	CMOS	V
		-	1.45	-	TTL	
VT+	Schmitt Trigger, Positive-going Threshold	-	3.0	3.5	CMOS	V
		-	1.8	2.0	TTL	
VT-	Schmitt Trigger, Negative-going Threshold	1.5	2.0	-	CMOS	V
		0.8	1.1	-	TTL	
IIH	High level Input Current					
	Input Buffer	-10	-	10	Vin = VDD	µA
	Input Buffer with Pull-Down	10	100	200		
IIL	Low level Input Current					
	Input Buffer	-10	-	10	Vin = VSS	µA
	Input Buffer with 50k Pull-up	-200	-100	-10		
VOH	High Level Output Voltage					
	All Output	VDD -0.05	-	-	IOH = -1µA	V
	Type B2 (*1)	2.4	-	-	IOH = -2mA	
	Type B8 (*2)				IOH = -8mA	
VOL	Low Level Output Voltage					
	All Output	-	-	0.05	IOL = 1µA	V
	Type B2 (*1)	-	-	0.4	IOL = 2mA	
	Type B8 (*2)				IOL = 8mA	
IOZ	Tri-state output leakage current	-10	-	10	Vout = VSS or VDD	µA
IOS	Output Short Circuit Current	-	-	233	VDD = 5.5V, VO = VDD	mA
		-233	-	-	VDD = 5.5V, VO = VSS	
CIN	Input Capacitance (*3)	-	-	4	Any Input & Bidirectional Buffers	pF
COUT	Output Capacitance (*3)	-	-	4	Any Output Buffer	pF

(*1) : Type B2 Pin: 46, 47, 48, 49, 50, 51, 52, 53, 54, 57, 58, 59,
60, 61, 62, 63, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79,
82, 83, 87, 88, 90, 91, 97, 100, 101, 102, 120, 121, 123, 124, 125, 126, 127,
130, 131, 132, 133, 134, 135, 136, 137, 139, 140, 141, 142, 143, 144, 145, 146, 148, 149, 151, 152, 115, 153, 154,

(*2): Type B8 Pin: 92, 104, 105, 106, 107, 108, 109, 110, 111

(*3) : This Value exclude Package Parasitics.

OPERATING CONDITIONS

Normal Operating Conditions

Symbol	Parameter	Rating		Unit
VDD	DC Supply Voltage	5.0V	4.5 to 5.5	V
		3.3V	3.0 to 3.6	
TA	Commercial Temperature Range		0 to 70	°C

Maximum Operating Conditions

Symbol	Parameter	Rating		Unit
VDD	DC Supply Voltage	-0.3 to 7.0		V
VIN	DC Input Voltage	3.3V I/O	-0.3 to 3.6	V
		5.0V I/O	-0.3 to 5.5	
TSTG	Storage Temperature	-40 to 125		°C

BLOCK FEATURES

DSP BLOCK

ECC FEATURE

— Euclid's Algorithm Use.

— Same circuits are used for DVD and CD.

(1) For DVD (primitive polynomial : $x^8 + x^4 + x^3 + x^2 + 1$)
: Error correction capability for DVD Data.
→ PI (182, 172, 11) CODE : 5 error correction / 10 errata correction
→ PO (208, 192, 17) CODE : 8 error correction / 16 errata correction

— 33.8688 MHz Clock : at 1X operation (PI+PO+PI)/1 EFM BLOCK satisfied
->Basic operation

(2) For CD (primitive polynomial : $x^8 + x^4 + x^3 + x^2 + 1$)
→ C1 (32, 28, 5) CODE : 2 error correction
→ C2 (28, 24, 4) CODE : 2 error correction / 4 errata correction

— Repeated correction executed for Video-CD (C1-> C2 -> C1 -> C2)

EFM DEMODULATOR FEATURE

— CD PLAYER, CD-ROM, and DVD PLAYER Mode operations

— Demodulator
EFM+ Demodulation (DVD)
EFM Demodulation (CD)

— ID SYNC, Frame SYNC Detection/ Protection/ Insertion
4 Step ID SYNC/ Frame SYNC Protection Window interval setting
4 Step ID SYNC/ Frame SYNC Insertion Frame number setting

— SID Error Correction

— ID (Frame) SYNC Continuous Check

MEMORY CONTROL FEATURE

— CD data processor and DVD data processor share external 4M or 8M DRAM

— EFM data write, ECC data R/W, DESCRAMBLER R/W, and TRANSFER read addressing function.

(1) For DVD

— Uses 33.8688MHz crystal clock

— Continuous storage according to input regardless of data type (PO de-interleave)

— Acquires 13 ECC block areas in the 4M bit DRAM
(EFM, ECC, DESCRAMBLER, and TRANSFER circular execution)

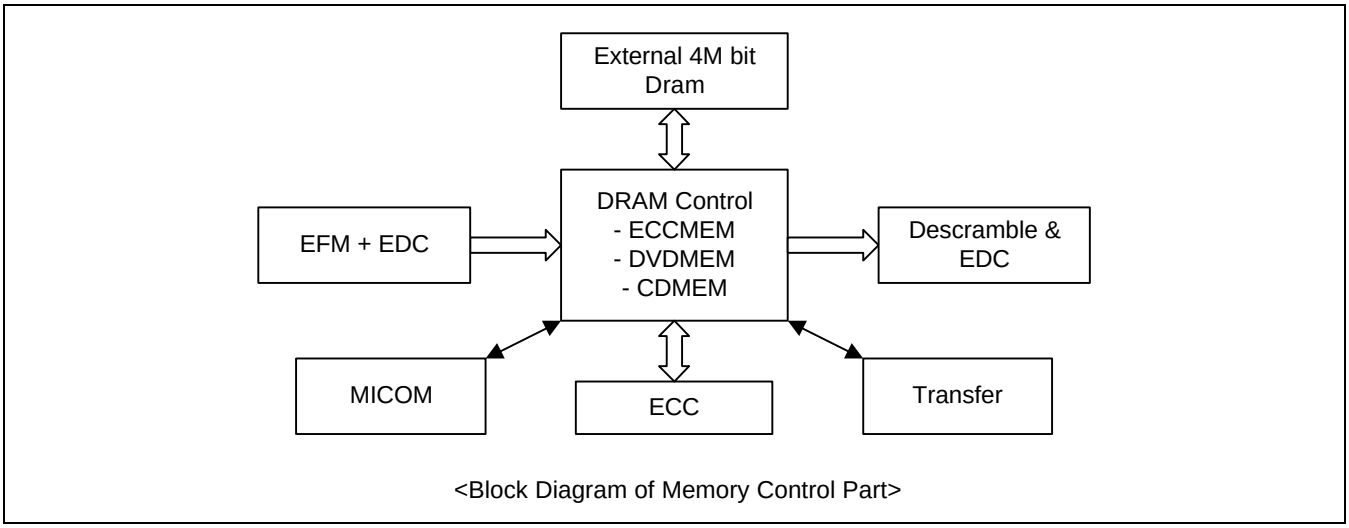
— Aquires MICOM user area.
(Selective use of 1 - 8 block in ECC block unit)

— Writes in sectors when writing the EFM data.

— Can transmit in sectors when transmitting data

— Block copy feature (Can specify the number of sectors)

— MICOM direct access on DRAM



<Block Diagram of Memory Control Part>

(2) For CD

— Uses CD-DA, CD-ROM, V-CD : 33.8688MHz crystal clock

— VIDEO-CD : Repeat correction possible

— Uses 8 kbyte memory

— EFM, ECC, and TRANSFER functions.

— EFM : WFCK base.

— ECC, TRANSFER : RFCK base.

— MICOM direct access on DRAM.

DESCRAMBLER & EDC & TRANSFER FEATURE

— MICOM descramble on/off control possible

— Output EDC flag to MICOM.

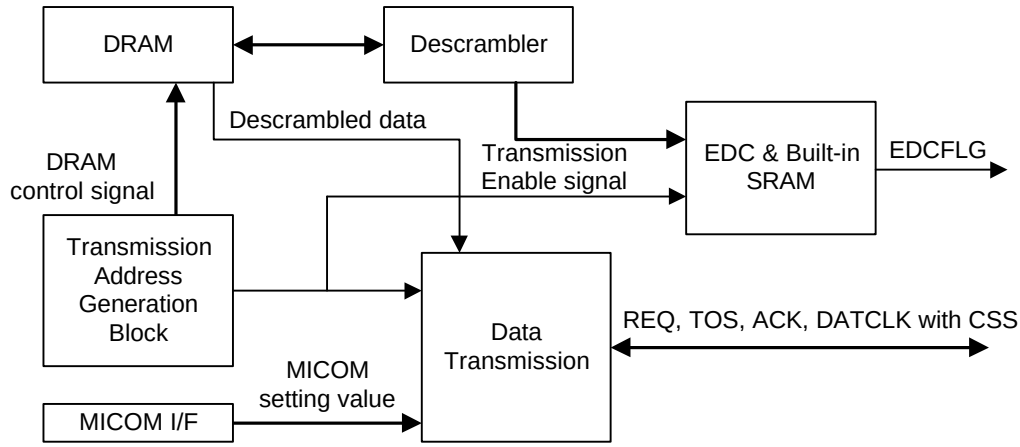
— 2048 bytes or 2064 bytes output selection possible

— Number of transmission sector specification possible

— Maximum transmission rate 5.4 MBytes/s.

— Parallel synchronous I/F support

— REQUEST, TOS, ACK, DATCLK, and EDCFLG active "L/H" selection possible.



<Block Diagram of the Transfer Part>

CD AUDIO FEATURE

¾ Receives data that has been completely corrected of errors in units of byte, and outputs it serially.

¾ INTERPOLATION, MUTE, and ATTENUATION processing for CD-DA.

SUBCODE I/F FEATURE

¾ CD graphic processing subcode data (P, Q, R, S, T, U, V, W) is serially output.

¾ Errors existing in the disc controlling subcode data (Q) are checked and output.
($p(x) = x^{16} + x^{12} + x^5 + 1$)

MICOM I/F FEATURE

¾ Address / Command Data : 1 byte

¾ Write Register Access
: CS Enable → W_reg Address Write → Command Data Write → CS Disable

¾ Read Register Access
: CS Enable → R_reg Address Write → R_reg Data Read → CS Disable

DIGITAL SERVO BLOCK

PRODUCT SUMMARY AND FEATURE

— The servo block in chip uses the input signal processed in the RF amplifier and read from the CD-DA/VIDEO-CD/DVDP Disc. The digital servo block receives the input signal for focus and tracking.

OPERATION DESCRIPTION

NORMAL PLAY

¢°¢° HOME IN

Summary

If a PS signal is not produced after a specified time after moving the P/U from its initial position to the innermost track using the reverse sled move, it assumes that the P/U has homed in and moves forward for the amount of time it takes for the P/U to escape the lead in area. Then it finishes the task.

— input signal : PS0, PS1

— output signal : SLD

— operation MODE selection : (LIM = HDWcmd's factor)

LIM = L	LIM = H
Sled stop determined by the limit S/W	Sled stop determined by the position sensor

COMMAND

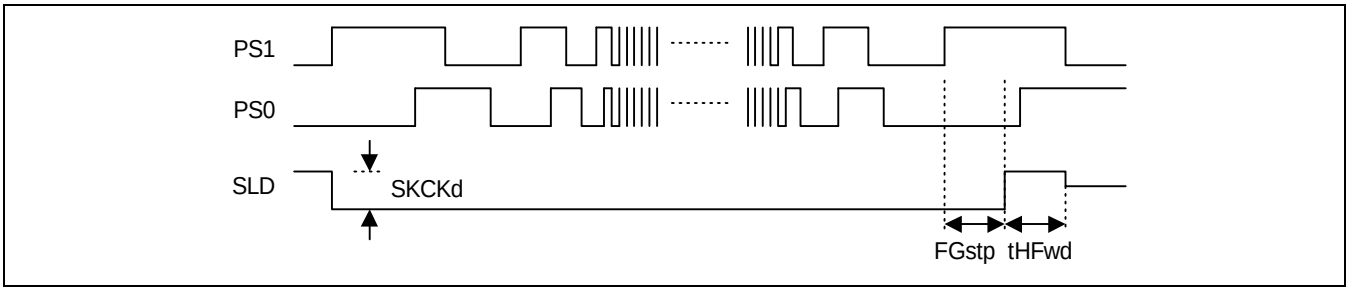
— SLDcmd(A4xxxx cmd) Transmission

Related REGISTER

REGISTER	Address	FUNCTION	COMMAND
SKCKd	10C1	SLED KICK LEVEL (Vref reference)	AFFFF1
FGstp	0049	PS period that determines the sled stop	ACFFF8
tHFwd	004A	FWD move time after home in	ACFFF9

Operation Description

— Sled is moved in the reverse direction. If PS1 or PS0 shows no signal change for a set length of time (FGstp), forward KICK the sled output for tHFwd, then return to Vref.



— Home In detection by limit S/W (when there is no sled position sensor) :
If there is a limit S/W, it is set to HDWcmd's LIM = L (sled stop determined by limit S/W), DSSP's PS0 pin is changed to SSTOP, and the limit S/W is connected to that block.
SLDcmd's home = L (normal), SMOV, SPLY's bit is controlled, and MICOM is manual.

¢°¢° FOCUS SEARCH (DISC DETECTION)

Summary :

The FOD outputs delta waves and moves the actuator up and down to determine disc presence and disc type using the FE (S_CURVE) signal. The results are sent to MICOM using a data bus.

— Input signal : FE

— Output signal : FOD, MDATA[7:0]

COMMAND

— DDTcmd(A1xxxx) Focus search & Disc detect

Related REGISTER

REGISTER	ADDR.	FUNCTION	COMMAND
FSpk	0055	Ouput control coefficient at F_srch pull_in(% of full swing)	AAFFF0
unBal	00BD	S_curve unbalance % reference	BE00BD
POS_J	10C7	Determine with FODbias level	AFFFF7
DDT_J	10C8	Detection level	AFFFF8
Fpk_J	10C9	S_curve size level	AFFFF9
LYdt	10CE	layer length level	AFFFFE
NZlvl	10CC	noise level	AFFFFC

Operation Description

— When the focus search command is received, the output signal FOD starts at the Vref voltage and outputs triangular waveforms. At this time, search speed or slope is decided by the FSP value from the disc detect command coefficients.

— Disc presence and type are detected by the disc detect command, and its references include the following:

(1) FEpk : FE input signal's peak to peak value

(2) DBL : Number of S-curves

(3) POS : S-curve detection location

(4) DIN : S-curve presence

The location for carrying out disc detection is in the middle of moving from the lower value to the upper value when AUTO = L and UPDN = H. The results are stored in [FEpk] and [DDTdt]. After completing the disc detect command, the OR values of the two memories are output to MICOM (refer to command set's DDTcmd).

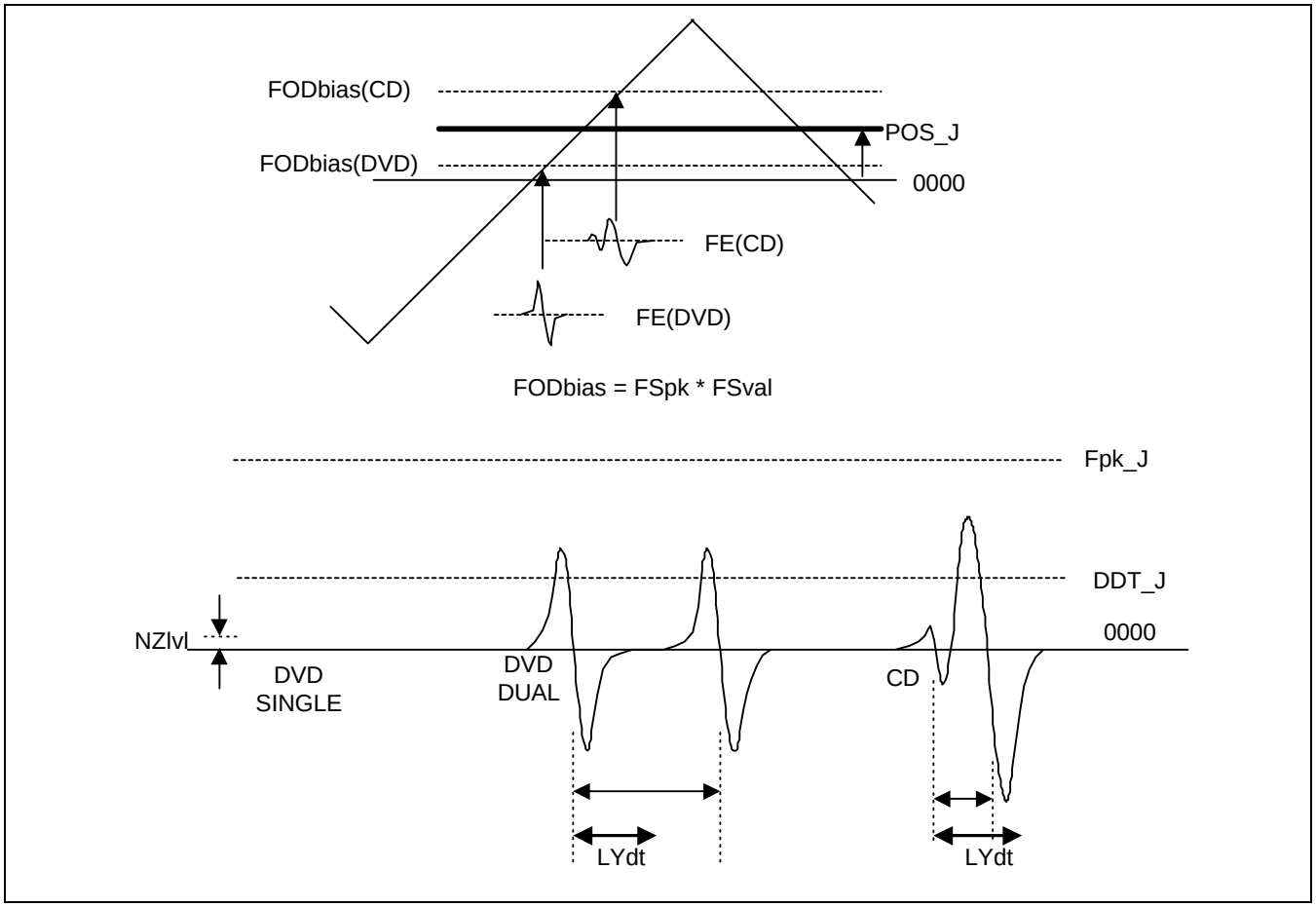
15 [DH] 8	7 [DL] 0							
FE PEAK LEVEL	DBL	FEpk	POS	0	0	0	DIN	0

FPS2-0	search speed
000	3.46 Hz
001	1.73 Hz
011	0.87 Hz
111	0.43 Hz

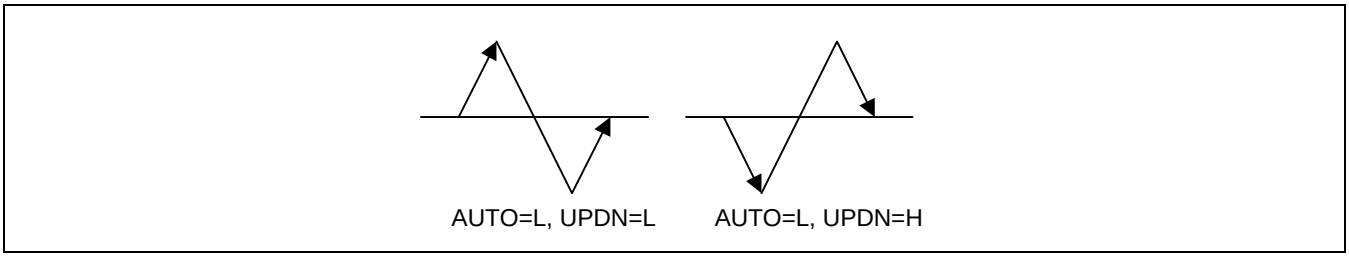
bit	Description	0	1
DBL	Number of S_CURVE	SINGLE(1)	DUAL(2)
Fpk	S_CURVE size	CD,DVDD(small)	DVDS(large)
POS	S_CURVE detection position	DVD(low)	CD(high)
DIN	S_CURVE detection	Empty	Present

— You can also set an S-curve detecting and search method using the command set CDScmd (A6xxxx)'s constants, FSOS and FSHF. When FSOS = "L", S-curve is detected in both directions without regard to DDTcmd's UPDN bit. When it is "H", S-curve is detected when UPDN = "L"(actuator up) and actuator is down. When UPDN = "H"(actuator down), S-curve is detected when actuator is up. This is because the actuator and the system can be initially unstable, and the S-curve must be detected when they are stable. Also, you can decide on a full search or half search during DDT using FSHF, to choose the search time.

DDT detection waveform



→ Reverse the focus search when Auto =1 and UPDN = 1.



¢°¢° FOCUS PULL-IN

Summary

The FOD outputs delta waves to move the actuator up and down, and carries out focus pull-in near the FE (S-curve) signal's zero cross.

— input signal : FE, FOKB

— output signal : FOD, FLKB

COMMAND

FONcmd (A2xxxx) Transmission

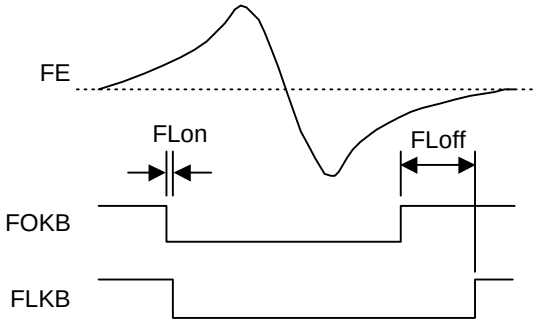
Related Register

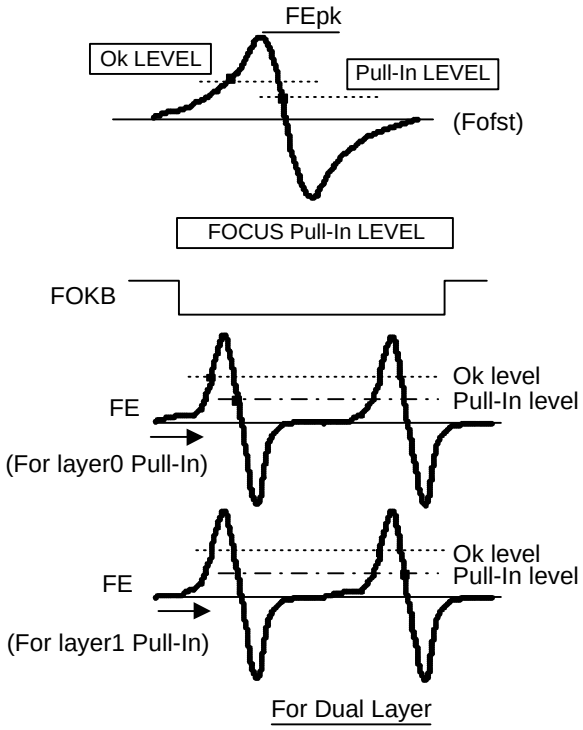
Register	Address	Function	Command
FSpk	0055	Output control coefficient at F_srch pull_in	
FZCofs	10CF	FZC offset level (manual mode)	
FLoff	004D	FLKB (Focus Lock) off time	
FLon	004E	FLKB (Focus Lock) on time	
FSspd	0038	Focus search speed register	

Operation Description

Pull-in standby status is maintained starting when the FE signal becomes larger than the S curve ok level (S_OK_L), and focus pull-in is carried out when the FE signal becomes smaller than the S curve pull-in level (S_PI_L).

PIL[3:0]	S_curve ok level	Pull-In level
xx11	FEpk/2	FEpk/4
xx01	FEpk/2	FEpk/8
x110	FEpk/4	FEpk/8
x010	FEpk/4	FEpk/16
1x00	FEpk/8	FEpk/16
0x00	FEpk/8	FEpk/32





¢°¢° TRACKING PULL-IN

Summary

When a TRK pull-in command is received in off track status, the tracking loop is turned on. If SLSV = L, sled is turned on simultaneously.

— input signal : TE, MIRR

— output signal : TRD, TLKB

Execution COMMAND

TONcmd(03xxxx) transmission

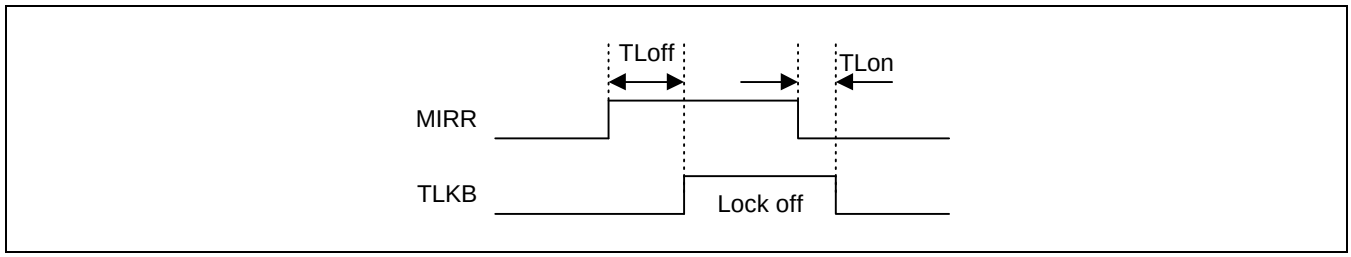
Related Register

Register	Address	Function	Command
GuT	0046	TRK Gain up time after TRK_pull_in	ACFFF5
dlyTG	1096	TGup delay time after completing GuT	BE1096
TLoff	004F	TLKB (Tracking Lock) off time	ACFFFE
TLon	0050	TLKB (Tracking Lock) on time	ACFFFF

Operation Description

— GuT (+dlyTG) must be set so that right after tracking on, gain is up to the tracking servo's settling period (period where the remaining difference exceeds the allowed range) to raise the stability of track pull-in.

— If a beam spot exists between tracks during play (deviation from the track), the RF IC outputs to MIRR = H. tracking lock status is determined using the MIRROR signal.



FOCUS / TRACKING manual gain up/down command :

The MICOM can optionally set the gain.

GAIN	COMMAND	Fchg	DWN (fcs)	Tchg	UP (trk)
manual fcs down/trk up	FBF000	H	H	H	H
manual fcs down/trk norm	FBE000	H	H	H	L
manual fcs/trk gain normal	FBA000	H	L	H	L
manual fcs norm/trk up	FBB000	H	L	H	H
manual fcs/trk gain change off	FB0000	L	don't care	L	don't care

AUTOMATIC CONTROL FUNCTION

¢°¢° FOCUS/TRACKING OFFSET CONTROL

Summary

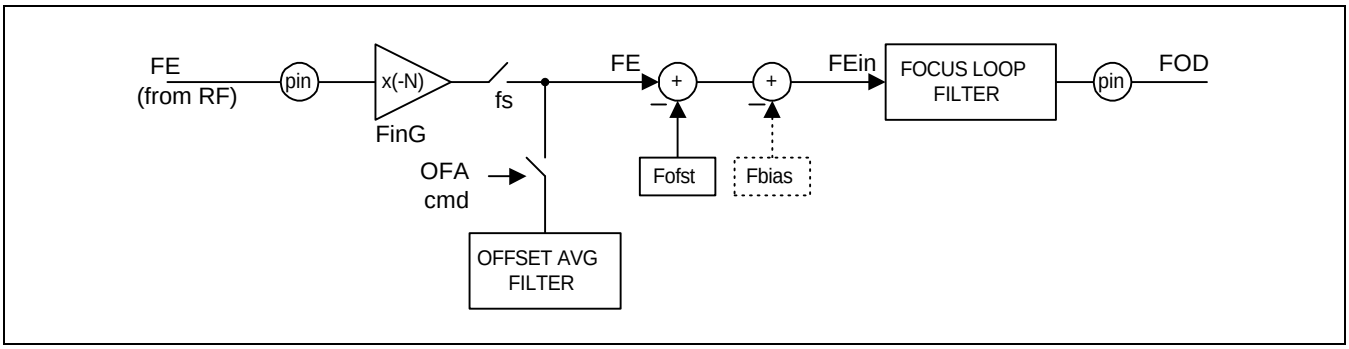
Before turning the servo loop filter on, the focus and tracking error offset are measured/averaged and stored in the register. This is to use the values during later filter operations in order to eliminate remaining error offset.

— Input signal : FE, TE

— Control Register(32bit) : Fofst(#1083~2), Tofst (#1085~4)

— Output Signal : SENSE

— FILTER Operation :
FEin = FE - Fofst - (Fbias) TEin = TE - Tofst
(FE/TE : ADC DATA, FEin/TEin : LOOP FILTER INPUT DATA)



Execution COMMAND

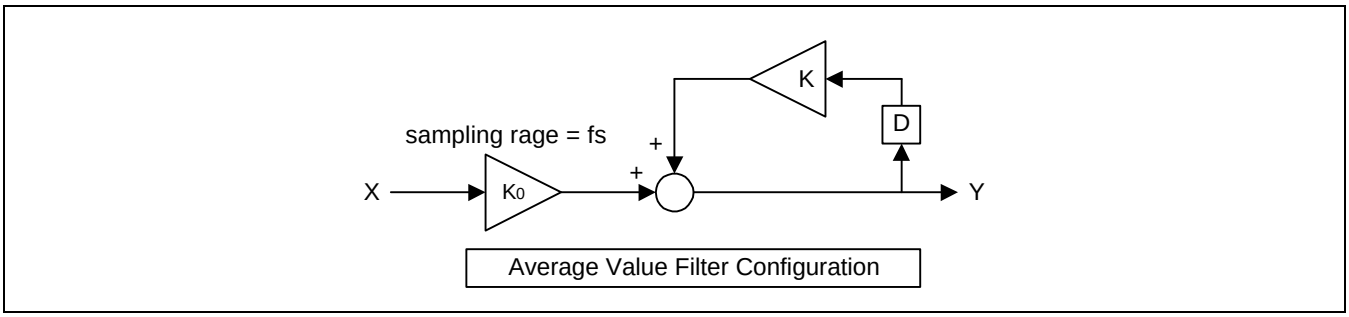
— OFAcmd(B1xxxx)

— Laser on/off selection is possible during offset measurement. If FOK is already on, the lens is automatically moved up/down until free of FOK.

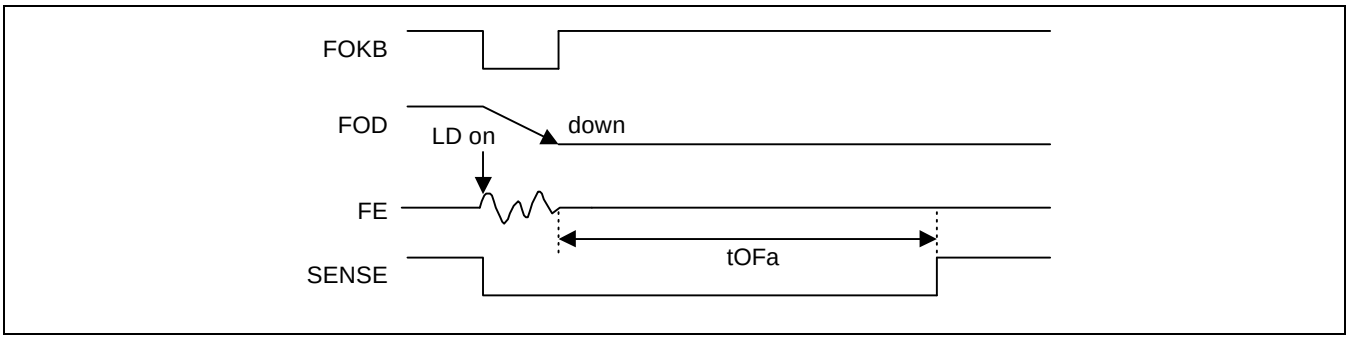
Related Register

Register	Address	Function
Fofst	1082	Focus Offset Data Save
Tofst	1084	Tracking Offset Data Save
Toffset K_0	003C	New data gain of the offset average value filter (K_0 = 1-K)
Toffset K	003D	Old data gain of the offset average value filter
tOFa	0058	Offset Measurement Time

— Average Value Filter :
The average value filter has basically the same configuration as the integrating filter, except K_0 must always have the value of 1-K. For example, if K_0 = 0040, a new average value is found by adding the new input's 1/512 and the previous average 511/512. (If the input is DC, it is maintained for the output without any changes in the gain.)



TIMING DIAGRAM (For example: When LD on & LENS down)



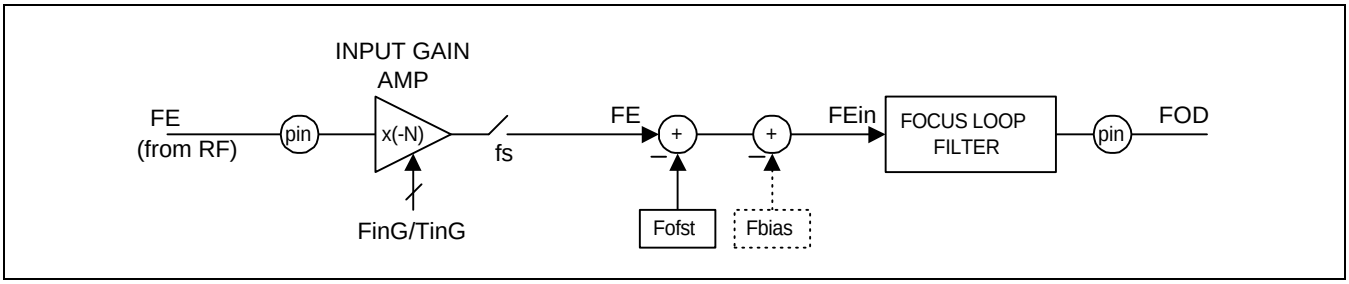
¢°¢° FOCUS/TRACKING INPUT GAIN ADJUSTMENT

Summary

The object of the focus/tracking input gain adjustment is to select the appropriate input gain using H/W before sampling, according to the size of the FE and TE signals input into the servo part. This allows you to use the ADC's full input range and raises the quantized data's ability for decomposition.

— Input signal : FE, TE

— Output signal : FEin, TEin(internal signal) or FOD, TRD (external signal)



COMMAND

manual setting : DPRW(BC) cmd
Automatic control : focus → DDT (A1) cmd
tracking → TBA (B3) cmd

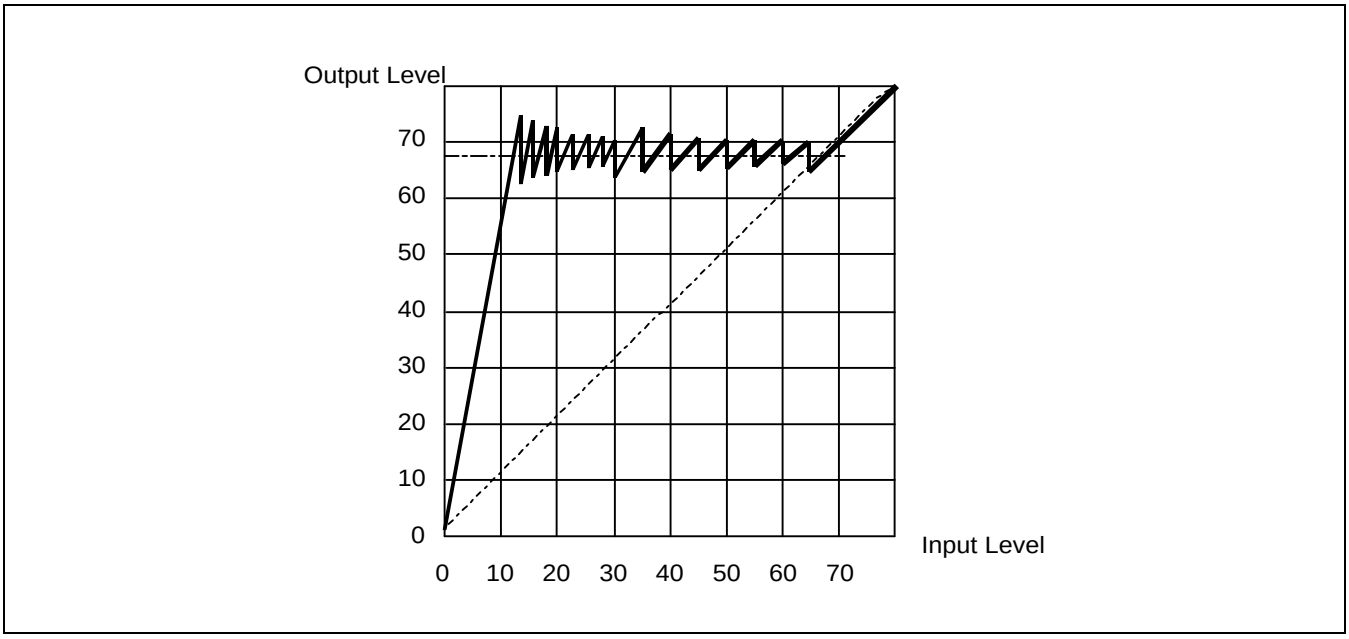
LOOK-UP TABLE

FinG/TinG	[dB]	Input level	Output level
00 - 07	0	7F - 70	7F - 70
00 - 07	0	6F - 68	6F - 68
08 - 0F	0.67	67 - 60	70 - 68
10 - 17	1.39	5F - 58	70 - 67
18 - 1F	2.18	57 - 50	70 - 67
20 - 27	3.05	4F - 48	71 - 66
28 - 2F	4.02	47 - 40	71 - 66
30 - 37	5.10	3F - 38	72 - 65
38 - 3F	6.35	37 - 30	6E - 64
40 - 43	7.41	2F - 2C	6F - 76
44 - 47	8.20	2B - 28	6F - 67
48 - 4B	9.07	27 - 24	6F - 66
4C - 4F	10.04	23 - 20	6F - 66
50 - 53	11.13	1F - 1C	70 - 65
54 - 57	12.37	1B - 18	70 - 64
58 - 5B	13.82	17 - 14	71 - 62
5C - 5F	15.56	13 - 10	72 - 60
5C - 5F	15.56	0F - 00	5A - 00

Operation Description

The input gain's automatic adjustment has the ability to absorb the deviation of the focus and tracking error's signal level from the RF IC for each set. Also, when there is no gain swiching feature for different disc types within the RF IC, it corrects the focus and tracking error's signal level difference. For focus, the s_curve size measured during focus search is used as the input gain amp's input. For tracking, the TE's track zero cross size when the disc is spinning in off track status is used as the input gain amp's input. Automatic adjustment is carried out so that it is near 4.2V (6ch) no matter what the input gain amp's output level is. The look-up table given above shows the input gain amp's gain characteristics. This has the advantage of using the ADC's input range to its fullest, and improving the decomposition ability in quantization. If you have a gain feature in the RF IC according to disc type and the automatic adjustment feature is used for the total loop gain, the input gain can be set to a fixed value at an appropriate level by manual setting.

Input Gain Adjustment AMP'S Gain Characteristics (for automatic adjustment)



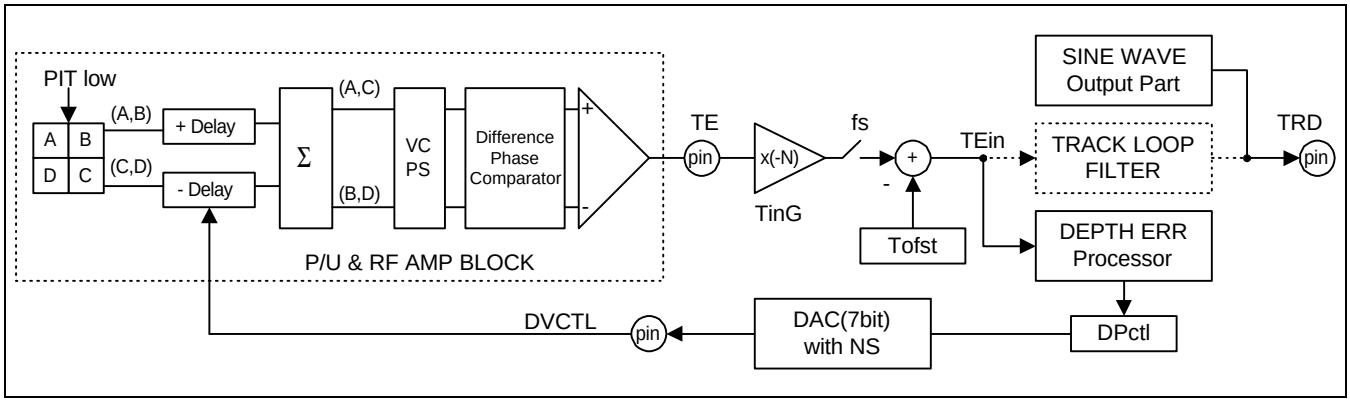
¢°¢° PIT DEPTH CONTROL (RESERVED).

Summary

When finding tracking error in the DVD using the DPD (Differential Phase Detect) method, the TE signal's size and offset can differ according to the various pit depths for each disc. To compensate for this characteristic, a delay of the opposite polarity to the RF Amp's (A, B) and (C, D) is given, and the amount of delay in the servo is adjusted to have a TE of a regular size regardless of the lens location.

— input signal : TE

— output signal : TRD, DPC



COMMAND

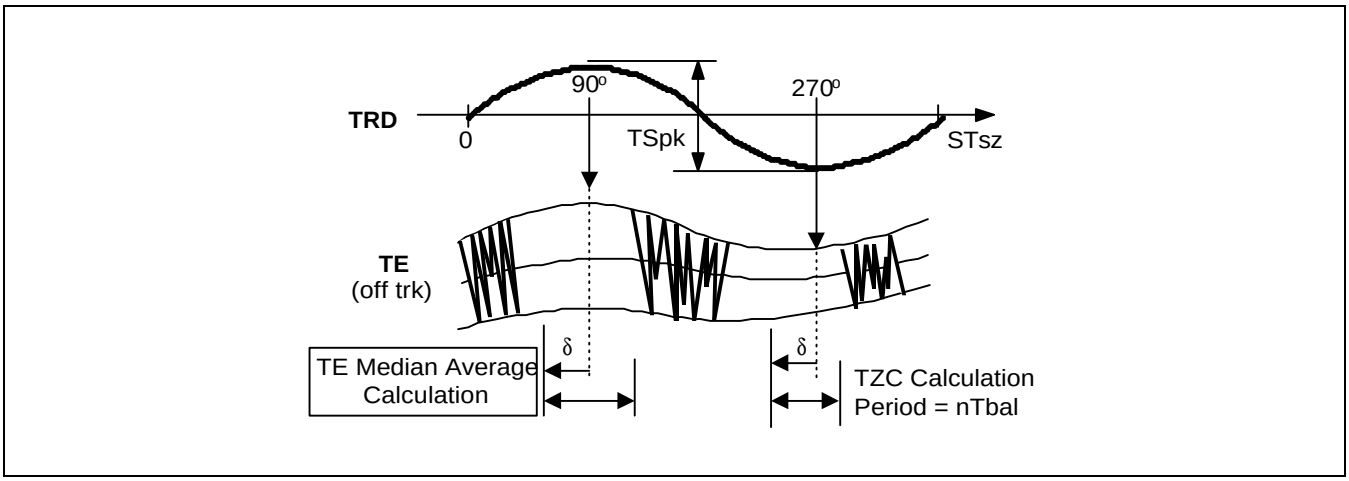
Transmit DPAcmd(B6xxxx)

Related Register

REGISTER	ADDR.	FUNCTION	COMMAND
nTbal	0061	Number of tzc cycles for extract the 1st depth control error	AAFFFC
nDP	10BE	TRD(sine) output frequency	ADFFFE
TSpk	0056	TRD(sine) output amplitude	AAFFF1
DPok	10B4	depth variance ok level (allowable error)	ADFFF4
DPk	002E	pit depth control sensitivity coefficient	AEFFFA
Tengh	00BE	cancel limit of the tzc size	BE00BE
fmin	00DA	tzc detection minimum frequency	BE00DA
fmax	00EA	tzc detection maximum frequency	BE00EA

Operation Description

The TE signal's amplitude and median changes according to the lens shift amount, due to the influence of the disc pit depth. The deviation is the most severe when the inner/outer shift amount is at its peak. Therefore, if you vary the RF IC's depth delay and carry out automatic adjustment, the TE signal's amplitude and median will be regular regardless of shift amount. This algorithm uses a method where the inner and outer circumferences' medians are the same at the maximum shift.



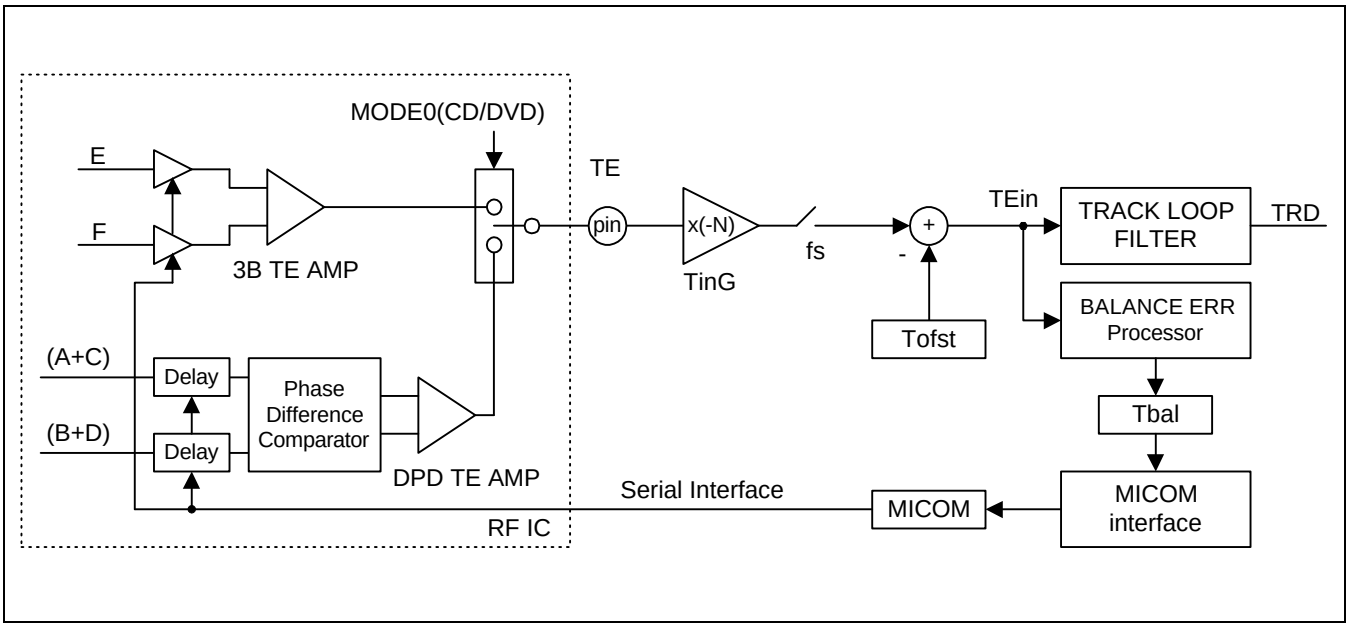
¢º¢º TRACKING BALANCE ADJUSTMENT

Summary

TE's zero cross component cycle's maximum and minimum value, generated by the eccentricity in the off track state, is found and averaged. TBAL signal is output so that the average value is the same as Tofst. For CDs, the balance is repeat adjusted by varying the E, F amp's gain within the RF Amp. For DVDs, the balance is repeat adjusted by varying each channel's delay amount.

— Input signal: TE

— Output signal : TBAL



COMMAND

TBAcmd (B3xxxx)

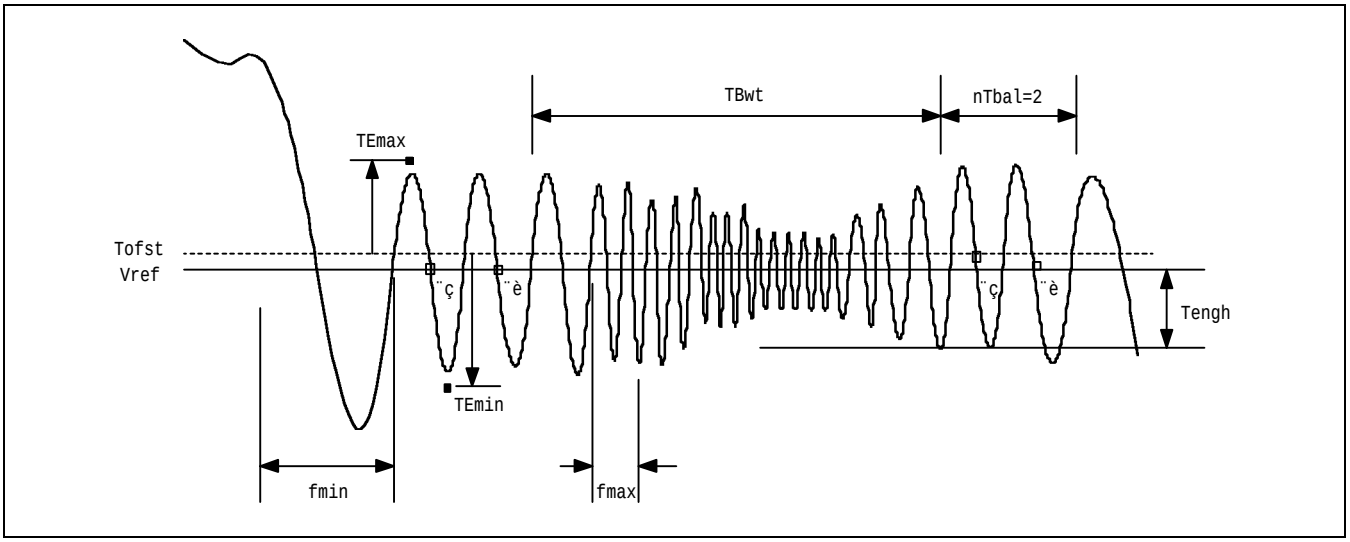
Related Register

REGISTER	ADDR.	FUNCTION	COMMAND
nTbal	0061	Number of TZC cycles to calculate the 1st balance error	AAFFFC
TBwt	005A	Wait time to the next measurement after changing Tbal	AAFFF5
TBok	10B1	Tbal ok level (allowable error)	ADFFF1
TBk	0031	TRK balance control sensitivity coefficient	AEFFFD
Tengh	00BE	TZC size minimum limit	BE00BE
fmin	00DA	TZC detection minimum frequency	BE00DA
fmax	00EA	TZC maximum frequency	BE00EA

Operation Description

Out of the TE(tzc) signals, the TEmin and TEmax are measured in the periods that pass through Vref and satisfy all the conditions of fmin and fmax. The median of these two values is calculated, and if these periods are continued for the number of nTbals, the difference between the average value of the medians and the adjustment reference level (= Tofst) is said to be the balance error. If the error is smaller than TBok, the adjustment is ended, but if it is larger, the product of Tbal's previous value and TBk is output.

When you renew the Tbal output value, the gain or delay within the RF's TE AMP varies, making the TE signal's balance error change as well. A wait time (TBwt) longer than the settling time according to such analog characteristics is set. When the system is stabilized after the wait time, the operations for balance error detection are repeated.



→ nTbal can be set maximum to 0080h with $2^{N.}$

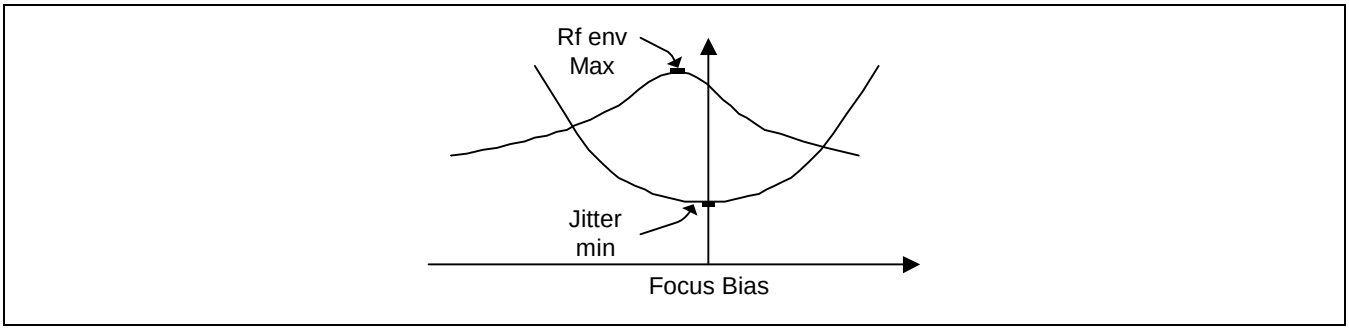
→ fmin and fmax frequencies → set data conversion method

$$\frac{fs}{fmin} = \frac{151.2\ kHz}{615\ Hz} = 246\ (00F6h)$$

¢°¢° FOCUS BIAS CONTROL

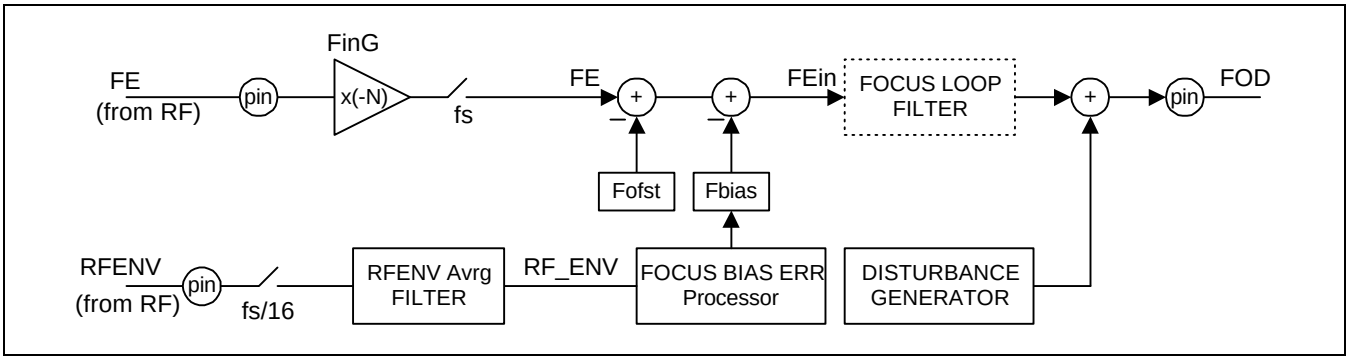
Summary

Focus bias adjustment is carried out so that playback is executed when the RF signal quality is at its best. The quality of the RF signal is shown by the jitter amount, but it is difficult to have an algorithm that can measure jitter on the IC and find the minimum point. Therefore, you use the characteristic where the jitter is always at its minimum near the focus bias point with the largest RF envelope size. The focus bias is adjusted so that the envelope is at its maximum size.



— Input signal: FE, RFENV

— Output signal: FOD



COMMAND

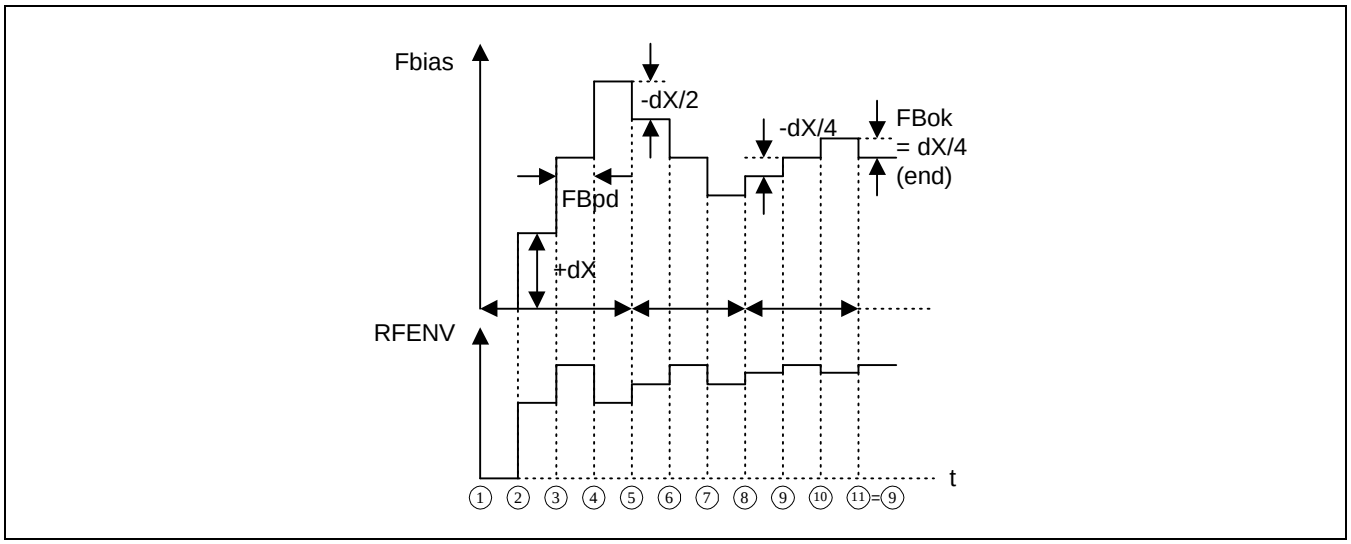
FBAcmd(B2xxxx)

Related Register

REGISTER	ADDR.	FUNCTION	COMMAND
FBpd	0059	Focus Bias control RFENV measurment cycle	AAFFF4
FBok	10B0	Focus Bias ok level	ADFFF0
dXbuf	002F	Initial dX setting level	AEFFFB

Operation Description

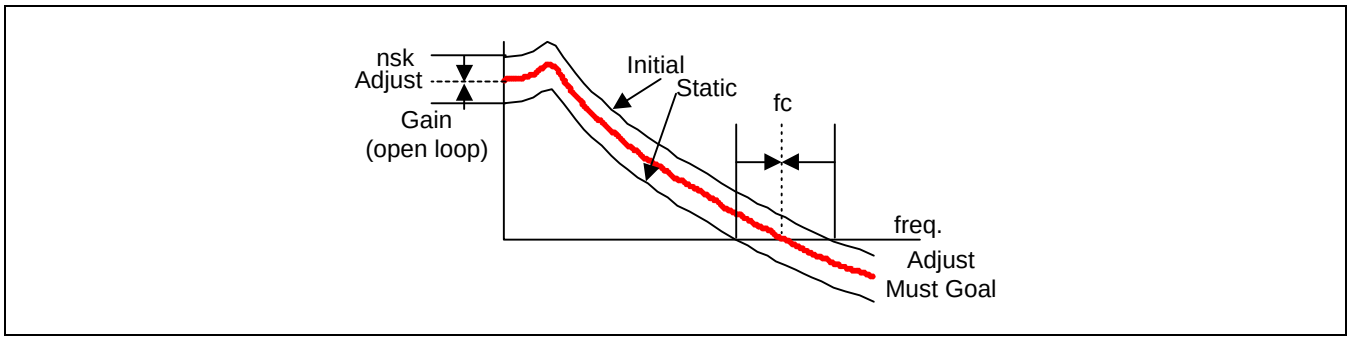
RFENV's signal difference is minimized by the FE signal carrying the disturbance. The disturbance uses the FE as reference and is used after selecting +, - dX. The disturbance level value is given to the first + direction, the RFenv value is stored, and + drepeated so that the dxbuf amount of the largest RFENV level is added/subtracted from the Fbias amount to find the final Fbias.



¢°¢° FOCUS/TRACKING LOOP GAIN CONTROL

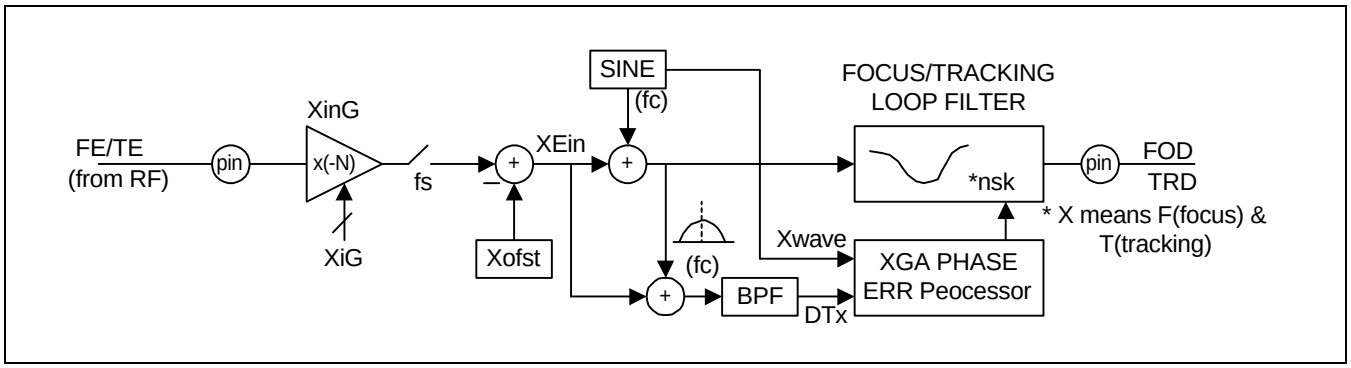
Summary

The loop filter's output gain is automatically adjusted so that the focus/tracking open loop bandwidth is at the specific frequency needed by the system.



— Input signal : FE, TE

— Output signal: FOD, TRD



COMMAND

— FOCUS GAIN control : Transmit FGAcmd(B4xxxx)

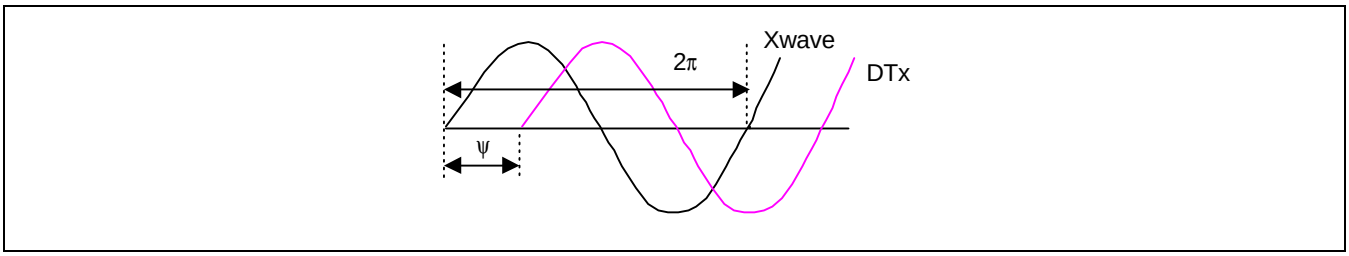
— TRACKING GAIN control : Transmit TGAcmd(B5xxxx)

Related Register

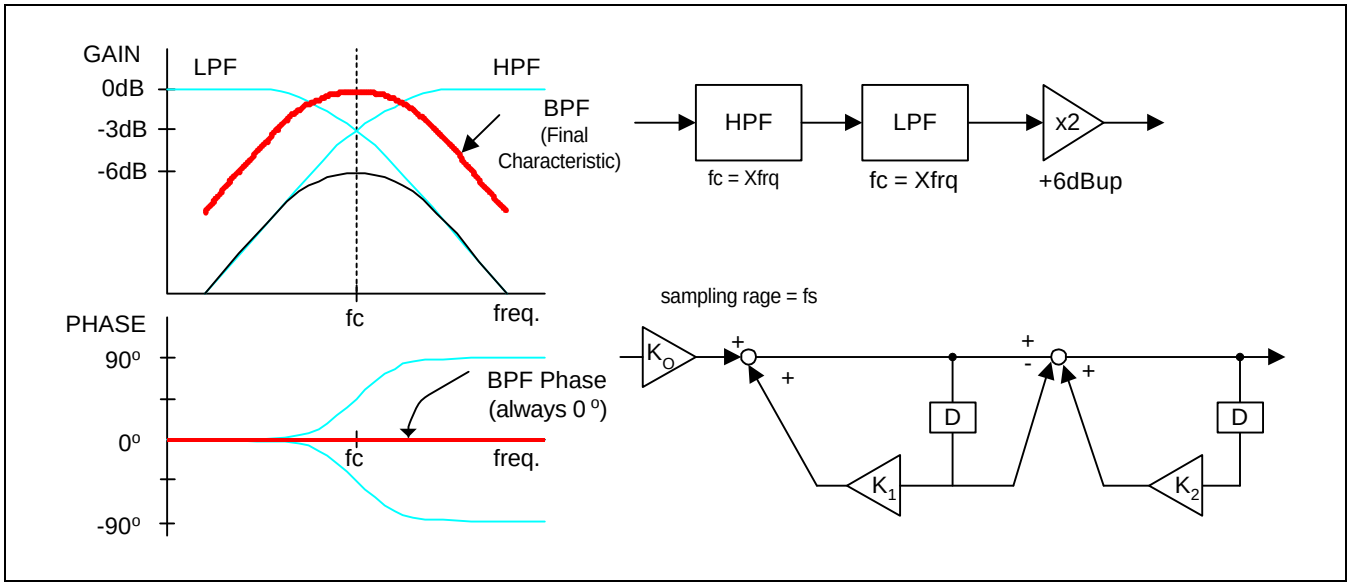
Register	Address	Function	Command
xGcnt	10C5	Measurement period	AFFFF5
xGwt	10C4	wait time	AFFFF4
Ffrq	0074	Focus loop bandwidth (sine freq.)	AAFFFE
Kf	0076	F_gain (sine) disturbance level	BE0076
Kcf	0032	F_gain control sensitivity coefficient	AEFFFE
FGok	10B2	F_gain control ok level	ADFFF2
FGmax	005C	F_gain control upper limit	AAFFF7
FGmin	005D	F_gain control lower limit	AAFFF8
Tfrq	0078	Tracking loop bandwidth (sine freq.)	AAFFFF
Kt	007A	T_gain (sine) disturbance level	BE007A
Kct	0033	T_gain control sensitivity coefficient	AEFFFF
TGok	10B3	T_gain control ok level	ADFFF3
TGmax	005E	T_gain control upper limit	AAFFF9
TGmin	005F	T_gain control lower limit	AAFFFA

Operation Description

A sine wave is output to the FOD output, and the phase difference (**y**) of the signals that have passed through mech such as P/U, and the original sine wave are compared. The loop EQ filter's final output gain is automatically adjusted so that the phase difference is 90°.
The adjustment is repeated many times to find the optimum state, and BPF is carried out to eliminate the noise components in the input signal.



BPF for detection signal



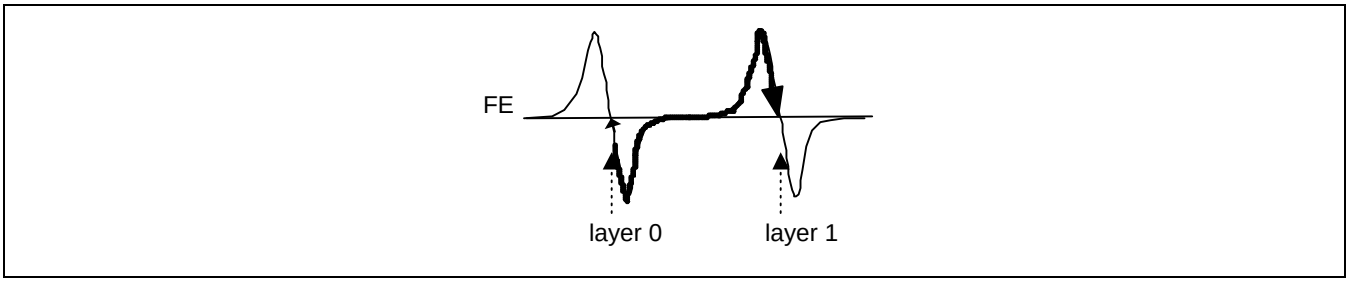
REGISTER	ADDR.	FUNCTION	COMMAND
xGa K_0	00FA	xGA BPFÀÇ K_0 (attenuator gain) = (1-K_1)*2	FDxxxx
xGa K_1	00FB	xGA BPFÀÇ K_1 (LPF pole coefficient)	FExxxx
xGa K_2	00FD	xGA BPFÀÇ K_2 (LPF pole coefficient)	FFxxxx

LAYER JUMP & TRACK JUMP & SLED MOVE FUNCTION

¢°¢° FOCUS (LAYER) JUMP

Summary

Layer jump is for when you want to go from the current layer to another layer and continue playback, while in DVD dual layer disc playback, or in off track state. Layer jump is carried out by outputting a kick/brake pulse to the focus output block.



— Input signal : FE

— Output signal : FOD

Execution COMMAND

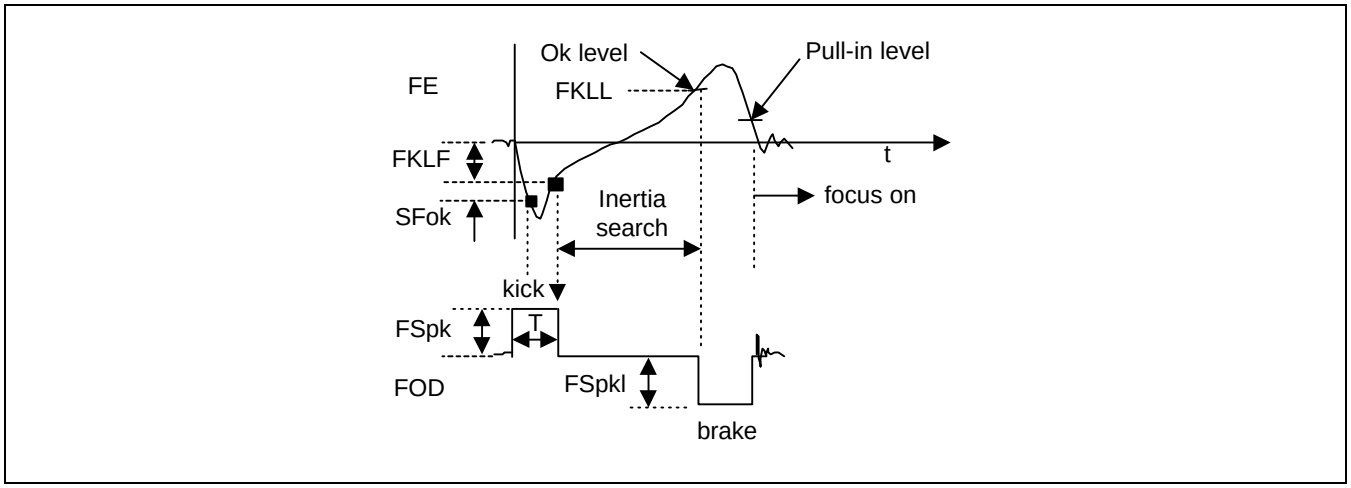
FONcmd's LYRX and TONcmd's TLRX specify the move target layer.

Related Register

Register	Address	Function	Command
FSpk	0055	f_srch output control coefficient (kick level)	AAFFF0
Fkll	0024	kick time determining FE level coefficient	AEFFF0
Fklf	108D	brake time determining FE level coefficient	BE108D
FSpkl	002C	f_srch output control coefficient(brk level)	AEFFF8
SFok	10CD	FE hysteresis level	AFFFFD
tFpi	0042	time after focus pull-in until tracking pull-in	ACFFF1

Operation Description

When the FON/TON command is input, the kick/brake level is selected according to the layer you are jumping to, and the sum of the FOD output average value and the kick value is output. This value determines the FE value, checks the FE signal level, and completes the layer jump by selecting a kick area and brake area according to the absolute values FKLF or FKLL.



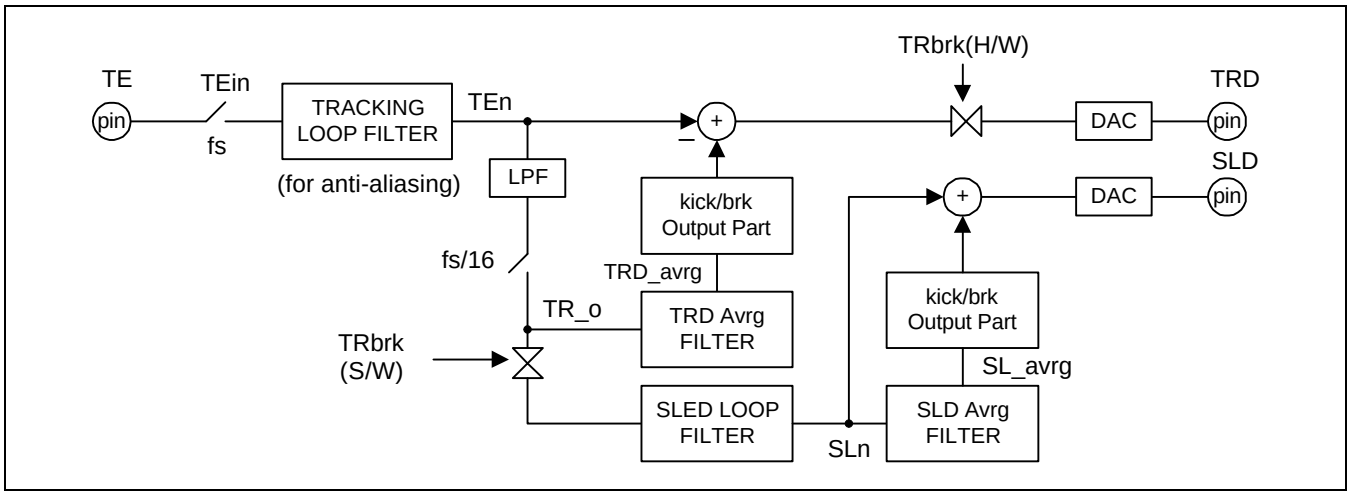
¢°¢° TRACK JUMP using KICK/BRAKE

Summary

This method jumps tracks by outputting an acceleration/deceleration pulse to the TRD output (bang-bang jump) to carry out kick/brake. The algorithm consists of 3 steps (kick + brake + stabilizing area), and the track count is executed using mirror or C.OUT (TZC without noise). Speed control is not part of the basic operations. Sled move (kick/brake method) can be carried out together depending on the number of tracks to be jumped.

— Input Signal : TE(TZC), MIRR

— Output Signal : TRD, SLD, C.OUT, TrS(TDAC), SENSE



INITIALIZE

(* is the default setting)

cmd	bit	MODE Content	L	H	default
Ton	TOLB	lens brake during trk pull-in after a jump	off	on(*)	A33600
	SFOG	Focus gain during kick+brk+Gut	normal	down(*)	
	STRG	Tracking gain during kick+brk+GuT+dlyTG	normal	up(*)	
INI	JPCK	track counter clock select during a jump more than Cchg	TZC(*)	MIRR	A90100
	TKJM	track jump method	kick/brk(*)	speed control	
	BTS	brake end condition	ivbuf(*)	Jstp	
FLG	enTJn	absolute trk pull-in during jump when target number of track is approached	No(*)	Yes	BA0011
HDW	enTT	TDAC output signal	TrS(*)	Tilt	A85900

Execution COMMAND

Transmit JMPcmd(A5xxxx)

JPM[1]	JPM[0]	JUMP MODE
0	0	AUTO (determined by bound)
0	1	TRACK JUMP
1	0	SLED MOVE
1	1	REPEAT TRK JUMP

Related REGISTER

Register	Address	Function	Command
TKCKd	10C0	Initial kick level	AFFFF0
SMlvl	10C3	sled move level during trk jump	AFFFF3
TKj_k	0025	trk kick time T = TKj_k * N kick/brake duty setting coefficient.	AEFFF1
TKl_k	002A	trk brake level control coefficient. trk brake level = TKCKd * 2 * TKl_k	AEFFF6
SMl_k	002B	sled brake level control coefficient. sled brake level = SMlvl * 2 * SMl_k	AEFFF7
Kwdt	0077	maximum kick delay interval time	BE0077
Bmin_k	10CA	minimum brake time (/5 if kick time)	AFFFFA
sTMk	00FF	trk brake interval sense window time maximum trk brk time = T * 2 * sTMk	BE00FF
Tstbl	0043	stable time after trk jump	ACFFF2
Twin	0044	MIRR/TZC blind time	ACFFF3
Mstp	0045	stop time compensation time during jump (stop = ivbuf-Mstp)	ACFFF4
GuT	0046	TGup/FGdw time after jump	ACFFF5
dlyTG	1096	TGup delay time after GuT end	BE1096
Cchg	10B8	C.OUT(up/dw) and TZC/MIRR(up) selection trk number	ADFFF8
Bound	10B9	trk jump and fine search boundary trk number	ADFFF9
SMcnt	10BB	number of trk until sled move after trk # kick	ADFFFB
ivTmg	00AA	TZC/mirr select trk # with K/B reversal location as reference	BE00AA
fsTjN	009A	Brk forced stop trk #	BE009A

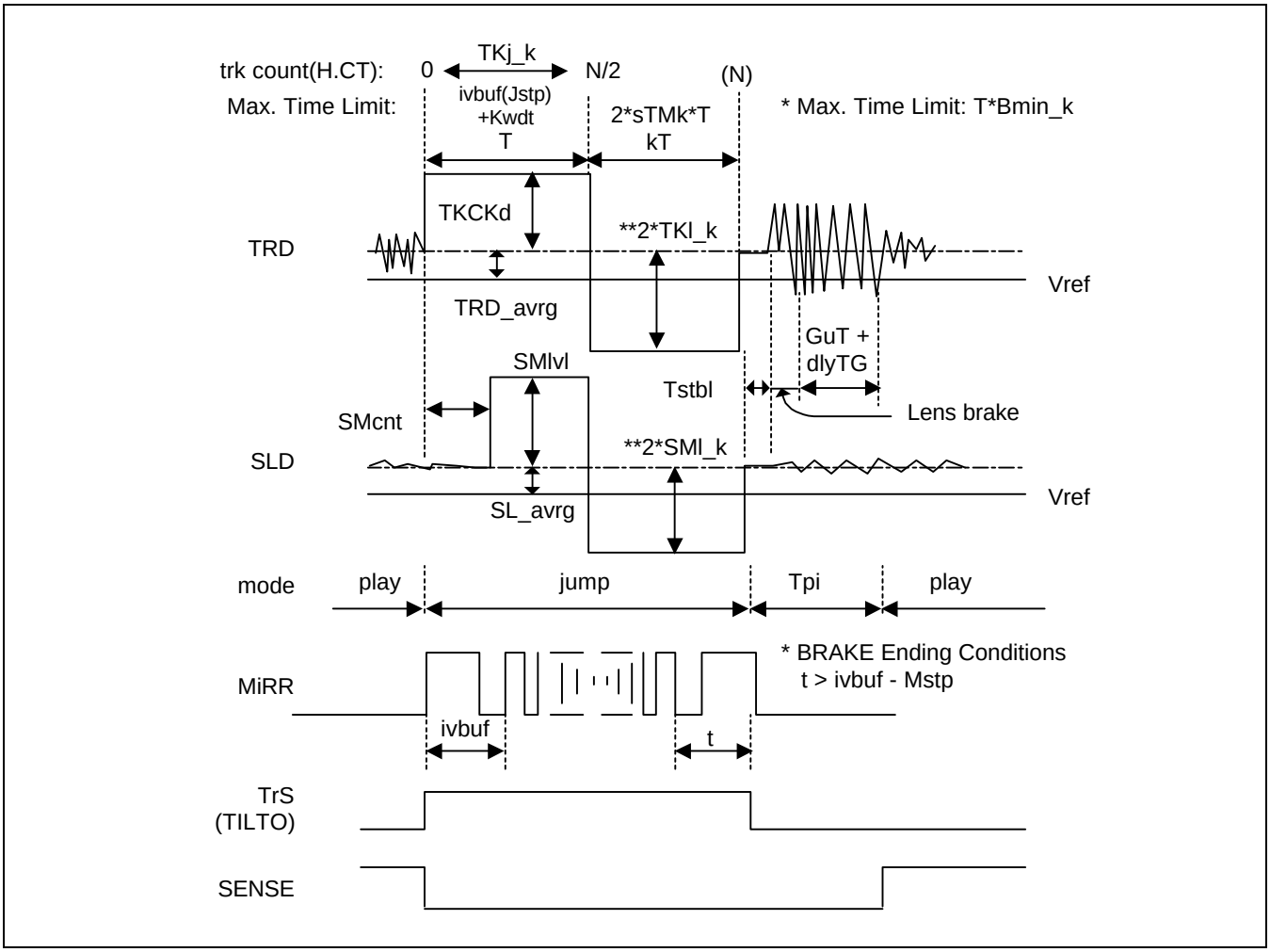
Operation Description

— TRACKING KICK/BRK output :
The track kick pulse is the TRD output average value (TRD_avrg) before jump, overlapped with the kick level (TKCKd). The track kick pulse reverts to brake when the track counter (H.CT) becomes larger than the jump z trk # (N)*TKj_k, and the level is TKCKd*2*TKl_k.

Maximum Kick Time Limit :
If the MIRR period within the kick area becomes larger than ivbuf (Jstp) + Kwdt (according to BTS select conditions), it is a long-term error of the MIRR, and there is a change to brake for safety.

— SLED KICK/BRAKE output :
When the jump trk # generated by the track kick reaches the sled movement count (SMcnt), the sled output average value before the jump (SL_avrg) and the sled move level (SMlvl) kick are overlapped. Sled reverts to brake along with the trk kick's reversion to brake, and the level is SMlvl*2*Sml_k.

— TRACKING KICK/BRK TIMING DIAGRAM

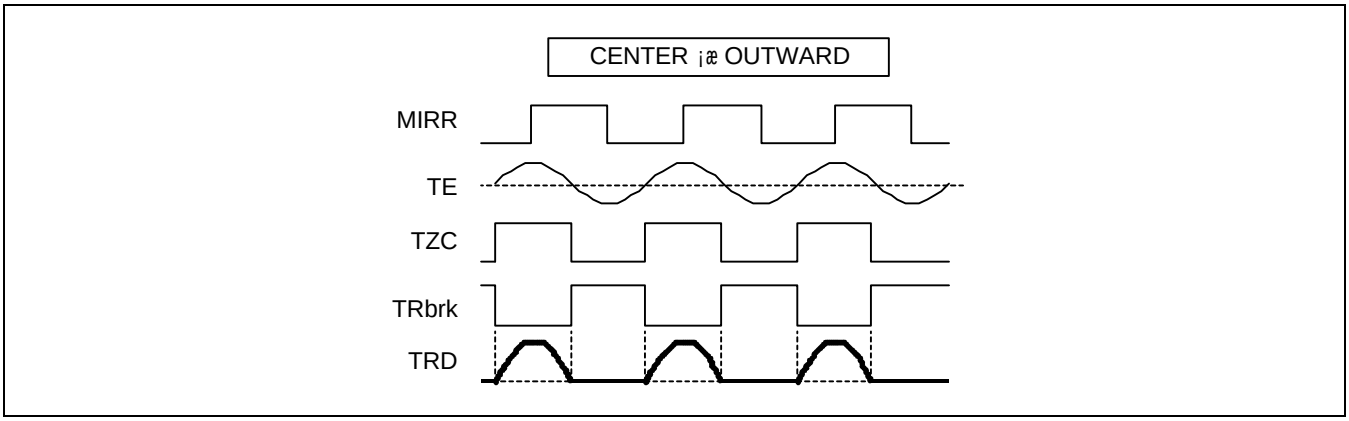


— JUMP end and Stabilization area

(1) Brake End
* When a deceleration is 1.5 times the acceration time (T).
* When the number of tracks you want to jump is less than [fsTJN], or when the initial value eTJN is 1 bit and the track counter hardware counter value is larger than the track number.
* When the timer value [TM1] selected in the deceleration area's Mirr negative edge is reduced at each interrupt so the value is less than [MSTP], and the different between 1.5T and the reduced value is less than [BRKmin].

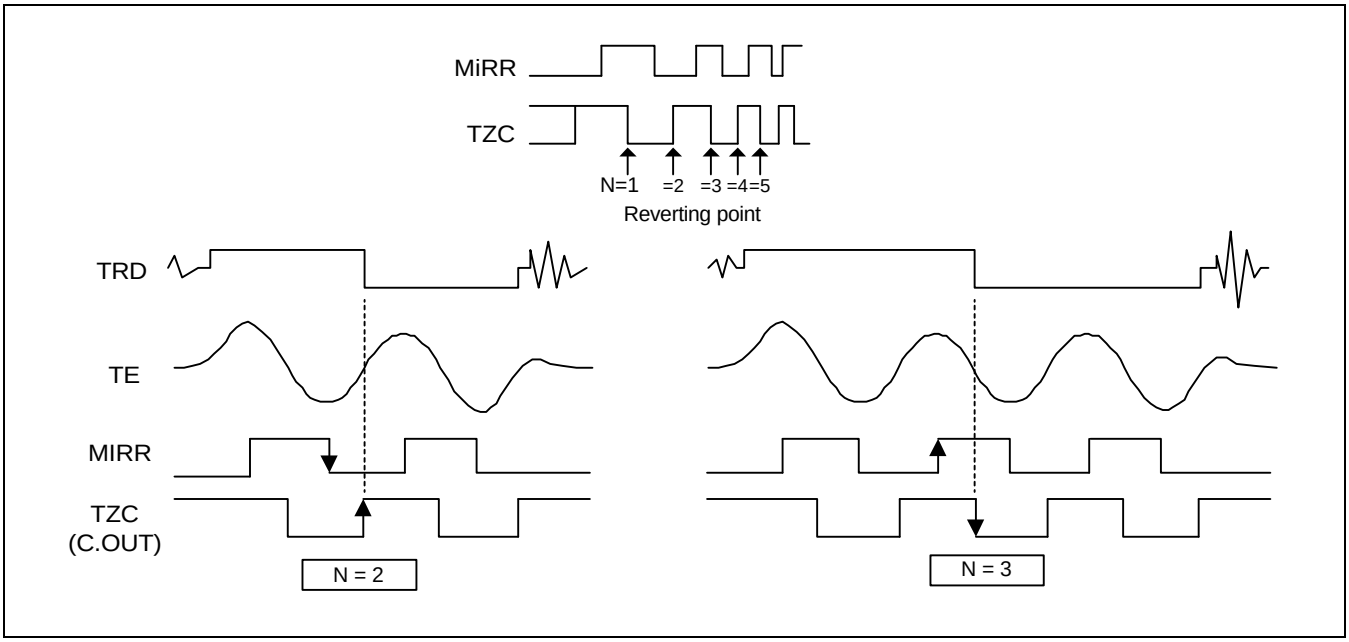
(2) Stabilization Time (Tstbl)
The brake end point is like when you step input to the actuator, so you wait at the output average level until the vibrations are settled.

(3) Lens Brake
When track cross is generated after the Tstbl period due to remaining speed, the TRD output is interrupted to the Vref level using the MIRR and TZC's phase difference.



(4) TRACKING GAIN UP :
After the stabilization time, the track on (Ton_int) routine is started. When Tstbl is over, GuT is set and tracking gain up (when STRG = H) and focus gain down (when SFOG = H) are carried out.
When GUT period is past, focus gain goes back to normal, and the sled filter is turned on. Also, when dlyTG passes, the tracking gain is turned to normal as well, and goes basck to normal play mode.

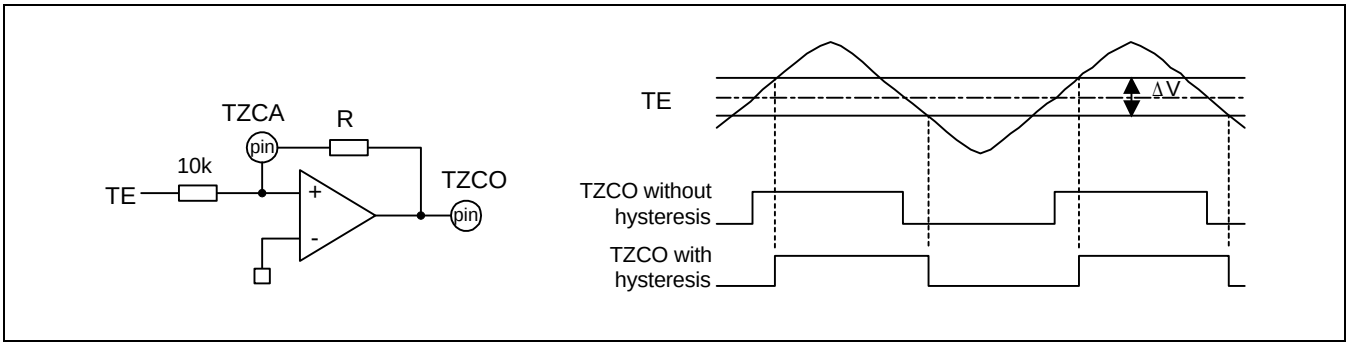
— KICK/BRAKE reversing POINT(calculate at the MIRR edge)



Output Average Value Filter

Register	Address	Function	Command
To_avrg K_0	003E	TRD average value filter's new data gain (K_0 = 1-K)	-
To_avrg K	003F	TRD average value filter's new data gain	FC7FC1
SLavrg K_0	007E	SLD average value filter's new data gain (K_0 = 1-K)	-
SLavrg K	007F	SLD average value filter's old data gain	FC7FC4

HYSTERESIS characteristics of the TZC Comparator



REPEAT TRACK JUMP(Refer to MICOM COMMAND SET)

XTAL / JIT[2:0]	0	1
000	MANUAL JUMP MODE	
001	2.3Hz	4.6Hz
010	2.3Hz	4.6Hz
011	3.5Hz	7.0Hz
100	5.7Hz	11.5Hz
101	9.2Hz	18.5Hz
110	12.7Hz	25.5Hz
111	17.0Hz	34.0Hz

¢°¢° FG PULSE SLED MOVE

Summary

This is a long distance track search using the sled kick/brake method when using the FG pulse as a way for measuring the number of tracks being moved. The FG pulse is composed of 2 pulses of 90° called PS1 and PS0, and the direction as well as distance can be found. the exclusive-or signal of PS0 and PS1 is called FG, and the move operation is carried out while counting the number of FG.

— input signal : PS0,PS1

— output signal : SLD, TRD, SENSE

INITIALIZE :

(* is default setting)

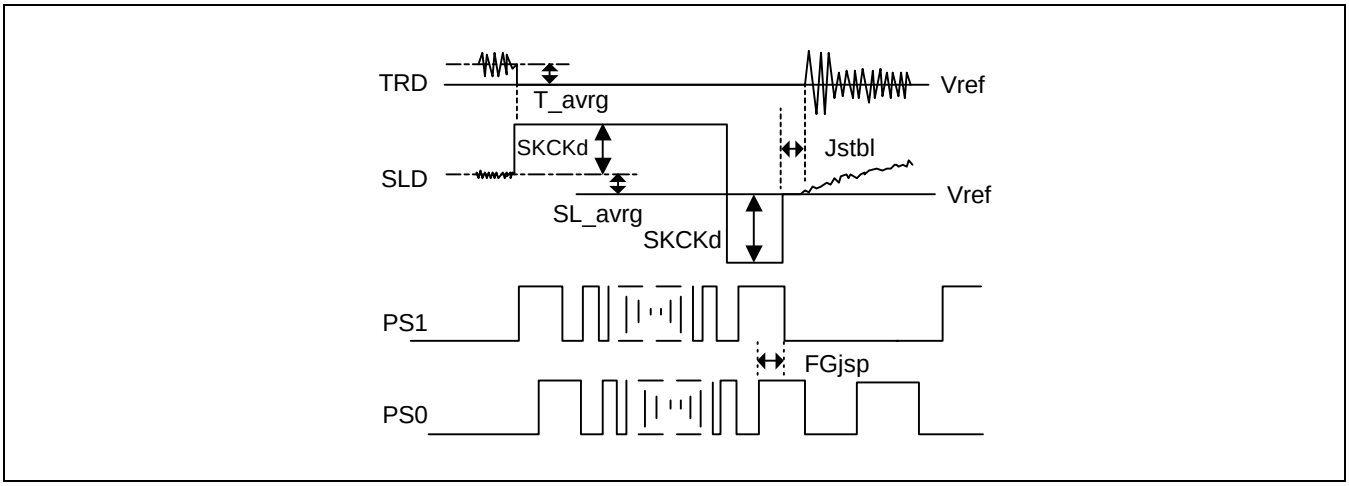
cmd	bit	MODE Description	L	H	default
HDW	enTT	TDAC output signal	TrS(*)	Tilt	A85900
	SNS	track count input signal during sled move	TZC/MIRR	FG(PS0,1) (*)	
INI	SMM	sled move method	kick/brk(*)	speed control	A90100
	JPEC	automatic error compensation when jumps over the target number of tracks.	no(*)	yes	
	BJJM	track jump compensation for the remaining tracks after a sled move.	no(*)	yes	
FLG	enTJn	When the target track number is reached while jumping, trk pull-in	no(*)	yes	BA0011
	enSPi	After sled move, pull in through SLED PULL IN routine	no(*)	yes	
Ton	TOLB	Lens brake during trk pull-in after jump	off	on(*)	A33600
	SFOG	Focus gain during kick+brk+Gut area	normal	down(*)	
	STRG	Tracking gain during kick+brk+GuT+dlyTG area	normal	up(*)	

Related REGISTER

Register	Address	Function	Command
SKCKd	10C1	kick/brk level	AFFFF1
SMlvl	10C3	kick level at sled move repeat kick (JPEC = H)	AFFFF3
SL_k	0029	kick period setting coefficient, separate setting for each move	AEFFF5
Jstbl	0041	stable time after sled move	ACFFF0
FGjsp	0044	PS period for trk pull_in	ACFFF7
PSstp	10F0	PS period for sled kick emergency detection reference	BE10F0
Twin	0044	MIRR/TZC blind time	ACFFF3
ENTc	10BD	sled encoder decomposition ability	BE10BD
GuT	0046	TGup/FGdw time after move	ACFFF5
dlyTG	1096	TGup delay time after GuT end	BE1096
Bound2	10BA	boundary between search and sled move	ADFFFA

Operation Description

— Position Sensor and track count method :
When the multiple N-S magnetic poles attached along the sled deceleration gear's cylinder starts to rotate by sled motor operation, the 2 hall sensors with the 90° phase angle detects the magnetic change and outputs a voltage in sine wave form. Also, this signal is changed into a logic signal in the comparator, and is input to the DSSP's status input as PS0 and PS1. The tolerance for the phase angle 90° is decided by the mechanical location, and if it is accurate, 4 FG edges are made in the PS0 and PS1's 1cycle.
The number of trks per FG pulse can be calculated by deck mechanisms such as the number of magnetic poles, etc. The value can be stored in the ENTc register by MICOM. When the FG edge is detected according to sled move, the S/W counter (STcnt) increases by ENTc, and you can measure the number of trks moved even without H.CT operation.



— SLED KICK/BRAKE Output :

(1) Waveform :
The sled kick pulse is the SLD output average value before the move (SL_avrg), overlapped with the sled kick level (SKCKd) and output to SLD. The sled kick pulse reverts to brake when the STcnt becomes the reverse count value found by move trk number (N)*SL_k. At this time, the brake level is the same as the kick level (SKCKd), but while the kick's point of reference is SL_avrg, that of brake is Vref. This is because the average output level before and after a move is different for long-distance moves. There isn't that much change in the lens shift in short movements in the level of track jump, so the kick/brake and stabilization area's output reference level are both SL_avrg (TRD_avrg). But in long-distance moves, the lens is at the midpoint, so there is no more meaning for the output average after kick. Therefore, the TRD output during sled kick/brake and stabilization area are held at Vref instead of TRD_avg, and off status is maintained.

(2) Limit function for emergencies during KICK/BRAKE :
Unlike track jump using MIRR/TZC, PS0 and PS1 have almost no chance of an output error due to circuitry reasons, apart from the damage of the hall sensor or comparator. However, there is a chance of kick time becoming very long, or getting trapped in an endless kick when the load on the sled becomes abnormally large. To prevent this, there is an emergency detection timer (PSstp) that stops the move and changes to pull-in mode when the PS edge doesn't come out within a specific length of time.

— MOVE end and stable period:

(1) BRAKE end :
In the deceleration area, if the interval between the FG pulse period is longer than the time set by MICOM (FGjsp), or the movement direction is incorrect, the SLD output is set back to Vref and the brake is stopped.

(2) Stabilization area :
The SLD output is held to Vref for the stabilization area set by MICOM. TRD also maintains Vref status. When the stabilization area comes to an end, it diverges into the TrSV routine within the Fon_int, and attempts normal tracking/sled pull-in.

¢°¢° SPEED CONTROL TRACK JUMP & SLED MOVE

SPEED CONTROL TRACK JUMP

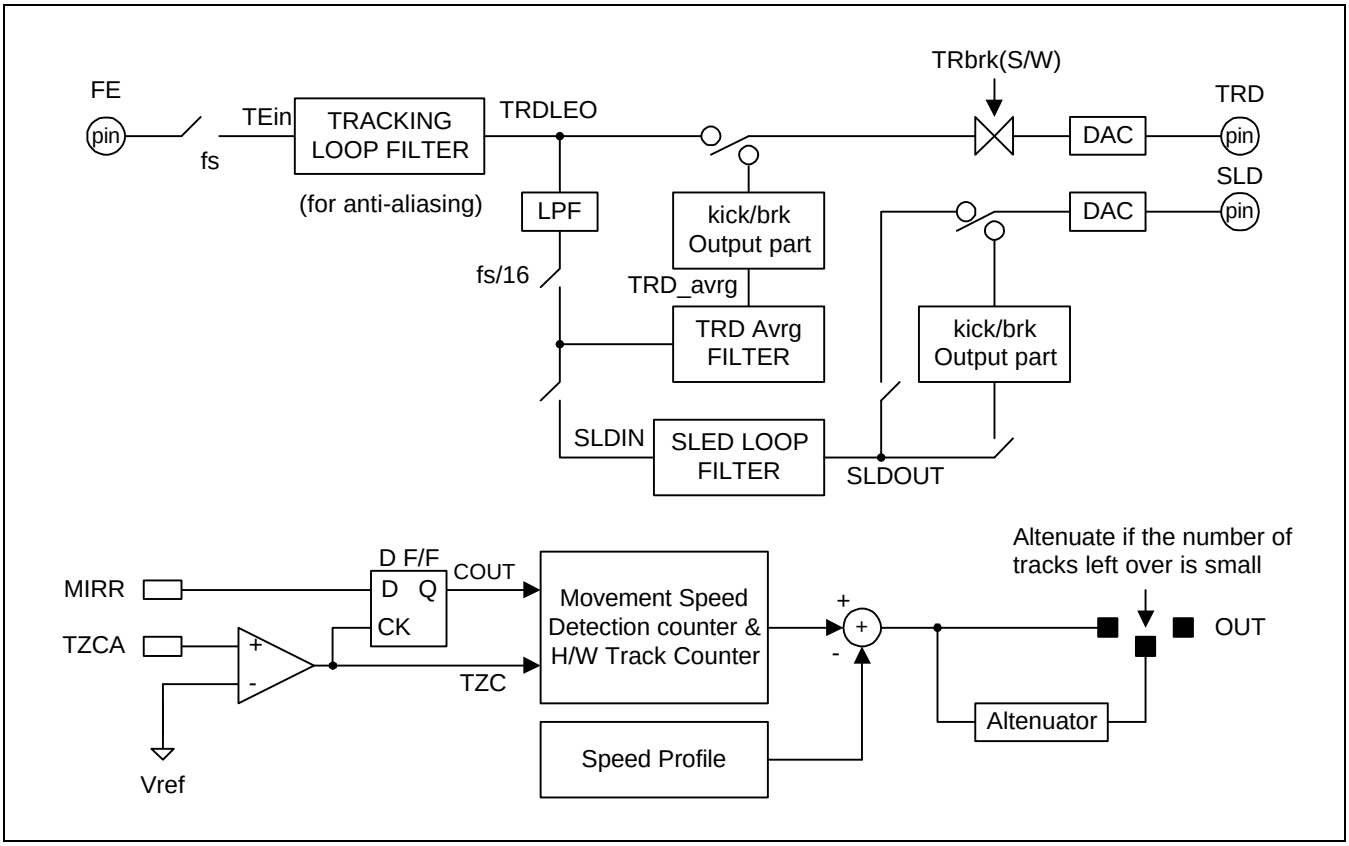
Summary

Speed control track jump is a track jump method that moves the P/U's lens. The number of tracks to be jumped can be set between 1 and 255. The speed control kick detects the P/U lens'speed in relation to the disc using the track error and MIRR signals from the disc, and controls the TRD kick signal so that it matches the DSP speed profile.
You can select the TM_win to reduce TZC errors such as glitches generated by initial kicks. When tracking is on, lens brake and loop gain up periods can be selected.

INITIALIZE

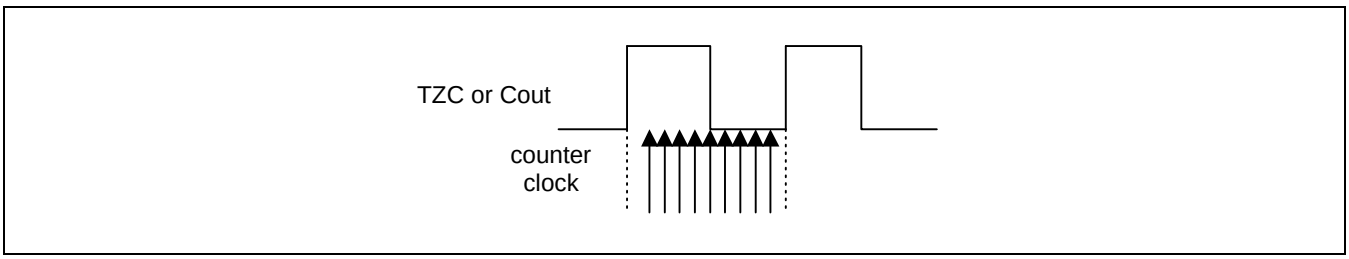
When INIcmd's TKJM is set to H and JPMcmd is received, speed control track jump is carried out for the number of tracks set by command. Other initial conditions are the same as those described in track jump using kick/brake.

BLOCK DIAGRAM RELATED TO SPEED CONTROL



Operation Description

Tracking drive carried out by measuring the difference between the speed profile and the MIRR distance: Speed is controlled by feedback to the TRD level. TZC, MIRR or COUT input into DSSP can be counted by the internal counter clock, so that you can move the tracks at the speed you want.
(Maximum speed 151.2/4kHz)



MIRR/TZC SPEED CONTROL SLED MOVE 1

SUMMARY

This method is a speed control sled move, but it uses the TZC/MIRR in the detection signal, consequently using the tracking drive (TRD) as well as the sled drive (SLD) as control output. It also has the track kick correct for eccentricity. However, it needs enough tuning because the combination of the mixing is very complicated. This method is appropriate for jumps that are too long for track kick, but too short for FG sled move. The principle behind speed control is almost the same as speed control track jump. The only difference is that the control output is not only track drive (TRD), but includes the sled drive (SLD). The maximum speed of this method is 151.2/4kHz .

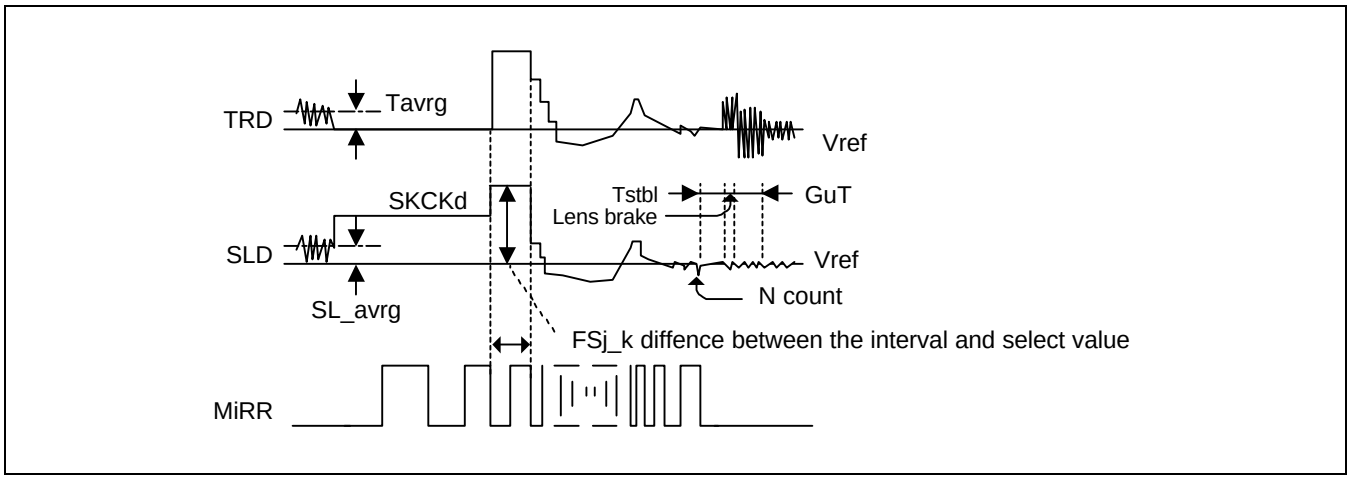
INITIALIZE :

When HDWcmd's SNS = "L", INIcmd's SMM = "H" and JPMcmd is received, a speed control track jump is carried out for the number given by command. Other initial conditions are same as those in track jump using kick/brake.

COMMAND

JMPcmd (A6xxxx).

TIMING DIAGRAM



MIRR/TZC SPEED CONTROL SLED MOVE 2

Summary

Like speed control sled move 1, this method also uses TZC/MiRR in the detection signal. However, this method only uses sled drive (SLD) as the control output, so it is appropriate for jumps where a high speed sled speed is required. The principle for speed control is almost the same as that of sled move 1, only excepting that the control output controls only sled drive (SLD) and that actual MIRRs are counted instead of between the edges of MIRRs. This method is usually used for long distance move, and the maximum speed is the same as MIRR or TZC's maximum speed from the RF IC. Therefore, when using this method, you need a high quality MIRR at high speeds.

INITIALIZE

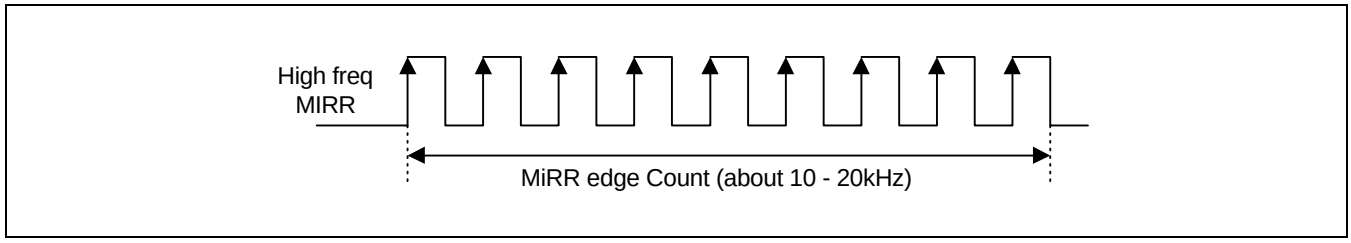
When HDWcmd's SNS = L, INIcmd's SMM = H and JPMcmd is received, speed control track jump is carried out for the number of tracks given by command. Other initial conditions are the same as those in track jump using kick/brake.

Executable COMMAND

JMPcmd (A6xxxx).

Operation Description

The speed can be controlled by selecting before hand the speed you want (number of MIRR) and counting the number of MIRR for measuring the deviance and sending feedback to the sled drive (SLD) level. You can move the tracks at the speed you want using the internal counter clock to count the TZC or MIRR input into DSSP.



FG PULSE CONTROL SPEED SLED MOVE

Summary

This method is an FG speed control (INIcmd's SMM = "H") sled move when you can use the FG pulse as a way to measure the number of tracks being moved. The principle of speed control is almost the same as that of speed control track jump. The difference is that the speed detection signal is not MiRR but FG (PS1& PS0), and the control output is not TRD, but SLD. This method is also used for long distance moves.

INITIALIZE

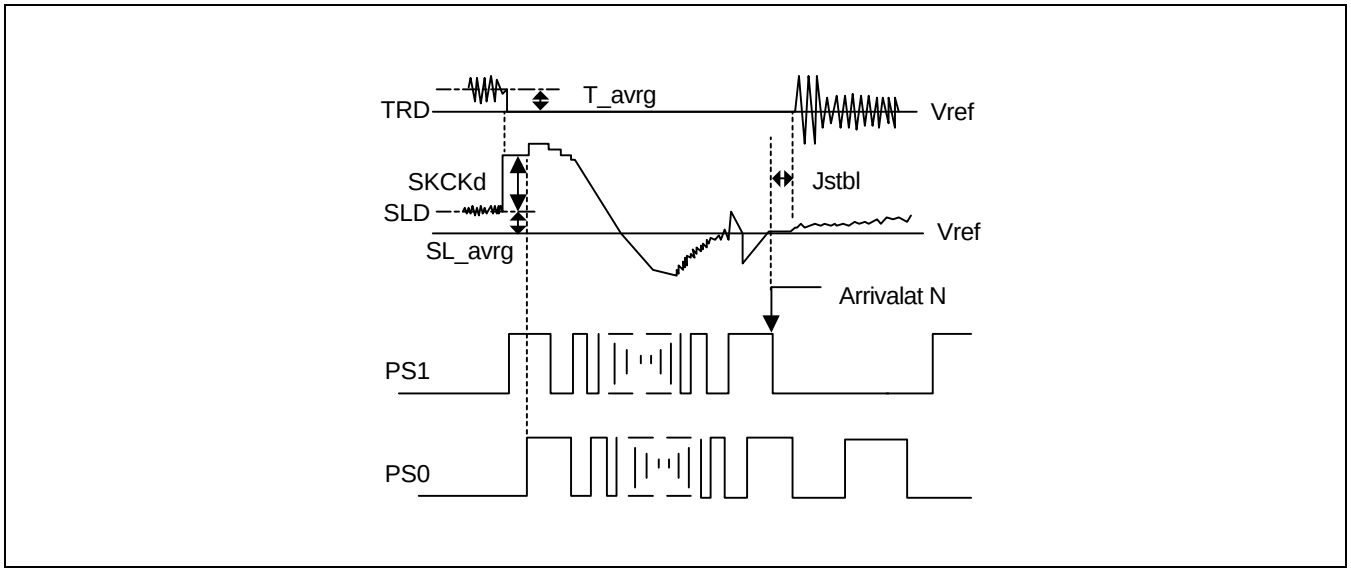
When HDWcmd's SNS = H, INIcmd's SMM = H and JPMcmd is received, track jump is carried out for the number of tracks given by command. Other initial conditions are the same as those in track jump using kick/brake.

Execution COMMAND

JMPcmd (A6xxxx).

Operation Description

The sled kick pulse is the SL_avrg before kick overlapped with SKCKd, which is output to SLD. The sled kick pulse reacts with the difference between the FG pulse's second edge and the speed profile's interval, so that the drive voltage is output to SLD. Speed control is carried out so that it matches the profile. Also, FG pulse is ENTc track, so if you have a short track search, the number of tracks moved becomes N immediately after speed control, making speed control useless.



¢°¢° EMERGENCY PROCESSING

FOCUS DROP PROCESSING

Summary

If during focus pull-in, playback or jump, the focus servo is dropped due to any reason, the system stability is increased by having an operation mode that automatically carries out pull-in without MICOM. You only need to set the initial conditions. No separate commands are needed.

— Input signal : FE, FOKB

— Output signal : FOD, FLKB

INITIALIZE

(* is default setting)

cmd	bit	MODE Description	L	H	default
FON	FOPI	Automatic pull-in at focus drop	yes(*)	no	A26200
EME	FDOL	layer selection for automatic pull-in after focus drop	previous layer(*)	don't care	A74F00
	upFv	FSval(P/U location info.) update after focus pull-in	yes	no(*)	
FLG	Fptmg	focus drop flag	FLK(*)	FOK	BA0011
HDW	PCUP	P/U type (vibration)	strong	weak(*)	A85900

Related REGISTER

Register	Address	Function	Command
FONc	1004	FON(02cmd) parameter copy	BE1004
FSspd	0038	Repeat pull-in f_srch speed	BE0038
FSpk	0055	F_srch pull_in output control coefficient	AAFFF0
FSrng	10C6	F_srch limit level	AFFFF6
tFpi	0042	T_pull_in time after F_pull_in	ACFFF1
FLoff	004D	Focus Lock off time	ACFFFC
FLon	004E	Focus LocK on time	ACFFFD

ANTI SHOCK MEASURES

Summary :

If an external shock is applied to the system while in playback, the lens shakes, causing tracking errors that lower the stability of the servo system. To reduce the influence of such errors, abnormal signals above a certain level of frequency is detected as shock components for generating ATSC signals. Appropriate steps are taken by the tracking and focus servo loop.

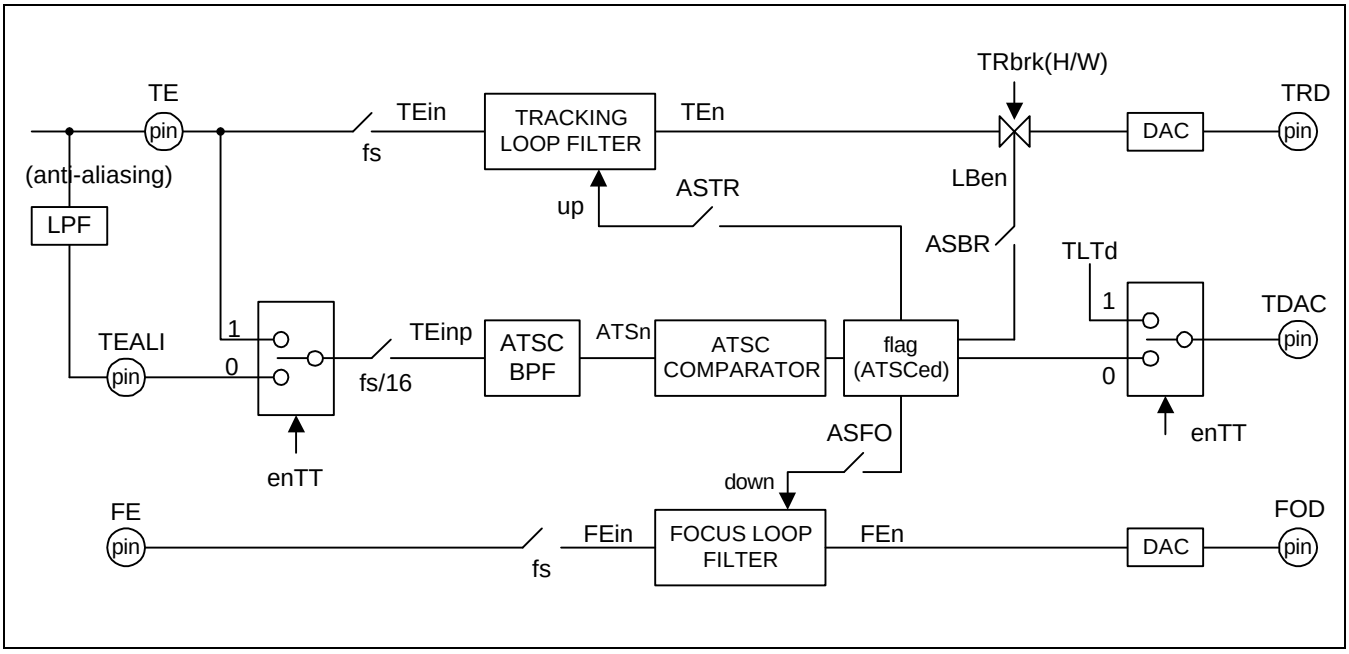
— Input signal : TEALI (TE input for ATSC)

— Output signal: FOD, TRD, TDAC (monitor)

INITIALIZE

(* is default setting)

cmd	bit	MODE Description	L	H	default
HDW	enTT	ATSC BPF input pin select	TILTI (*)	TE	A85900
	enASin	ATSC BPF (shock detection)	internal BPF(*)	external BPF	
TON	TRPI	kick pulse use at tracking pull_in	yes	no(*)	A33600
EME	DSAS	ANTI SHOCK processing	enable	disable(*)	A74F00
	ASFO	Focus gain during the ATSC period	normal	down(*)	
	ASTR	Tracking gain during the ATSC period	normal	up(*)	
	ASBR	Lens brake during the ATSC period	off	on(*)	



— Operation changes depending on the TRPI and DSAS combination.

TRPI	DSAS	Operation Contents
0	0	Track pull-in using kick pulse at off track during ATSC
0	1	Kick pull-in when Mirr is output at off track during play
1	0	select from 3 (ASBR,ASFO,ASTR)
1	1	X (Let stand and leave it to Servo)

— Function combinations when TRPI = "H" and DSAS = "L"

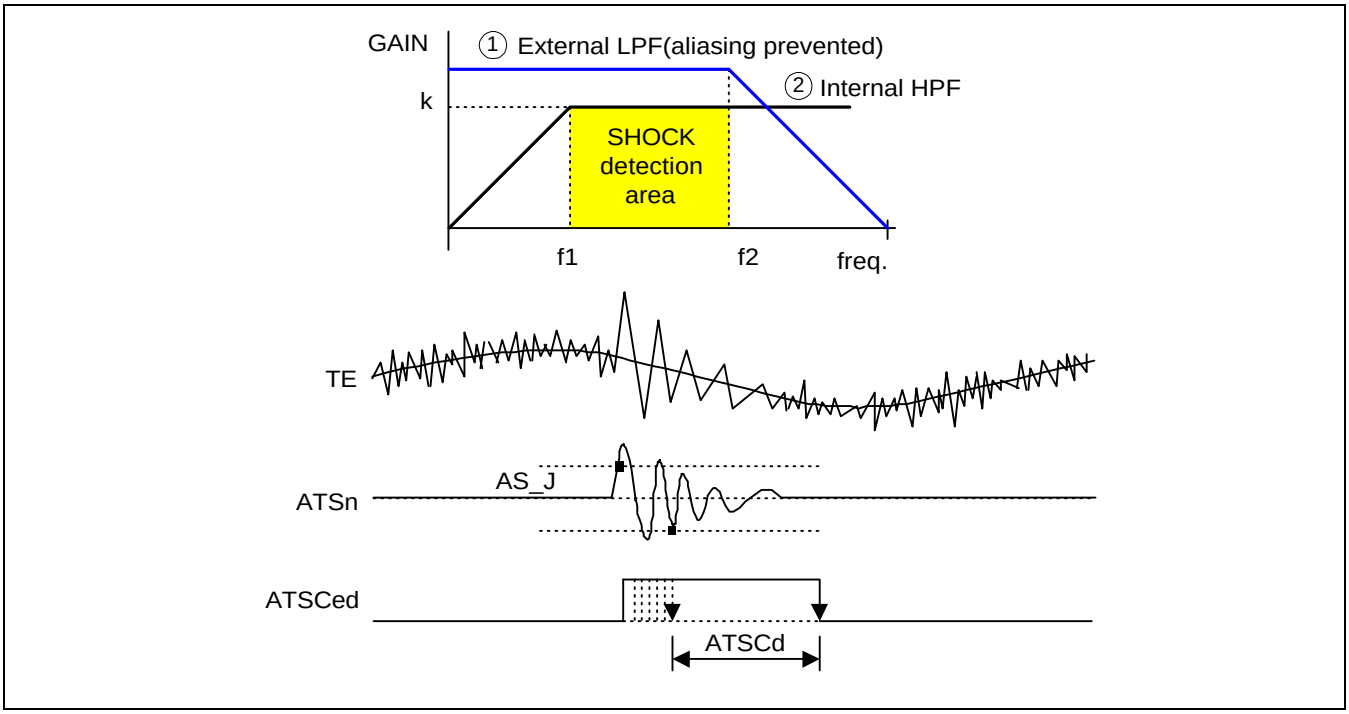
cmd	A741	A742	A743	A744	A745	A746	A747
ASFO	0	0	0	1	1	1	1
ASTR	0	1	1	0	0	1	1
ASBR	1	0	1	0	1	0	1

Related REGISTER

Register	Addres	Function	Command
AS_J	10CB	ATSC comparator threshold level	AFFFFB
ATSCd	004C	Continuous operation time after ATSC	ACFFFB
ATSCk1	00CB	ATSC BPF low frequency pole(f1)	F5FFFF
ATSCk	00CC	ATSC BPF gain	F6FFFF

Operation

TE is filtered to make ATSn, to which a delay is added to make the ATSC signal.



CLV LOCK OFF MEASURES

Summary

If CLV lock is turned off during playback for any reason, the spindle servo becomes unstable, and it can affect the tracking servo, causing an emergency. To prevent such an occurence, you can receive the lock from the data processor to take the appropriate steps to the tracking and sled servo when lock is off.

— Input signal : LOCK

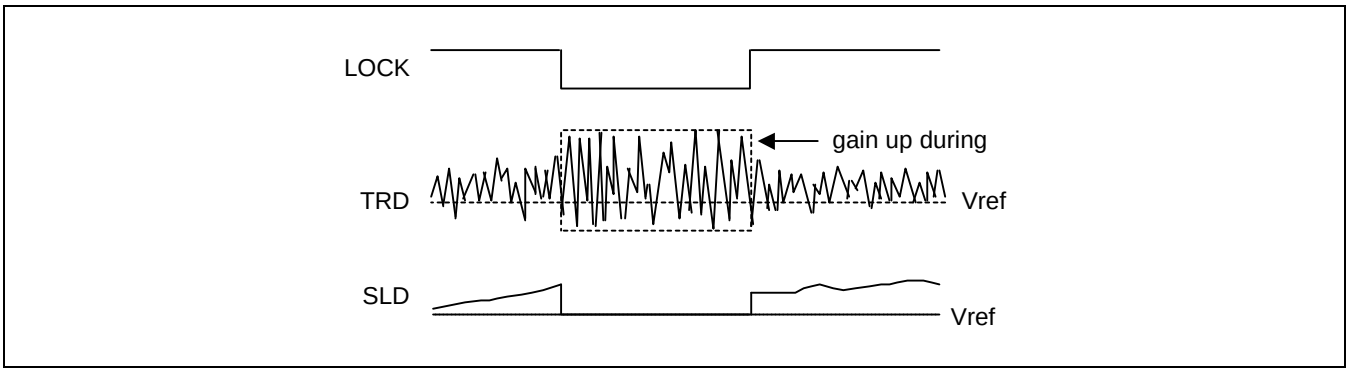
— Output signal : TRD, SLD

INITIALIZE

(* is the default setting)

cmd	bit	MODE Content	L	H	default
FLG	enLOCK	LOCK OFF TRACKING GAIN	normal	up (*)	BA0011
EME	SLST	LOCK OFF SLED STOP	no	yes (*)	A74F00

TIMING DIAGRAM

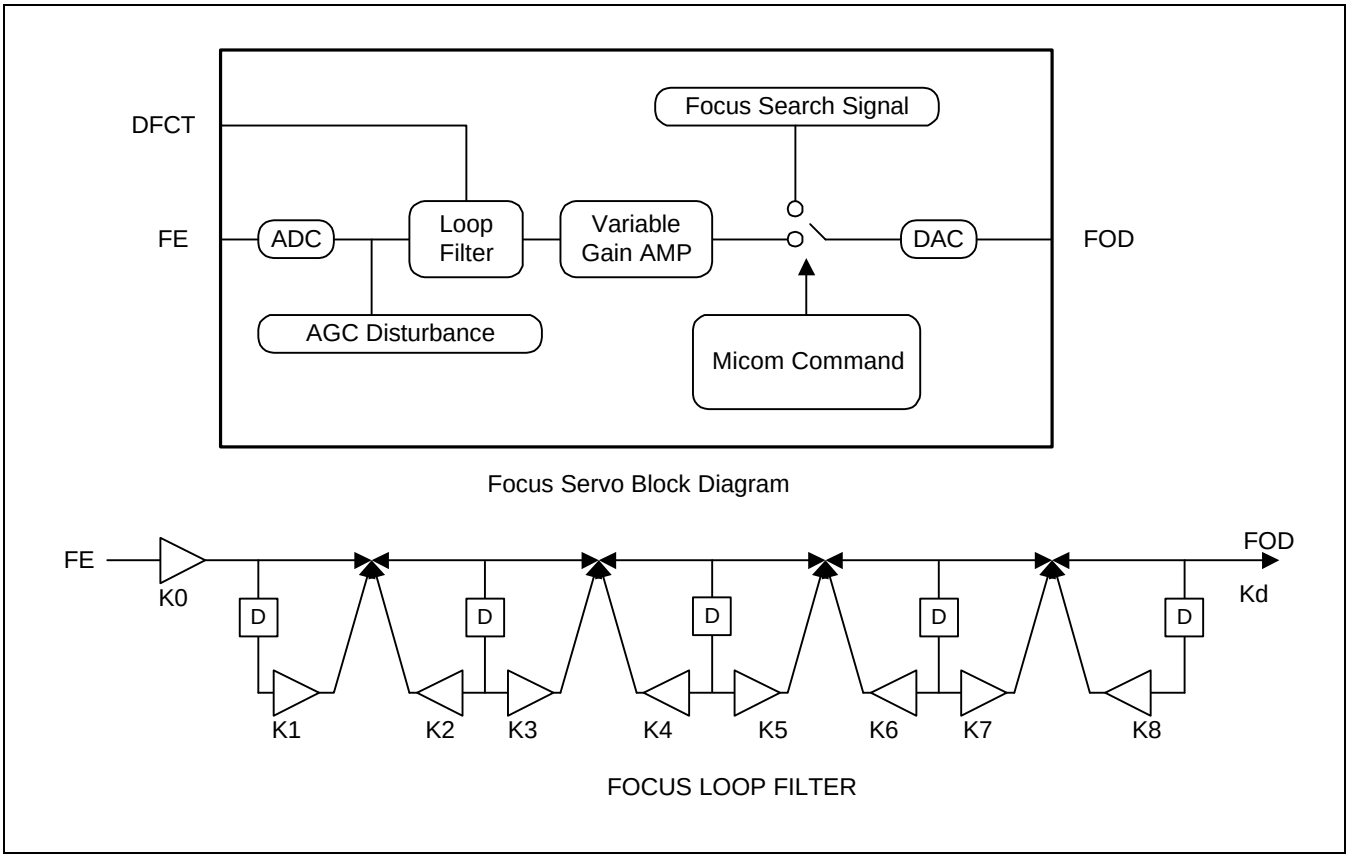


¢°¢° SERVO LOOP FILTER

Focus Servo

Summary

As shown in the focus servo block diagram, the focus error signal from the FE block goes through the compensation filter and variable gain AMP after A/D, then goes through D/A conversion to be output to the FOD/TRD block. The variable gain AMP is automatically selected during auto gain adjustment.



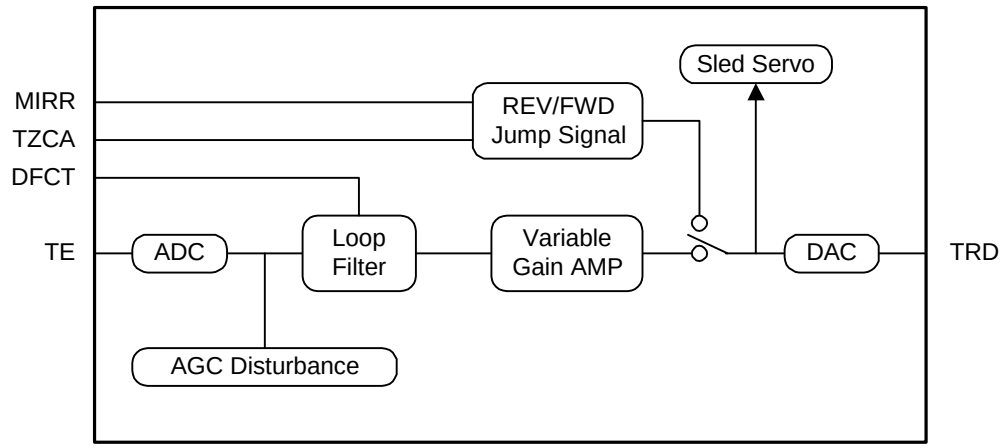
Focus Servo Block Diagram

FOCUS LOOP FILTER

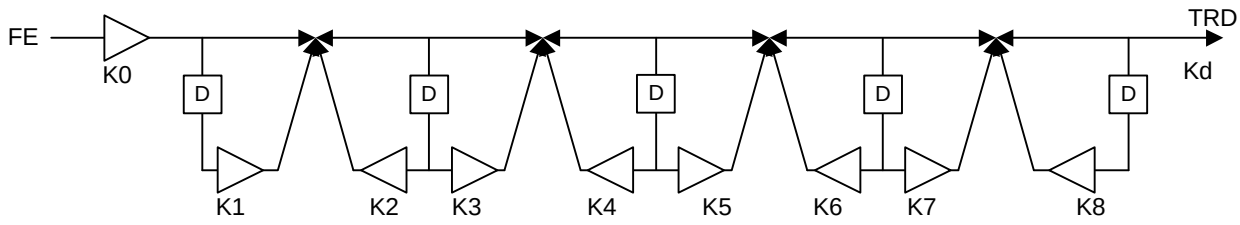
TRACKING SERVO

Summary

As shown in the focus servo block diagram, the focus error signal from the FE block goes through the compensation filter and variable gain AMP after A/D, then goes through D/A conversion to be output to the TRD block. The variable gain AMP is automatically selected during auto gain adjustment.



Tracking Servo Block Diagram

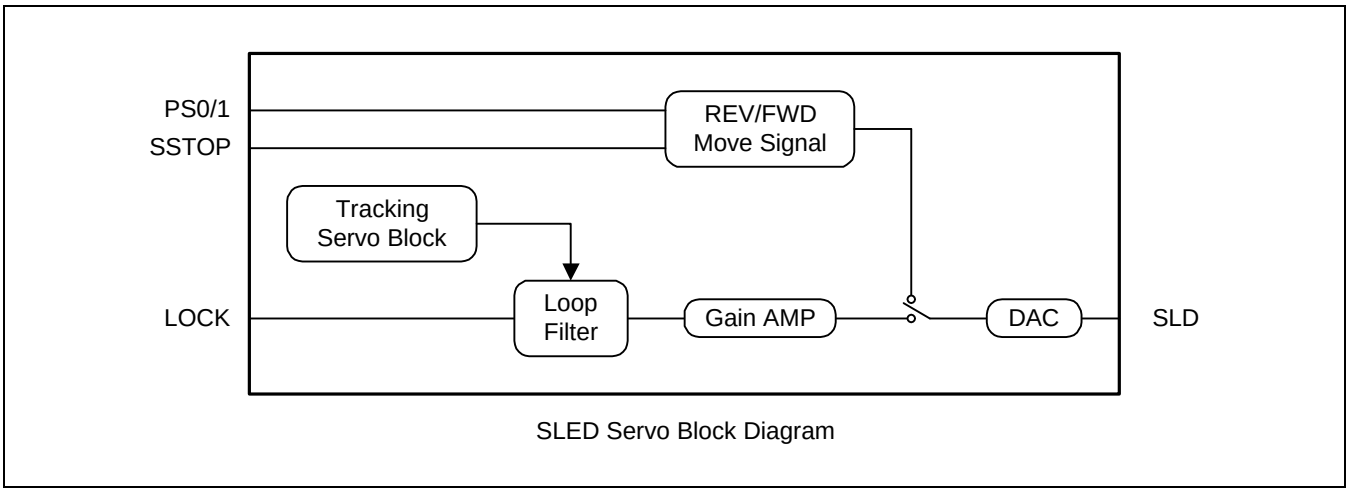


TRACKING LOOP FILTER

SLED SERVO

Summary

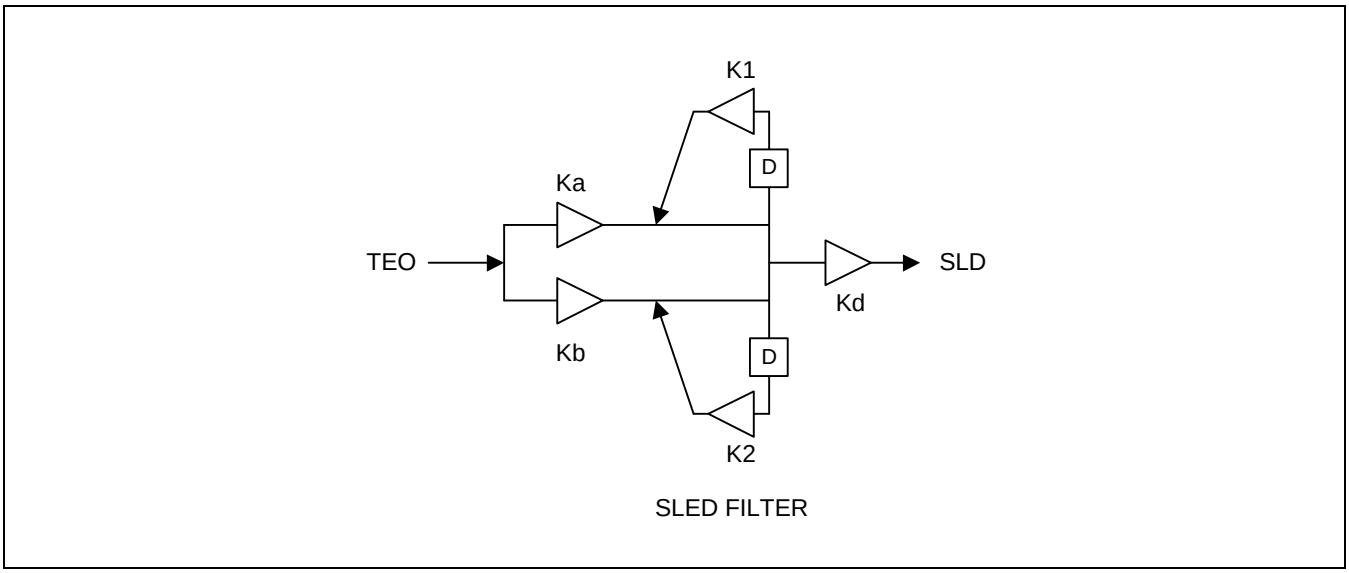
As shown in the sled servo block diagram, the TRD signal input from the tracking servo block goes through the compensation filter and gain AMP, then is D/A converted for outputting into the SLD block.



SLED Servo Block Diagram

FWD/REV

The sled can be moved quickly by using the FG signal of the sled motor from the PSO and PS1. (SLED stop at LOCK off)



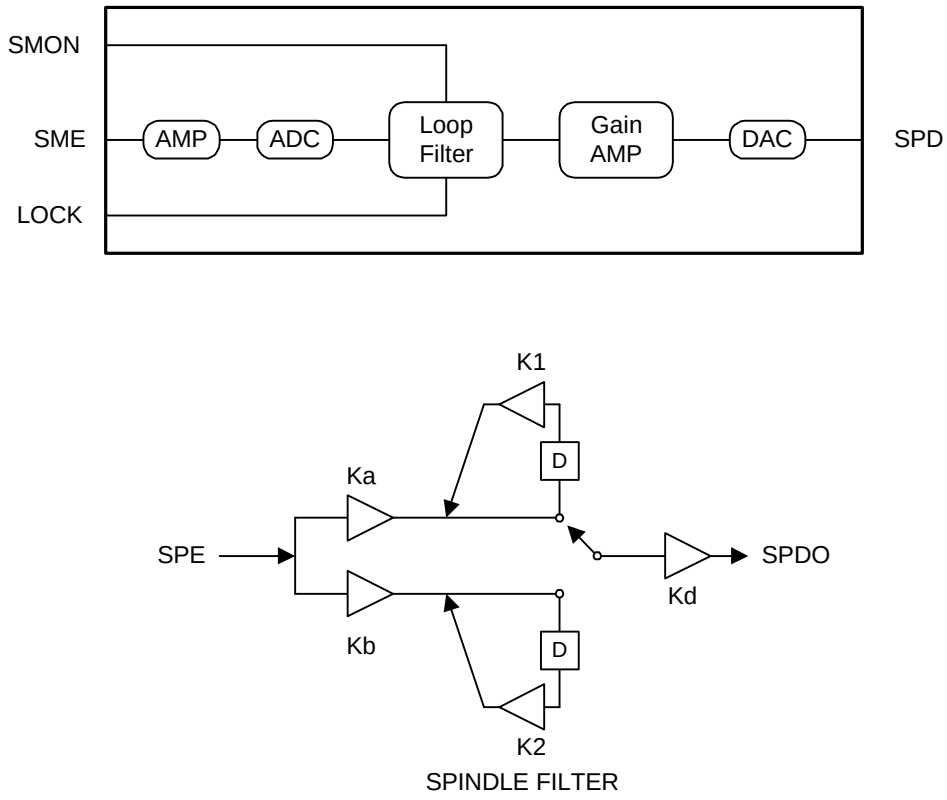
SLED FILTER

SPINDLE SERVO

Summary

In the spindle servo block diagram, the spindle error signal input from DSP goes through the compensation filter and the gain AMP, then is D/A converted to be output into the SPD block.

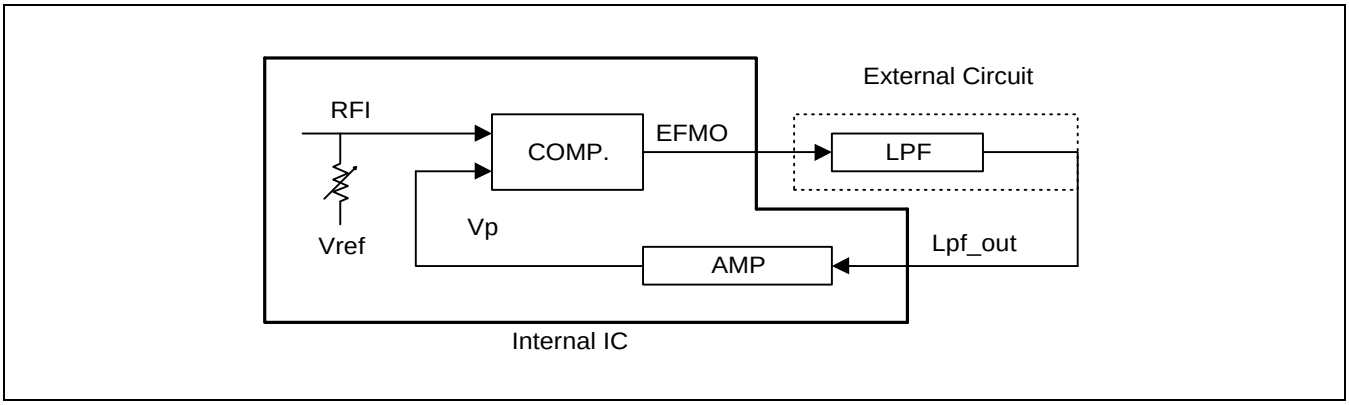
(LOCK = L : reduce loop filter bandwidth with CLV s-mode
LOCK = H : extend loop filter bandwidth with CLV p-mode)



DATA_SLICER CIRCUIT

Summary :

The input signal from RF (3T - 14T) is converted into a pulse waveform of duty 50% and output without regard to Δ Voffset generation.



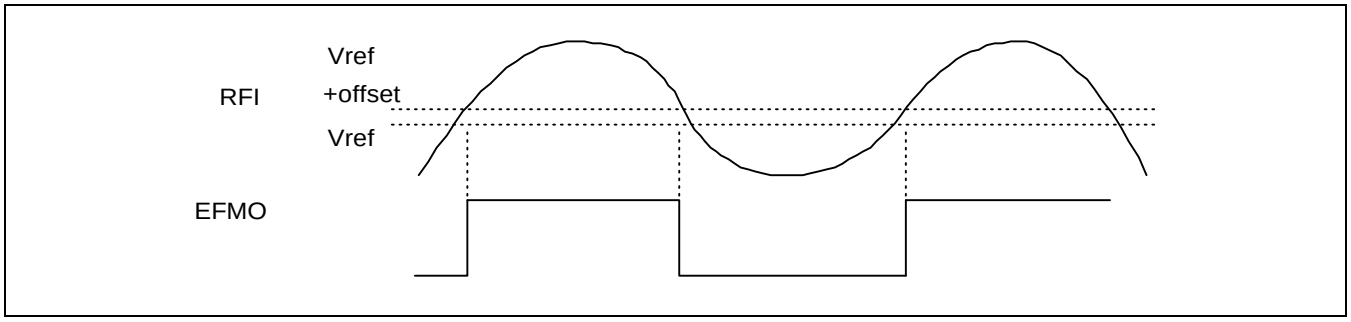
PINS

PIN name	I/O	Description
RFI	I	Analog RF input signal
LPF_DVD	I	Slicing Level Error voltage limited to the LPF_DVD
LPF_CD	I	Slicing Level Error voltage limited to the LPF_CD
EFMO	O	EFM output signal waveform adjusted by comp.

MODE Frequency Inputs (3T reference)

Mode	Frequency
CD *1	720kHz
CD *4	2.88MHZ
CD *8	5.76MHZ
CD *16	11.52MHZ
CD *24	17.28MHZ
DVD *1	4.36MHZ
DVD *2	8.72MHZ
DVD *3	13.08MHZ

Operating Waveform



RFI Input Impedance

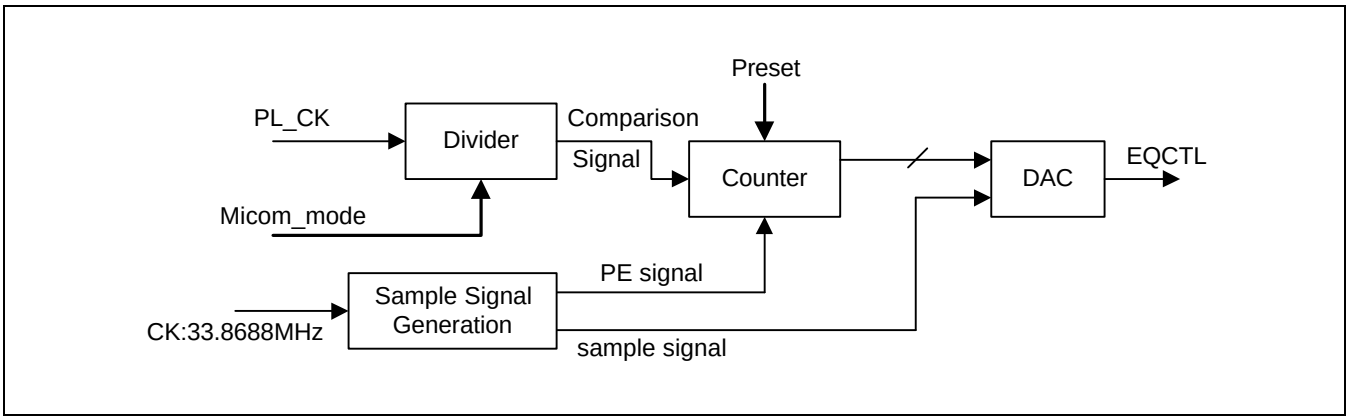
— 6 step Impedance Setting

MICOM Mode	000	001	010	011	100	101
Resistance (kΩ)	40	20	10	5	15	7.5

EQ_CONTROL

Summary

F/V convert that converts frequency into voltage by inputting the clock generated in PLL.



PIN

PIN name	I/O	Description
PL_CK	internal signal	Bit clock generated at PLL according to speed
Micom_mode	I	MICOM interface
CK	I	Main clock (33.8688MHz)
EQCTL	O	Bit clock F/V Output

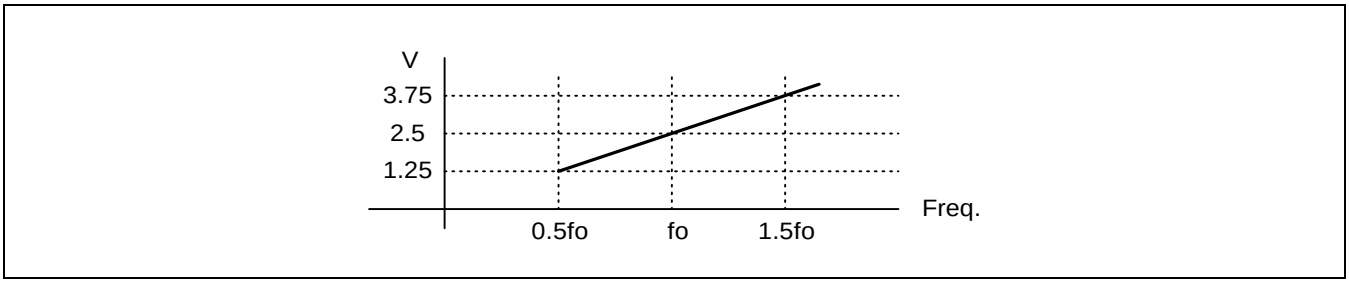
SPEC

— 6step F/V frequency select (CLV reference)

— Input frequency range center frequency ± 50%

— ± 0.25V/± 10%

— Linearity : < ± 7%



Speed and Comparison signal

— Produces a fixed comparison signal using the MICOM speed data and PL_CK from the PLL block.

Speed data		PL_CK [MHz]	N	Comparison signal [MHz]
000	CD*1	4.3218	1	4.3218
001	CD*2	8.6432	2	4.3218
010	CD*4	17.2872	4	4.3218
011	CD*8	34.5744	8	4.3218
100	DVD*1	26.1600	6	4.3600
101	DVD*2	52.3200	12	4.3600

WIDE CAPTURE RANGE PLL

Summary

The channel clock restoration PLL supplies the system clock for restoring the EFM data in the DSP into its original signal components. The EFMI signal from the data slice has the form of RLL (3T - 11T, 14T) code. Restoring the clock in a signal means that you are extracting clocks with a period of T. The PLL being supplied follows the frequency change of the clock existing within 50% of the center frequency, allowing for playback speed improvement at track jump or other points when the data is incontinuous. It can also be used with the CAV control method. The built-in features include the following:

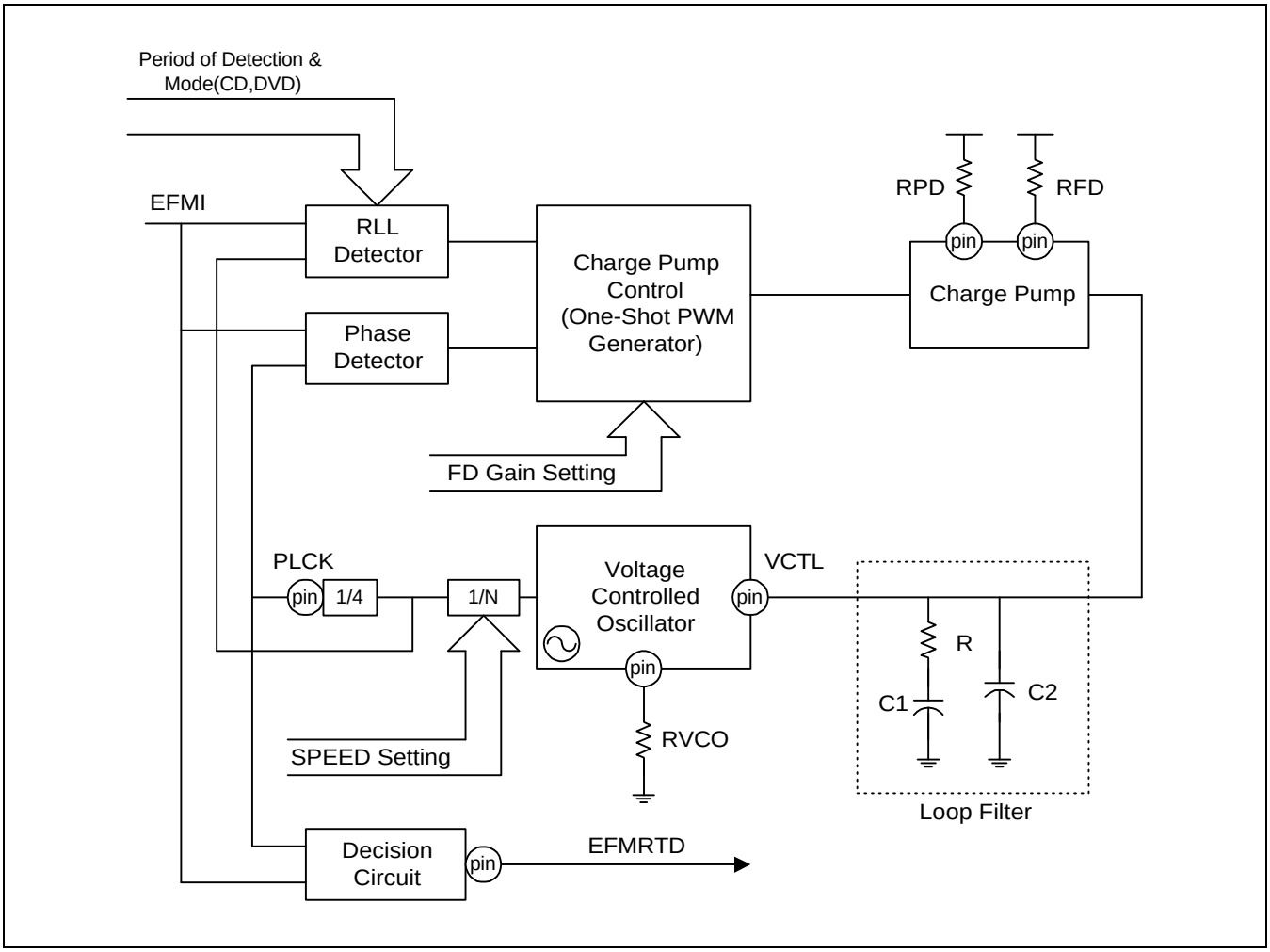
— CD 1/2/4/8x and DVD 1x compatible

— Track jump and disc DFCT through PHOLD pin possible

— Uniform LPF regardless of speed

— Fast tracking through PWM generation during jump control

— PD, FD gain separation control using RPD and RFD (improves safety and speed)



BLOCK Operation

— Frequency detector
Detects the frequency difference between the reference signal(EFM) and the VCO divided by N.

— Phase detector
Detects the phase difference between the reference signal (EFM) and the VCO divided by N.

— Charge pump control
Controls the detected deviance with the 10 PWM (Pulse Width Modulation) outputs.

— Charge pump
Generates a current according to the detected deviance.

— External LPF
Changes the current generated in the charge pump to analog form.

— Voltage Control Oscillator (VCO)
Outputs proportional frequency according to the analog input.

— Programmable frequency divider
Divides the VCO clock output according to the mode set by MICOM.

MICOM COMMAND

MICOM REGISTER MAP

1) For DSP: Micom Write Register & Read/Write Register Table (R/W not indicated; W)

name	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SIGOUTCON	06	-	WFCKOEN	RFCKOEN	PLCKOEN	EFMTRDOEN	CK16MOEN	WDCKOEN	PCDOEN
VITERBI	07	VITON	CKINV	LOCKCON	VITOPT3	VITOPT2	VITOPT1	VITOPT0	CLR_FLAG
CAVCNT1	08	CAVCKSEL1	CAVCKSEL0	-	-	-	CAVVAL10	CAVVAL9	CAVVAL8
CAVCNT2	09	CAVVAL7	CAVVAL6	CAVVAL5	CAVVAL4	CAVVAL3	CAVVAL2	CAVVAL1	CAVVAL0
INTCTL1	0A	DVDIEN	DSIEN	TOSEN	TSCMPEN	ECCIEN	EMPTYEN	OVEREN	UNDEREN
INTCTL2	0B	SBQIEN	MCPEN	-	-	-	-	-	-
INTCTL3	0C	-	-	-	IFRQ2	IFRQ1	IFRQ0	-	CLRINT
SYSCONT1	0D	MRESET	-	-	RCF1	RCF0	DISC2	DISC1	DISC0
USER1CON	0E	WIDEWIN	GFSPRO	SYNCDEC	ISPROT	FNADJ	RFNCON	-	-
USER2CON	OF	ABTH7	ABTH6	ABTH5	ABTH4	ABTH3	ABTH2	ABTH1	ABTH0
DVDDSET	10	-	-	FWSEL1	FWSEL0	FGSEL1	FGSEL0	IGSEL1	IGSEL0
DVDCONTROL1	11	DSCREN	STRST	-	-	INSEN	WNDEN	WNDRT	FCLDS
DVDCONTROL2	12	WRST	TRST	ECCST	ECNEGLT	ECMOD2	ECMOD1	ECMOD0	MCPST
CLVCONTROL1	13	PGAIN1	PGAIN0	SGAIN1	SGAIN0	-	-	-	-
CLVCONTROL2	14	MDSCON1	MDSCON0	PLLC1	PLLC0	-	MDPC	P_RES1	P_RES0
CLVCONTROL3	15	FALTHR1	FALTHR0	RISTHR1	RISTHR0	REFSEL	SERVOC	CLVC1	CLVC0
CLVMODE	16	SDWP	SDWB	-	-	SDCM3	SDCM2	SDCM1	SDCM0
CDPTEST	17	CTMOD4	CTMOD3	CTMOD2	CTMOD1	CTMOD0	nsync	flg_con	cpeak
CDDEFECT	18	fsc_con3	fsc_con2	fsc_con1	fsc_con0	dc_con1	dc_con0	cps1	cps0
TRMODE	19	IFMOD2	IFMOD1	IFMOD0	-	CDIF0	DRATE	-	DVDIF0
CDSPEED	1A	-	-	-	-	-	CDSPD2	CDSPD1	CDSPD0
CDMUTCNT	1B	CBITIN2	CBITIN1	CBITIN0	DGOEN	DEMPHA	MUTE	ZCMT	ATTN
CDCONTROL	1C	PLCKINV	PLCKCON	EFMCON	PCDCON	BYPASS	INFR	-	T3_MODE
ECCREG1	1D	ERAMODF	ERAMODL	maxmod c2f	maxmod c2l	c2eccf	c2eccl	c2err onlyf	c2err onlyl
ECCREG2	1E	-	cdecc	eccmode	c2fgtype[4]	c2fgtype[3]	c2fgtype[2]	c2fgtype[1]	c2fgtype[0]
ECCREG3	1F	jithold	jumphold	-	-	SETFLG[3]	SETFLG[2]	SETFLG[1]	SETFLG[0]
Address Setting on Micom Direct Access Buffer Mode (¡Ø Read/Write)									
WADRH	20	-	-	-	ADR20	ADR19	ADR18	ADR17	ADR16
WADRM	21	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
WADRL	22	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Data Write to Buffer (when MDAB=1)									
WDATA	23	WDT7	WDT6	WDT5	WDT4	WDT3	WDT2	WDT1	WDT0

name	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
JITNLB	24	jitnl7	jitnl6	jitnl5	jitnl4	jitnl3	jitnl2	jitnl1	jitnl0
JITNUB	25	jitnu7	jitnu6	jitnu5	jitnu4	jitnu3	jitnu2	jitnu1	jitnu0
JITRLB	26	jitrl7	jitrl6	jitrl5	jitrl4	jitrl3	jitrl2	jitrl1	jitrl0
JITRUB	27	jitru7	jitru6	jitru5	jitru4	jitru3	jitru2	jitru1	jitru0
JUMPNLB0	28	jumpnl15	jumpnl14	jumpnl13	jumpnl12	jumpnl11	jumpnl10	jumpnl9	jumpnl8
JUMPNLB1	29	jumpnl7	jumpnl6	jumpnl5	jumpnl4	jumpnl3	jumpnl2	jumpnl1	jumpnl0
JUMPNUB0	2A	jumpnu15	jumpnu14	jumpnu13	jumpnu12	jumpnu11	jumpnu10	jumpnu9	jumpnu8
JUMPNUB1	2B	jumpnu7	jumpnu6	jumpnu5	jumpnu4	jumpnu3	jumpnu2	jumpnu1	jumpnu0
JUMPRLB0	2C	jumprl15	jumprl14	jumprl13	jumprl12	jumprl11	jumprl10	jumprl9	jumprl8
JUMPRLB1	2D	jumprl7	jumprl6	jumprl5	jumprl4	jumprl3	jumprl2	jumprl1	jumprl0
JUMPRUB0	2E	jumpru15	jumpru14	jumpru13	jumpru12	jumpru11	jumpru10	jumpru9	jumpru8
JUMPRUB1	2F	jumpru7	jumpru6	jumpru5	jumpru4	jumpru3	jumpru2	jumpru1	jumpru0
Buffering Start Sector Unit Number									
WBAH	30	-	-	-	-	-	-	B9	B8
WBAL	31	B7	B6	B5	B4	B3	B2	B1	B0
ECC Start Block Unit Number									
WEAH	32	-	-	-	-	-	-	B9	B8
WEAL	33	B7	B6	B5	B4	B3	B2	B1	B0
Transfer Start Sector Unit Number									
WTAH	34	-	-	-	-	-	-	B9	B8
WTAL	35	B7	B6	B5	B4	B3	B2	B1	B0
Over Threshold Size (Sector Unit Number) (¡Ø Read/Write)									
OTSH	36	-	-	-	-	-	-	B9	B8
OTSL	37	B7	B6	B5	B4	B3	B2	B1	B0
Under Threshold Size (Sector Unit Number) (¡Ø Read/Write)									
UTSH	38	-	-	-	-	-	-	B9	B8
UTSL	39	B7	B6	B5	B4	B3	B2	B1	B0

name	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Transmission Sector Number Assignment (¡Ø Read/Write)									
TNH	3A	B15	B14	B13	B12	B11	B10	B9	B8
TNL	3B	B7	B6	B5	B4	B3	B2	B1	B0
MICOM Buffer Size Assignment (¡Ø Read/Write)									
MBS	3C	-	-	-	-	B3	B2	B1	B0
Decoder Direct Data Block Copy Source Sector Addresses (¡Ø Read/Write)									
BCPSH	3D	-	-	-	-	-	-	B9	B8
BCPSL	3E	B7	B6	B5	B4	B3	B2	B1	B0
RESERVED (3F)									
Decoder Direct Data Block Copy Target Sector Addresses (¡Ø Read/Write)									
BCPTH	40	-	-	-	-	-	-	B9	B8
BCPTL	41	B7	B6	B5	B4	B3	B2	B1	B0
Descramble Start Sector Unit Number (¡Ø Read/Write)									
WDAH	42	-	-	-	-	-	-	B9	B8
WDAL	43	B7	B6	B5	B4	B3	B2	B1	B0
	44	-	-	TSTWRD	ECTEST	NMON3	NMON2	NMON1	NMON0
User Register2	45	MONITOR3	MONITOR2	MONITOR1	MONITOR0	MPRSTZ	TST ENDMUX	TST POREND	TST PIREND
	46	REGEG	ACKEG	STREG	TOSEG	DTREG	-	TSTID	TSTIDSY
RESERVED (47 - 49)									

2) For DSP: Micom Read Register & Read/Write Register Table (R/W not indicated; R)

name	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
INTSTAT1	4A	DVDSINT	DSINT	TOSINT	TRSCMPLT	ECCMPLT	EMPTY	OVER	UNDER
INTSTAT2	4B	SBQINT	MCPINT	-	-	-	-	-	-
ERRSTAT	4C	EIDERR	DSIERR	IDCONERR	-	ECCERR	EDCFLG	-	SBQERR
DVDSTATUS	4D	-	-	-	-	SYOK	NOSY	ILSY	-
DVDSVSTAT	4E	-	LOCK	GFS	-	-	-	-	-
RESERVED (4F)									
CDSUBQ	50	SBQ79	SBQ78	SBQ77	SBQ76	SBQ75	SBQ74	SBQ73	SBQ72
	↓	↓	↓	↓	↓	↓	↓	↓	↓
	59	SBQ07	SBQ06	SBQ05	SBQ04	SBQ03	SBQ02	SBQ01	SBQ00
RESERVED (5A - 5F)									
SEEKIDADR	60	SID31	SID30	SID29	SID28	SID27	SID26	SID25	SID24
	61	SID23	SID22	SID21	SID20	SID19	SID18	SID17	SID16
	62	SID15	SID14	SID13	SID12	SID11	SID10	SID09	SID08
	63	SID07	SID06	SID05	SID04	SID03	SID02	SID01	SID00
TRANSIDADR	64	TID31	TID30	TID29	TID28	TID27	TID26	TID25	TID24
	65	TID23	TID22	TID21	TID20	TID19	TID18	TID17	TID16
	66	TID15	TID14	TID13	TID12	TID11	TID10	TID09	TID08
	67	TID07	TID06	TID05	TID04	TID03	TID02	TID01	TID00
RESERVED (68 - 6F)									
Address Reading on Micom Direct Access Buffer Mode (¡Ø Read/Write)									
RADRH	70	-	-	-	ADR20	ADR19	ADR18	ADR17	ADR16
RADRM	71	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
RADRL	72	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Data Read from Buffer									
RDATA	73	RDT7	RDT6	RDT5	RDT4	RDT3	RDT2	RDT1	RDT0
RESERVED (74 - 7F)									

name	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Buffering End Sector Unit Number									
RWAH	80	-	-	-	-	-	-	B9	B8
RWAL	81	B7	B6	B5	B4	B3	B2	B1	B0
ECC End Sector Unit Number									
REAH	82	-	-	-	-	-	-	B9	B8
REAL	83	B7	B6	B5	B4	B3	B2	B1	B0
Transferring End Sector Unit Number									
RTAH	84	-	-	-	-	-	-	B9	B8
RTAL	85	B7	B6	B5	B4	B3	B2	B1	B0
DSI Unit Number									
DSIH	86	-	-	-	-	-	-	B9	B8
DSIL	87	B7	B6	B5	B4	B3	B2	B1	B0
Descramble End Sector Unit Number									
RDAH	88	-	-	-	-	-	-	B9	B8
RDAL	89	B7	B6	B5	B4	B3	B2	B1	B0
Remaining Data Size(SECTOR UNIT Number)									
RDSH	8A	-	-	-	-	--	-	B9	B8
RDSL	8B	B7	B6	B5	B4	B3	B2	B1	B0
RESERVED (8C - 93)									
ECC End ID Address									
EEIDA	94	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
	95	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
	96	ID15	ID14	ID13	ID12	ID11	ID10	ID09	ID08
	97	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
RESERVED (98 - 9B)									
DSI ID Address									
DSIDA	9C	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
	9D	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
	9E	ID15	ID14	ID13	ID12	ID11	ID10	ID09	ID08
	9F	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00

3) For Servo ..Micom Write Register & Read/Write Register Table

Command		DHH				DHL				DL	com-
Name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit7 - bit0	ment
STPcmd	A0	STOP	ABRT	IDLE	LDX	0	0	0	0	-	-
DDTcmd	A1	/AUTO	/UPDN	/FIGA	/FBAL	/FoFa	FSP2	FSP1	FSP0	-	FSspd
FONcmd	A2	LYRX	FMthd	/FOPI	FSPC	0	0	0	0	-	FONc
TONcmd	A3	TLRX	/SLSV	/TRPI	TOLB	MTLB	SFOG	STRG	DGs	-	TONc
SLDcmd	A4	HOME	SMOV	SPLY	0	0	0	0	0	-	-
JMPcmd	A5	DIR	JPM1	JPM0	JIT2	JIT1	JIT0	JPD9	JPD8	JPD7 - JPD0	JMPc
CDScmd	A6	WHIN	STSP	FSOS	DPSI	PLLS	JPCC	JPFC	FSHF	-	INIc (15-9)
EMEcmd	A7	FDOL	SLST	RPT	upFv	DSAS	ASFO	ASTR	ASBR	-	EMEc
HDWcmd	A8	enTT	LIM	enASin	SNS	PCUP	/DOFO	/DOTR	XTAL	-	HDWc
INIcmd	A9	SLDO	JPCK	TKJM	JPEC	BJJM	BTS	SMM	SLB	-	iNic
MSCcmd	AA	MD11	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3-MD0 MSS3-MSS0	BANK0 55
SPDcmd	AB	DKS1	DKS0	0	/VCT	0	0	SPD1	SPD0	-	SPDc
TMScmd	AC	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3-TD0 TMS3-TMS0	BANK0 41
OKScmd	AD	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3-OD0 OKS3-OKS0	BANK1B0
AJKcmd	AE	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3-AD0 AJS3-AJS0	BANK0 24
LEScmd	AF	LD11	LD10	LD9	LD8	LD7	LD6	LD5	LD4	LD3-LD0 LES3-LES0	BANK1 C0

Command		DHH				DHL				DL	com-ment
Name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit7 - bit0	
AARWcmd	B0	AA11	AA10	AA9	AA8	AA7	AA6	AA5	AA4	AA3-AA0 AAS3-AAS0	
OFAcmd	B1	FTS	LDOF	U/B	0	0	0	0	0		
FBAcmd	B2										
TBAcmd	B3	/TIGA	/RPTB	0	0	0	0	0	0		
FGAcmd	B4										
TGAcmd	B5										
DPAcmd	B6										
EFMCcmd	B7	LPFS	EGA2	EGA1	EGA0	RES2	RES1	RES0	0	ODA5-0DA0	
FcScmd	B8				HW04	HW03	HW02	HW01	HW00		
SQJcmd	B9	JPLY	0	0	0	0	0	0	0		
FLGcmd	BA	stp	Fptmg	enHYS	HOME	ituJ	TSV	SSV	enTJn		
		DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0		
		DFCTed	ATSCed	tbmthd	fbmthd	enASin	FSend	enSPi	enLOCK		
SNSCcmd	BB	RWB	0	NORM	FTCK	0	0	0	BANK	MOD7 -MOD0	
DPRWcmd	BC	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3 - DD0 st6,DPS2-0	
FTSTcmd	BD				WTF				WFF		
RamRcmd	BE	NEXT	0	0	BANK	0	0	0	PAGE	RAM7 - RAM0	
RamWcmd	BF	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7 - RD0	

Command		DHH				DHL				DL	com-
Name	Address	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7 - DL0	ment
Fxkcmd	C0 : D3	RWB	Fxk 14	Fxk 13	Fxk 12	Fxk 11	Fxk 10	Fxk 9	Fxk 8	Fxk7 - Fxk0	
SPKxcmd	D4 : D8	RWB	SPk 14	SPk 13	SPk 12	SPk 11	SPk 10	SPk 9	SPk 8	SPk7 - SPk0	
SRDcmd	D9										
SLKxcmd	DA : DE	RWB	SLk 14	SLk 13	SLk 12	SLk 11	SLk 10	SLk 9	SLk 8	SLk7 - SLk0	
PLLcmd	DF	IDACN[5:0]							SHIFT_G		
		IDACP[5:0]						PLOCKSL	IS_UP		
		RARR[2:0]			VARI_G[2:0]				VCOSL		
		PWM[7:0]									
Txkcmd	E0 : EF	RWB	THk 14	THk 13	THk 12	THk 11	THk 10	THk 9	THk 8	THk7 - THk0	
	F1 : F3	RWB	TLK 14	TLk 13	TLk 12	TLk 11	TLk 10	TLk 9	TLk 8	TLk7 - TLk0	
MNIcmd	F4	MNI1	MNI0	CSEL	DSEL	DCUT[3:0]					
ASKxcmd	F5	RWB	AHK14	AHk13	AHk12	AHk11	AHk10	AHk9	AHk8	AHk7 - ALk0	
	F6	RWB	ALK14	ALk13	ALk12	ALk11	ALk10	ALk9	ALk8	AHk7 - ALk0	
EVAcmd	F7	UP	DOWN								
TTKxcmd	F8 : FA	RWB	TTK 14	TTk 13	TTk 12	TTk 11	TTk 10	TTk 9	TTk 8	TTk7- TTk0	
FTGcmd	FB	Fchg	DWN	Tchg	UP						
AVkcmd	FC	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4-AD0 AVS2-AVS0	
xGkxcmd	FD : FF	RWB	GK 14	Gk 13	Gk 12	Gk 11	Gk 10	Gk 9	Gk 8	Gk7 - Gk0	

MICOM REGISTER DESCRIPTION

1) DSP Part: MICOM Write register & Read/Write Register (R/W Not Indicated; W)

06	Pin Signal Output Control			
bit	**Name**	**Description**		**def.**
7	-		Reserved	
6	WFCKOEN		Pin 90 WFCK output control	0
		1	Output Enable	
		0	Output Disable	
5	RFCKOEN		Pin 91 RFCK output control	0
		1	Output Enable	
		0	Output Disable	
4	PLCKOEN		Pin 92 PLCK output control	0
		1	Output Enable	
		0	Output Disable	
3	EFMTRDOEN		Pin 97 EFMTRD output control	0
		1	Output Enable	
		0	Output Disable	
2	CK16MOEN		Pin 100 CK16M output control	0
		1	Output Enable	
		0	Output Disable	
1	WDCKOEN		Pin 124 WDCK output control	0
		1	Output Enable	
		0	Output Disable	
0	PCDOEN		Pin 139-146 PCD [7:0] output control	0
		1	Output Enable	
		0	Output Disable	

07			VITERBI	
bit	**Name**		**Description**	**def.**
7	VITON		Test MICOM command. Make it '0' during normal play.	0
6	CKINV		Test MICOM command. Make it '0' during normal play.	0
5	LOCKCON		Test MICOM command. Make it '0' during normal play.	0
4	VITOPT3		Test MICOM command. Make it '0' during normal play. '0':EFM_flg=SLICE output EFM signal, '1':EFM_flg=PLCK Latched EFM signal	0
3	VITOPT2		Test MICOM command. Make it '0' during normal play. '0' : BM1_flg = /PLCK, '1' : BM1_flg = PLCK	0
2	VITOPT1		Test MICOM command. Make it '0' during normal play. '0':BM=EFM_flg & BM1_flg, '1':BM=EFM_flg	0
1	VITOPT0		Test MICOM command. Make it '0' during normal play. '0': VIT output is triggered at the PLCK neg edge '1': VIT output is triggered at the PLCK pos edge	0
0	CLR_FLAG		Test MICOM command. Make it '0' during normal play.	0

CAVCNT1,2 : CAV Control Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
08	CAVCK SEL1	CAVCK SEL0	-	-	-	CAVVAL10	CAVVAL9	CAVVAL8
09	CAVVAL7	CAVVAL6	CAVVAL5	CAVVAL4	CAVVAL3	CAVVAL2	CAVVAL1	CAVVAL0
Reset value	0	0	0	0	0	0	0	0

CAVCKSEL(1:0) : Reference clock setting for CAV control

CAVVAL(10:0) : Initial value setting for CAV control

CAVCK SEL1	CAVCK SEL0	Nck	Setting range of Number of Disc rotations	
			DVD	CD
0	0	8	1372.4 - 2746.5	215.2 - 430.7
0	1	4	686.2 - 1372.4	107.6 - 215.2
1	0	2	343.1 - 686.2	53.8 - 107.6
1	1	1	171.5 - 343.1	26.9 - 53.8

The disc rotation speed in CAV mode is set by the following equation.

DISC RPM = fsys × 10 × Nck / 1024 / CAV_REF

where fsys : System Clock FOR DVD(27 MHz), FOR CD(33.8688/8 MHz)
Nck : Clock division ratio set by CAVCKSEL[1:0]
(8 → 128 division,4 → 256 division,2 → 512 division,1 → 1024 division)
CAV_REF : Exists between 1408 ¡Â CAV_REF ¡Â 1537 through the value calculated by (1537- Ncarv)

$$CAV\_REF = \frac{XTAL \times 10 \times Nck}{1024 \times RPM}$$

where XTAL: DVD (XTL1) , CD (CK33M1/8)

Example) CAVVAL(10:0) value for 1440 RPM

$$CAV\_REF = \frac{26.16MHz \times 10 \times 8}{1024 \times 1440} = 1419.27 \cong 1419$$

CAVVAR = 1537 - 1419 = 118 = 76H

⇒ Be aware that the CAV_REF value calculated with the above equation can change with fsys.

0A	INTCTL1 : Interrupt Control Register 1 (DVD Interrupt Masking Register)			
bit	**Name**		**Description**	**def.**
7	DVDIEN		DVD ID-sync Interrupt request enable DVD Decoder-generated ID-sync Interrupt Restricted/Unrestricted control bit	0
		1	Enable	
		0	Disable	
6	DSIEN		DSI INTERRUPT	0
		1	Enable	
		0	Disable	
5	TOSEN		Top of Sector Interrupt request enable. Interrupt restrict/unrestrict control bit that informs of the first data in the sector among the data to be sent to the A/V decoder or host in the DVD decoder	0
		1	Enable	
		0	Disable	
4	TSCMPTEN		Transfer Complete Interrupt request enable. Control bit that generates an interrupt signal when all the number of bytes (TNH,L) have been sent during DVDROM use.	0
		1	Enable	
		0	Disable	
3	ECCIEN		ECC Complete Interrupt request enable. Enable / Disable control bit for the ECC complete interrupt in the DVD Decoder	0
		1	Enable	
		0	Disable	
2	EMPTYEN		Buffer Memory Empty Interrupt (for Transfer) request enable	0
		1	Enable	
		0	Disable	
1	OVEREN		Buffer Memory OVER Interrupt request enable. Interrupt request enable (hysteresis) generated when the filled area in the buffer memory is above the micom-specified over threshold size (OTS)	0
		1	Enable	
		0	Disable	
0	UNDEREN		Buffer Memory UNDER Interrupt request enable. Interrupt request enable (hysteresis) generated when the filled area in the buffer memory is above the micom-specified under threshold size.	0
		1	Enable	
		0	Disable	

0B	INTCTL2 : Interrupt Control Register 2 (CD interrupt Masking Register)			
bit	**Name**	**Description**		**def.**
7	SBQIEN		CD Subcode-sync Interrupt request enable. Enable/Disable control bit of the Subcode-sync interrupt generated in the CD decoder	0
		1	Enable	
		0	Disable	
6	MCPEN		Micom Block Copy Mode	0
		1	Enable	
		0	Disable	
5	-			x
4	-			x
3	-			x
2	-			x
1	-			x
0	-			x

0C	INTCTL3 : Interrupt control Register 3			
bit	**Name**	**Description**		**def.**
7	**-**			x
6	**-**			x
5	**-**			x
4	IFRQ2	IFRQ2-0 : Interrupt Request Frequency Specified Register(Applicable to only DVDSINT)		0
3	IFRQ1			0
2	IFRQ0			0
1	-			x
0	CLRINT		Interrupt Clear register. Decides on whether the micom will clear the interrupt register after reading the interrupt status register	1
		1	clear allow	
		0	clear not allow	

IFRQ2	IFRQ1	IFRQ0	Interrupt number/ID sector number
0	0	0	1/ 1 ID Sector
0	0	1	1/ 2 ID Sectors
0	1	0	1/ 4 ID Sectors
0	1	1	1/ 8 ID Sectors
1	0	0	1/16 ID Sectors
other			Reserved

<table>
<tr><th>0D</th><th colspan="3">SYSCONT1 : System Control Register 1</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>7</td><td>MRESET</td><td></td><td>Software Reset - Resets the Z-Decoder(Same as ZRST)).
After the micom resets the Z-decoder, the decoder automatically sets to '1' after performing the above function.</td><td>1</td></tr>
<tr><td></td><td></td><td>1</td><td>Reset off</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Reset on</td><td></td></tr>
<tr><td>6</td><td>-</td><td></td><td></td><td>x</td></tr>
<tr><td>5</td><td>-</td><td></td><td></td><td>x</td></tr>
<tr><td>4</td><td>RCF1</td><td colspan="2" rowspan="2">RCF1-0 : RAM Configuration -- Determines the Buffer Size
<table><tr><th>RCF1</th><th>RCF0</th><th>DRAM Configuration</th></tr><tr><td>0</td><td>0</td><td>4MBits</td></tr><tr><td>0</td><td>1</td><td>8MBits</td></tr><tr><td>1</td><td>0</td><td>N.A</td></tr><tr><td>1</td><td>1</td><td>16MBits</td></tr></table></td><td>0</td></tr>
<tr><td>3</td><td>RCF0</td><td>0</td></tr>
<tr><td>2</td><td>DISC2</td><td colspan="2" rowspan="3">Register for Z-decoder control.
DISC2-0 : Identifies the current disc type
<table><tr><th>DISC2</th><th>DISC1</th><th>DISC0</th><th>DISC type</th></tr><tr><td>1</td><td>0</td><td>0</td><td>DVD</td></tr><tr><td>1</td><td>1</td><td>0</td><td>DVD-ROM</td></tr><tr><td>0</td><td>0</td><td>0</td><td>CD-DA</td></tr><tr><td>0</td><td>0</td><td>1</td><td>V-CD</td></tr><tr><td>0</td><td>1</td><td>0</td><td>CD-ROM</td></tr><tr><td></td><td>other</td><td></td><td>Reserved</td></tr></table></td><td>1</td></tr>
<tr><td>1</td><td>DISC1</td><td>0</td></tr>
<tr><td>0</td><td>DIS0</td><td>0</td></tr>
</table>

0E	USERCONT1 : USER Control Register1 (Sync Control)			
bit	**Name**	**Description**		**def.**
7	WIDEWIN		Synchronized protection WINDOW control	1
		1	When the frame sync is not generated insertion number N times, specified in the protection window, it detects the sync by setting the widest protection window. When the sync is detected, it immediately synchronizes the window. If the window with a set width cannot detect protection, it immediately cancels the window.	
		0	Finds the sync by immediately cancelling the protection window without the wide window mode.	
6	GFSPRO		Good Frame Sync Dectection Condition	1
		1	Detection Sync and insertion Sync completely match	
		0	The difference between the detection sync and insertion sync is ± 1	
5	SYNCDEC		Frame Sync detection condition	1
		1	Sync detection through sync code (32 bit)	
		0	Sync detection using a special pattern (228bit)	
4	ISPROT		ID Sync protection start condition (After SYSTEM RESET, set to low.)	0
		1	ID Sync protection start immediately after sector sync detection	
		0	After the frame sync protection starts, the ID sync protection starts if the ID sync is detected in the expected frame Frame Number(FN) match: SO detection in FN0	
3	FNADJ		Frame Number(Address) compensation condition. FRAME SYNC must continue, but, if not, converts to insertion mode	1
		1	Counter value corrected when the difference between the frame number and frame counter value is ± 5	
		0	Counter value corrected when the difference between the frame number and frame counter value is ± 2	
2	RFNCON		Correct the frame number to the detected number. Frame sync must continue, but , if not, converts to insertion mode	1
		1	Frame Number correction (absolutely correct if the detected Frame Number is detected 3 times)	
		0	Frame Number correction (according to the FNADJ condition)	
1	-			x
0	-			x

0F	USERCONT2 : USER Con. Register2 (Channel Clock PLL Control)		
bit	**Name**	**Description**	**def.**
7	ABTH7	Generates a flag during the output of the L-Ch/R-Ch Serial Data when the average value (abth) specified to ABTH[7:0] and the absolute value (|(LX1)-(LX2)|) of the input data are large. ex) If Flag Pattern is Following	1
6	ABTH6	0 0 1 1 0 0 <- Flag	1
5	ABTH5	|L0-L1| |L1-L2| |L2-L3| |L3-L4| |L4-L5| |L5-L6| <- Data	1
4	ABTH4	=> L3 = (L2+L4)/2	1
3	ABTH3	0 0 1 1 1 0 <- Flag	0
2	ABTH2	|L0-L1| |L1-L2| |L2-L3| |L3-L4| |L4-L5| |L5-L6| <- Data	0
1	ABTH1	=> L3 = (L2+L5)/2,	0
0	ABTH0	L4 = (L3+L5)/2	0

<table>
<tr><td>10</td><td colspan="3">DVDDSET : DVD Decoder set (Sync Detect Condition)</td></tr>
<tr><td>bit</td><td>Name</td><td>Description</td><td>def.</td></tr>
<tr><td>7</td><td>-</td><td></td><td>x</td></tr>
<tr><td>6</td><td>-</td><td></td><td>x</td></tr>
<tr><td>5</td><td>FWSEL1</td><td rowspan="2">Frame Sync Protection Window Interval Setting
<table><tr><td>FWSEL1</td><td>FWSEL0</td><td>Frame Sync Protection Window (DVD)</td><td>Frame Sync Protection Window (CD)</td></tr><tr><td>0</td><td>0</td><td>± 6 clock</td><td>± 3 clock</td></tr><tr><td>0</td><td>1</td><td>± 12 clock</td><td>± 6 clock</td></tr><tr><td>1</td><td>0</td><td>± 20 clock</td><td>± 10 clock</td></tr><tr><td>1</td><td>1</td><td>± 24 clock</td><td>± 12 clock</td></tr></table></td><td>0</td></tr>
<tr><td>4</td><td>FWSEL0</td><td>0</td></tr>
<tr><td>3</td><td>FGSEL1</td><td rowspan="2">Frame Sync inserted Frame Number
<table><tr><td>FGSEL1</td><td>FGSEL0</td><td>Frame Sync inserted Frame Number</td></tr><tr><td>0</td><td>0</td><td>4 Frame</td></tr><tr><td>0</td><td>1</td><td>13 Frame</td></tr><tr><td>1</td><td>0</td><td>16 Frame</td></tr><tr><td>1</td><td>1</td><td>28 Frame</td></tr></table></td><td>0</td></tr>
<tr><td>2</td><td>FGSEL0</td><td>0</td></tr>
<tr><td>1</td><td>IGSEL1</td><td rowspan="2">ID Sync inserted Sector Number
<table><tr><td>IGSEL1</td><td>IGSEL0</td><td>ID Sync inserted Sector Number</td></tr><tr><td>0</td><td>0</td><td>1 Sector</td></tr><tr><td>0</td><td>1</td><td>2 Sector</td></tr><tr><td>1</td><td>0</td><td>3 Sector</td></tr><tr><td>1</td><td>1</td><td>4 Sector</td></tr></table></td><td>0</td></tr>
<tr><td>0</td><td>IGSEL0</td><td>0</td></tr>
</table>

11	DVDCONTROL1 : DVD Decoder Control Register 1 (Sync)			
bit	**Name**	**Description**		**def.**
7	DSCREN		DE-SCRAMBLE ON/OFF	1
		1	On	
		0	Off	
6	STRST		TR MODE Forced Cancellation	0
		1	Cancel	
		0	Normal	
5	-			x
4	-			x
3	INSEN		Insert Enable	1
		1	Frame, Executes the ID Sync insertion.	
		0	Does not execute the Sync insertion	
2	WNDEN		Window Enable (Frame)	1
		1	Enables the Sync Protection Window . The syncs detected outside the window is treated as an illegal sync and are not used in the insertion timing reset. The protection window resets and opens when an illegal sync is detected consecutively N times.	
		0	Opens the window and validates all the detected syncs.	
1	WNDRT		Window Reset. Used to quickly lock the window when a new sync is detected during a track jump etc.	0
		1	Opens the window	
		0	NORMAL	
0	FCLDS		Frame Counter Value Load condition	1
		1	Load the frame counter value continuously detected while continuity was being maintained	
		0	During continuance, it loads only the detected frame counter value in the initialized interval (Frwin interval) and loads the insertion frame counter outside of this interval.	

<table>
<tr><th>12</th><th colspan="3">DVDCONTROL2 : DVD Decoder Control Register 2</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>7</td><td>WRST</td><td></td><td>Permit setting to write EFM demodulated data to the buffer</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>Permit</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Not permit</td><td></td></tr>
<tr><td>6</td><td>TRST</td><td></td><td>Permit setting to transfer data from the buffer to either the A/V decoder or host</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>Permit</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Not Permit</td><td></td></tr>
<tr><td>5</td><td>ECCST</td><td></td><td>Permit setting to start Error correction</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>Permit</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Not Permit</td><td></td></tr>
<tr><td>4</td><td>ECNEGLT</td><td></td><td>Ignore error correction.
(If an error exists in the ECC completed block, use when the MICOM determines that ECC restart is unnecessary)</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>Ignore Error correction (skip the block that is being corrected and move to the next block)</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Try Multiple Error Correction.
(Until ECC Stop¡¸ ECCST='0'¡¹or ECNEGLT='1')</td><td></td></tr>
<tr><td>3</td><td>ECMOD2</td><td colspan="2" rowspan="3">Error Correction Method Selection.
* In the retry CD mode (ECMOD[2:0]='100'), if the error exists even after the correction, ECC is automatically retried when there is sufficient buffer space until the input of the ECNEGLT signal. (The Micom determines whether there is enough Buffer space.)
<table><tr><th>ECMOD2</th><th>ECMOD1</th><th>ECMOD0</th><th>Disc speed</th></tr><tr><td>0</td><td>0</td><td>0</td><td>No Error Correction</td></tr><tr><td>0</td><td>0</td><td>1</td><td>PI+PO</td></tr><tr><td>0</td><td>1</td><td>0</td><td>PI+PO+PI(Normal)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>PI+PO+PI+PO</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Retry correction (CD) mode</td></tr><tr><td colspan="3">Other</td><td>Reserved</td></tr></table></td><td>0</td></tr>
<tr><td>2</td><td>EDMOD1</td><td>1</td></tr>
<tr><td>1</td><td>EDMOD0</td><td>0</td></tr>
<tr><td>0</td><td>MCPST</td><td></td><td>MICOM Block Copy Start Command</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>The MICOM moves the 1 sector data of a specified register to a register specified automatically by the decoder. After completion, the MICOM outputs MCPEND and resets the MCPST to '0'.</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Normal</td><td></td></tr>
</table>

<table>
<tr><th>13</th><th colspan="3">CLVCONTROL1 : CLV Control Register 1</th></tr>
<tr><th>bit</th><th>Name</th><th>Description</th><th>def.</th></tr>
<tr><td>7</td><td>PGAIN1</td><td rowspan="2">MDP GAIN setting of the DVD/CD CLV
<table><tr><th>PGAIN1</th><th>PGAIN0</th><th>MDP GAIN</th></tr><tr><td>0</td><td>0</td><td>-6dB</td></tr><tr><td>0</td><td>1</td><td>-12dB</td></tr><tr><td>1</td><td>0</td><td>-18dB</td></tr><tr><td>1</td><td>1</td><td>0dB</td></tr></table></td><td>0</td></tr>
<tr><td>6</td><td>PGAIN0</td><td>0</td></tr>
<tr><td>5</td><td>SGAIN1</td><td rowspan="2">MDS GAIN setting of the DVD/CD CLV.
<table><tr><th>SGAIN1</th><th>SGAIN0</th><th>MDS GAIN</th></tr><tr><td>0</td><td>0</td><td>-6dB</td></tr><tr><td>0</td><td>1</td><td>-12dB</td></tr><tr><td>1</td><td>0</td><td>-18dB</td></tr><tr><td>1</td><td>1</td><td>0dB</td></tr></table></td><td>0</td></tr>
<tr><td>4</td><td>SGAIN0</td><td>0</td></tr>
<tr><td>3</td><td>-</td><td></td><td>x</td></tr>
<tr><td>2</td><td>-</td><td></td><td>x</td></tr>
<tr><td>1</td><td>-</td><td></td><td>x</td></tr>
<tr><td>0</td><td>-</td><td></td><td>x</td></tr>
</table>

<table>
<tr><td>14</td><td colspan="3">CLVCONTROL2 : CLV Control Register 2</td></tr>
<tr><td>bit</td><td>Name</td><td colspan="2">Description</td><td>def.</td></tr>
<tr><td>7</td><td>MDSCON1</td><td colspan="2">MDS sector operation range specification of the DVD/CD CLV
<table><tr><td rowspan="2">MDSCON1</td><td rowspan="2">MDSCON0</td><td colspan="2">sector range</td></tr><tr><td>DVDROM</td><td>CDROM</td></tr><tr><td>0</td><td>0</td><td>± 9%</td><td>± 4.5%</td></tr><tr><td>0</td><td>1</td><td>± 18%</td><td>± 9%</td></tr><tr><td>1</td><td>0</td><td>± 36%</td><td>± 18%</td></tr><tr><td>1</td><td>1</td><td>RESERVE</td><td>± 33%</td></tr></table></td><td>0</td></tr>
<tr><td>6</td><td>MDSCON0</td><td colspan="2"></td><td>0</td></tr>
<tr><td>5</td><td>PLLC1</td><td colspan="2">Setting of the threshold value to cancel the DVD/CD PLL LOCK signal
<table><tr><td>PLLC1</td><td>PLLC0</td><td>THRESHOLD</td></tr><tr><td>0</td><td>0</td><td>PLL lock falling after WFCK16</td></tr><tr><td>0</td><td>1</td><td>PLL lock falling after WFCK 32</td></tr><tr><td>1</td><td>0</td><td>PLL lock falling after WFCK 64</td></tr><tr><td>1</td><td>1</td><td>PLL lock falling after WFCK 128</td></tr></table></td><td>0</td></tr>
<tr><td>4</td><td>PLLC0</td><td colspan="2"></td><td>0</td></tr>
<tr><td>3</td><td>-</td><td></td><td></td><td>x</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">MDPC</td><td></td><td>MDP output outside the MDS sector range</td><td rowspan="3">0</td></tr>
<tr><td>1</td><td>Hi-Z output outside the MDS sector range</td></tr>
<tr><td>0</td><td>Error signal output outside the MDS range</td></tr>
<tr><td>1</td><td>PRES1</td><td colspan="2">MDP WFCK/RFCK reference signal setting in the CLVP mode at DVD/CD CLV
<table><tr><td>PRES1</td><td>PRES0</td><td>WFCK reference</td><td>RFCK reference</td></tr><tr><td>0</td><td>0</td><td>WFCK/2</td><td>RFCK/2</td></tr><tr><td>0</td><td>1</td><td>WFCK/4</td><td>RFCK/4</td></tr><tr><td>1</td><td>0</td><td>WFCK/8</td><td>RFCK/8</td></tr><tr><td>1</td><td>1</td><td>WFCK/16</td><td>RFCK/16</td></tr></table></td><td>0</td></tr>
<tr><td>0</td><td>PRES0</td><td colspan="2"></td><td>0</td></tr>
</table>

<table>
<tr><th>15</th><th colspan="3">CLVCONTROL3 : CLV Control Register 3</th><th></th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>7</td><td>FALTHR1</td><td colspan="2">DVD/CD's CLV lock signal falling time select.

<table><tr><th>FALTHR1</th><th>FALTHR0</th><th>THRESHOLD</th></tr><tr><td>0</td><td>0</td><td>CLV lock falling after WFCK/RFCK 32</td></tr><tr><td>0</td><td>1</td><td>CLV lock falling after WFCK/RFCK 64</td></tr><tr><td>1</td><td>0</td><td>CLV lock falling after WFCK/RFCK 128</td></tr><tr><td>1</td><td>1</td><td>CLV lock falling after WFCK/RFCK 256</td></tr></table></td><td>0</td></tr>
<tr><td>6</td><td>FALTHR0</td><td colspan="2"></td><td>0</td></tr>
<tr><td>5</td><td>RISTHR1</td><td colspan="2">DVD/CD's CLV lock signal rising time setting

<table><tr><th>RISTHR1</th><th>RISTHR0</th><th>THRESHOLD</th></tr><tr><td>0</td><td>0</td><td>CLV lock rising after WFCK/RFCK 1</td></tr><tr><td>0</td><td>1</td><td>CLV lock rising after WFCK/RFCK 2</td></tr><tr><td>1</td><td>0</td><td>CLV lock rising after WFCK/RFCK 4</td></tr><tr><td>1</td><td>1</td><td>CLV lock rising after WFCK/RFCK 8</td></tr></table></td><td>0</td></tr>
<tr><td>4</td><td>RISTHR0</td><td colspan="2"></td><td>0</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">REFSEL</td><td></td><td>GFS reference signal select for generating the DVD/CD CLV lock signal</td><td rowspan="3">0</td></tr>
<tr><td>1</td><td>RFCK</td></tr>
<tr><td>0</td><td>WFCK</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">SERVOC</td><td></td><td>DVD/CD servo lock signal falling time setting.
¡Ø Rising is executed when GFS is detected consecutively 2 times based on RFCK.</td><td rowspan="3">0</td></tr>
<tr><td>1</td><td>Servo lock falling after RFCK 128</td></tr>
<tr><td>0</td><td>Servo lock falling after RFCK 64</td></tr>
<tr><td>1</td><td>CLVC1</td><td colspan="2">MOD setting for DVD/CD CLV lock On/Off.
¡Ø WIDE MODE CLV lock signal : GFS
NARROW MODE CLV lock signal : GFS * narrow

The narrow signal indicates that the PLL is operating within the sector range, selected by 14:MDSCON(1:0); narrow means GFS = High and no saturation.

<table><tr><th>CLVC1</th><th>CLVC0</th><th>CLVLOCK ON
(Active High)</th><th>CLVLOCK OFF
(Active Low)</th></tr><tr><td>0</td><td>0</td><td>WIDE</td><td>WIDE</td></tr><tr><td>0</td><td>1</td><td>WIDE</td><td>NARROW</td></tr><tr><td>1</td><td>0</td><td>NARROW</td><td>WIDE</td></tr><tr><td>1</td><td>1</td><td>NARROW</td><td>NARROW</td></tr></table></td><td>0</td></tr>
<tr><td>0</td><td>CLVC0</td><td colspan="2"></td><td>0</td></tr>
</table>

16	CLVMODE : CLV Mode Register		
bit	**Name**	**Description**	**def.**
7	SDWP	Small interval sample signal	1
		1 Sample every RFCK/2	
		0 Sample every RFCK/4	
6	SDWB	Large interval sample signal	1
		1 Sample every RFCK/16	
		0 Sample every RFCK/32	
5	-		x
4	-		x
3	SDCM3	CLV MODE setting (In STOP Mode, the MDP must output as Hi-Z.)	0
2	SDCM2		0
1	SDCM1		0
0	SDCM0		0

SDCM 3	SDCM 2	SDCM 1	SDCM 0	CLV MODE	MDP Block	MDS Block
0	0	0	0	STOP	Hi-Z	Hi-Z
1	0	0	0	KICK	H	Hi-Z
1	0	1	0	BRAK	L	Hi-Z
1	1	1	0	CLVS	L,Z,H	Hi-Z
1	1	0	0	CLVH	L,Z,H	Hi-Z
1	1	1	1	CLVP	L,Z,H	L,H
0	1	1	0	CLVA	L,Z,H	L,Z,H
1	0	0	1	CAV	Hi-Z	L,Z,H
other				RESERVE		

17	CDPTEST		
bit	**Name**	**Description**	**def.**
7	CTMOD4	CD test mode bit4. Set it to '0' during normal play.	
6	CTMOD3	CD test mode bit3. Set it to '0' during normal play.	
5	CTMOD2	CD test mode bit2. Set it to '0' during normal play.	
4	CTMOD1	CD test mode bit1. Set it to '0' during normal play.	
3	CTMOD0	CD test mode bit0. Set it to '0' during normal play.	
2	nsync	New Frame sync detection method in CD mode. Assume frame sync if the period between the rising edges or falling edges of the EFM input signal is 22 clock of PLCK.	
		1 New Frame sync detection method in CD mode.	
		0 Does not use the new frame sync dectection method in the CD mode.	
1	flg_con	ECC flag control during the defect period in VCD mode.	
		1 ECC flag is set by force during defect period.	
		0 Use existing algorithm.	
0	cpeak	Precision ECC flag control during the defect period in the VCD mode	
		1 Executes precision control	
		0 Does not execute precision control	

18	CDDEFECT		
bit	**Name**	**Description**	**def.**
7	fsc_con3	Sets the length of the defect signal during ECC flag signal control in the defect period in VCD mode. 0000 : 11ms 0001 : 22ms : 1111 : 176ms	0
6	fsc_con2		0
5	fsc_con1		0
4	fsc_con0		0
3	dc_con1	Length of possible defect detection dc_con1 / dc_con0 / 0 / 0 / 0.45ms 0 / 1 / 0.55ms 1 / 0 / 0.65ms 1 / 1 / 0.75ms	0
2	dc_con0		0
1	cps1	CPEAK detection cycle select to set the C1 flag setting condition cps1 / cps0 0 / 0 / 24T 0 / 1 / 32T 1 / 0 / 40T 1 / 1 / 48T	0
0	cps0		0

19	TRMODE : Data Transfer Mode Register			
bit	**Name**		**Description**	**def.**
7	IFMOD2	I/F transmission method assignment for the A/V decoder or ROM decoder IFMOD2 / IFMOD1 / IFMOD0 / I/F Transmission Method 0 / 0 / 0 / C(A/V DECODER: Synchronous) - / - / - / Reserved		0
6	IFMOD1			0
5	IFMOD0			0
4	-			x
3	CDIF0		CD interface format assignment	0
		1	format2	
		0	format1	
2	DRATE		Transmission speed assignment for the A/V decoder or ROM decoder Set to byte/240nS in the DVD-ROM mode	1
		1	byte/240nS	
		0	byte/480nS	
1	-			x
0	DVDIF0		DVD interface format assignment	1
		1	mode2 (2064 BYTES SECTOR)	
		0	mode1 (2048 BYTES MAIN)	

1A	CDSPEED : CD Speed Control Register			
bit	**Name**	**Description**		**def.**
7	-			x
6	-			x
5	-			x
4	-			x
3	-			x
2	CDSPD2	CD speed control Register		0
1	CDSPD1			0
0	CDSPD0			0

CDSPD2	CDSPD1	CDSPD0	Disc speed
0	0	0	1X
0	0	1	2X
Other			Reserved

1B	CDMUTCNT : CD Mute Control Register			
bit	**Name**	**Description**		**def.**
7	CBITIN2	DIGITAL AUDIO OUTPUT CONTROL MODE Setting		0
6	CBITIN1			0
5	CBITIN0			0
4	DGOEN		Determines DIGITAL AUDIO OUTPUT Mode	0
		1	Output	
		0	Hi-Z	
3	DEMPHA		CD AUDIO DEEMPHASIS CONTROL	0
		1	On	
		0	Off	
2	MUTE		CD-DA Data Mute	1
		1	On	
		0	Off	
1	ZCMT		Zero Cross Mute Control bit	0
		1	Off	
		0	On	
0	ATTN		Attenuation On/Off	0
		1	On	
		0	Off	

CBITIN2	CBITIN1	CBITIN0	Setting
x	x	0	For common use (MODE II)
x	0	x	AUDIO
0	x	x	DIGITAL COPY not permitted
1	x	x	DIGITAL COPY permitted

ATTN	MUTE	dB
0	0	0
0	1	-∞
1	0	-12
1	1	-12

1C	CDCONTROL : CD Control Register		
bit	**Name**	**Description**	**def.**
7	PLCKINV	PLCK clock phase control	0
	1	Converts the PLCK clock phase	
	0	Does not convert the PLCK clock phase	
6	PLCKCON	PLCK pin I/O control	0
	1	Uses as the input mode	
	0	Uses as the output mode	
5	EFMCON	EFMTRD pin I/O control	0
	1	Uses as input mode	
	0	Uses as output mode	
4	PCDCON	Pin PCD7 - PCD0 I/O control	0
	1	Uses as Input mode	
	0	Uses as Output mode	
3	BYPASS	BYPASS MODE Setting	1
	1	L-Ch/ R-Ch Data Serial Output	
	0	Error Value correction circuit applied	
2	INFR	Determines whether to release the frame window just after the number of insertion frames set by the FGSEL(1:0)($10) or to release it after few more frame syncs detected by FWID.	1
	1	Does not immediately release the frame window but locks the frame window after the first detected frame sync resets the insertion counter and the detected frame sync appears continuously in regular cycles.	
	0	Immediately releases the frame window and locks it after the first detected frame sync resets the insertion counter.	
1	-		
0	T3_MODE	1 T3 correction mode Enable	0
		0 T3 correction mode Disable	

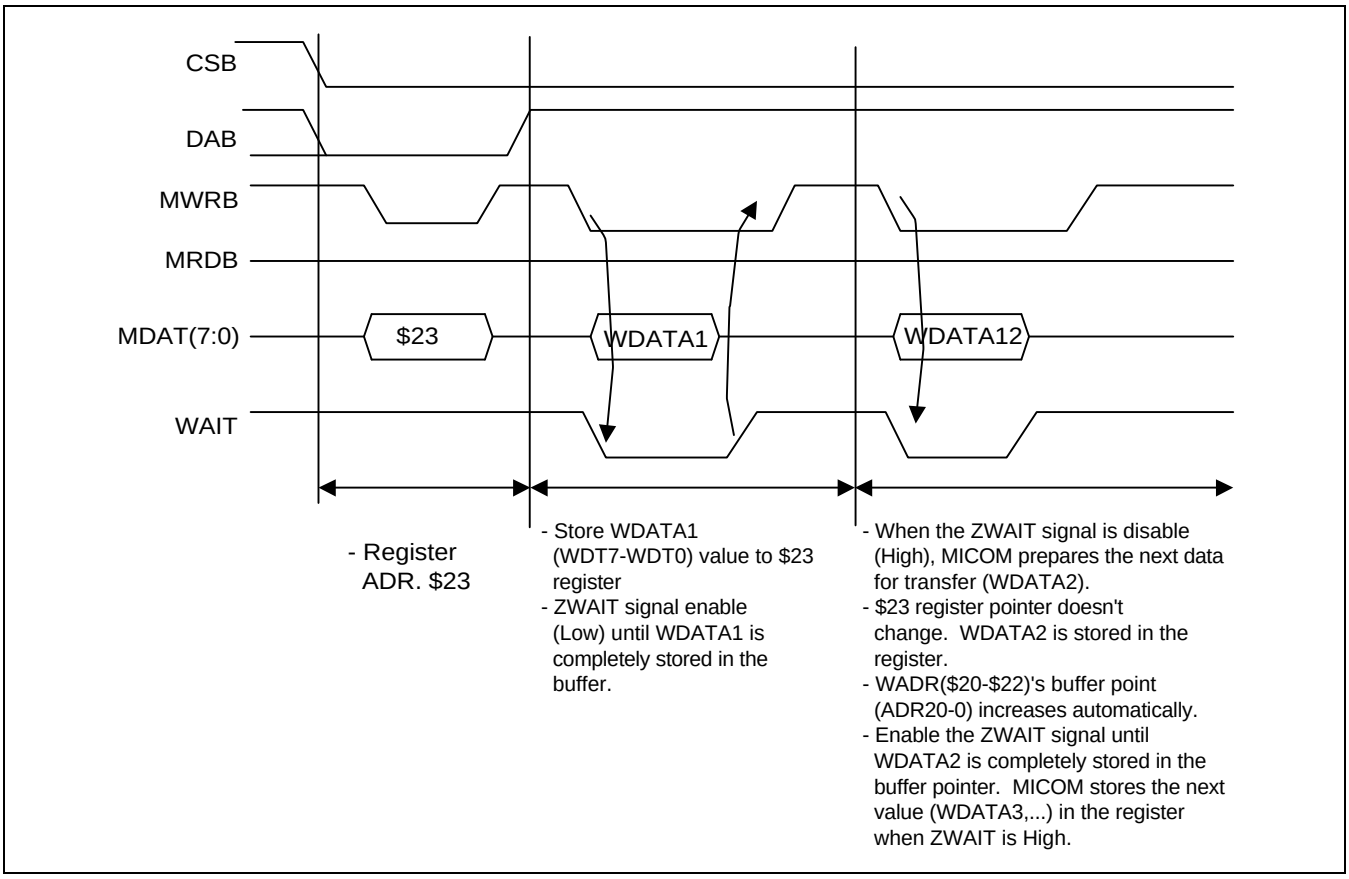
1D	CDCONTROL : CD Control Register			
bit	**Name**	**Description**		**def.**
7	ERAMODF		Erasure correction mode or error correction mode select for max erasure in DVD mode or CD-First-C2 Mode	1
		1	Erasure correction mode	
		0	Error correction mode	
6	ERAMODL		Erasure correction mode or error correction mode select for max erasure in CD-Last-C2 Mode(No DVD Mode)	1
		1	Erasure correction mode	
		0	Error correction mode	
5	maxmod c2f		Error correction status for max erasure in DVD mode and CD-First-C2 Mode	0
		1	No error correction	
		0	Error correction	
4	maxmod c2l		Erasure correction mode or error correction mode select for max erasure in CD-Last-C2 Mode(No DVD Mode)	0
		1	No error correction	
		0	Error correction	
3	c2ecc f		Error correction status for an overflow in CD-First-C2 Mode (No DVD Mode)	1
		1	No error correction	
		0	Error correction	
2	c2ecc l		Error correction status for an overflow in CD-Last-C2 Mode (No DVD Mode)	1
		1	No error correction	
		0	Error correction	
1	c2err onlyf		Error Correction Method in CD-First-C2 Mode	0
		1	Executes only error correction(ignore Flag)	
		0	Error correction(Erasure or error)	
0	c2err onlyl		Error Correction Method in CD-Last-C2 Mode	0
		1	Executes only error correction(ignore Flag)	
		0	Error correction (Erasure or error)	

1E	CDCONTROL : CD Control Register		
bit	**Name**	**Description**	**def.**
7	-		x
6	cdecc	Multiple correction status in CD Mode	1
		1 Multiple correction	
		0 Correction only once	
5	eccmode	First /Last period error correction status in CD multiple correction mode(cdecc = 1)	0
		1 No error correction in the first period and error correction only in the last period	
		0 Error correction for both First/Last periods	
CD Mode Flag Setting Condition			
4	c2fgtype [4]	When maxmodc2f/maxmodc2l='1' in the CD-C2 Mode	1
		1 C1 Flag Copy [11]	
		0 C2 Flag Out [01]	
3	c2fgtype [3]	When Overflow occurs in CD-C2 mode	1
		1 C1 Flag Copy [11]	
		0 C2 Flag Out [01]	
2	c2fgtype [2]	CD multiple correction mode. Max Correction(Error, Erasure) in the CD-Last -C2 mode	1
		1 C1 Flag Copy [11]	
		0 C2 Flag Out [01]	
1	c2fgtype [1]	CD 1st correction mode. Max Correction (Error, Erasure) in CD-C2 mode	1
		1 C1 Flag Copy [11]	
		0 C2 Flag Out [01]	
0	c2fgtype [0]	Un-Correctable Code in CD-C2 mode	1
		1 C1 Flag Copy [11]	
		0 C2 Flag Out [01]	

1F	CDCONTROL : CD Control Register		
bit	**Name**	**Description**	**def.**
7	jithold		0
		1 Interpolation Hold for duration of error period for memory jitter	
		0 Output without interpolation hold for Memory Jitter	
6	jumphold		0
		1 Interpolation Hold for the duration of discontinuous C2 correction period for a jump	
		0 Output without interpolation hold for a jump	
5	-		x
4	-		x
3	SETFLG[3]		1
		1 PI Flag in DVD Mode Flag Setting ← Must be 'Default' only when uncorrectable (Error or Erasure) C1-First Flag in CD Mode Flag Setting only when uncorrectable (exceeds 2 errors)	
		0 C1-First Flag in CD Mode. Flag Setting even for 2 error corrections	
2	SETFLG[2]		1
		1 PO Flag in DVD Mode Flag Setting ← Must be 'Default' only when uncorrectable (Error or Erasure) C2-First Flag in CD Mode Flag Setting only when uncorrectable (exceeds 2 errors)	
		0 -	
1	SETFLG[1]	CD Mode C1-Last Flag (No DVD Mode)	1
		1 Flag Setting only when uncorrectable (exceeds 2 errors)	
		0 Flag Setting even for 2 error corrections	
0	SETFLG[0]	C1-Last Flag in CD mode (No DVD Mode)	1
		1 Flag Setting ← Must be 'Default' when uncorrectable (exceeds 2 errors)	
		0 -	

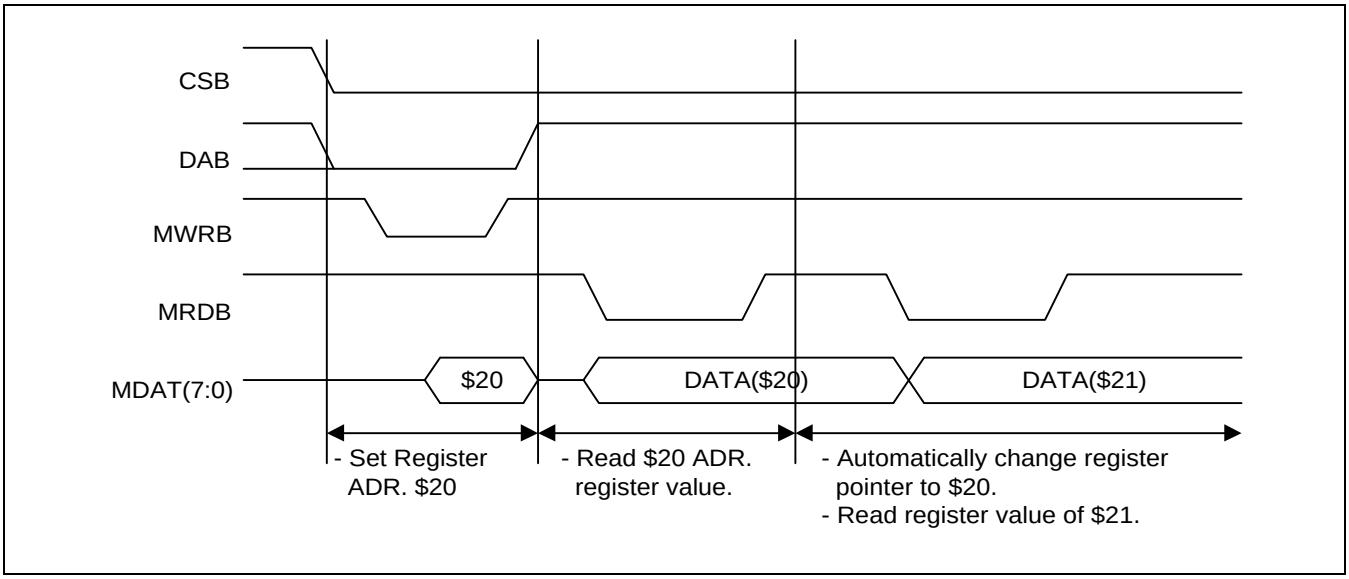
WADRH/M/L : Address Setting on Micom Direct Access Buffer Mode (¡Ø Read/Write)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
20	-	-	-	ADR20	ADR19	ADR18	ADR17	ADR16
21	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
22	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
WDATA : Data Write to Buffer(when MDAB = 1)								
23	WDT7	WDT6	WDT5	WDT4	WDT3	WDT2	WDT1	WDT0
Reset value	20 - 23 register : all-zero							

¾ Buffer Writing



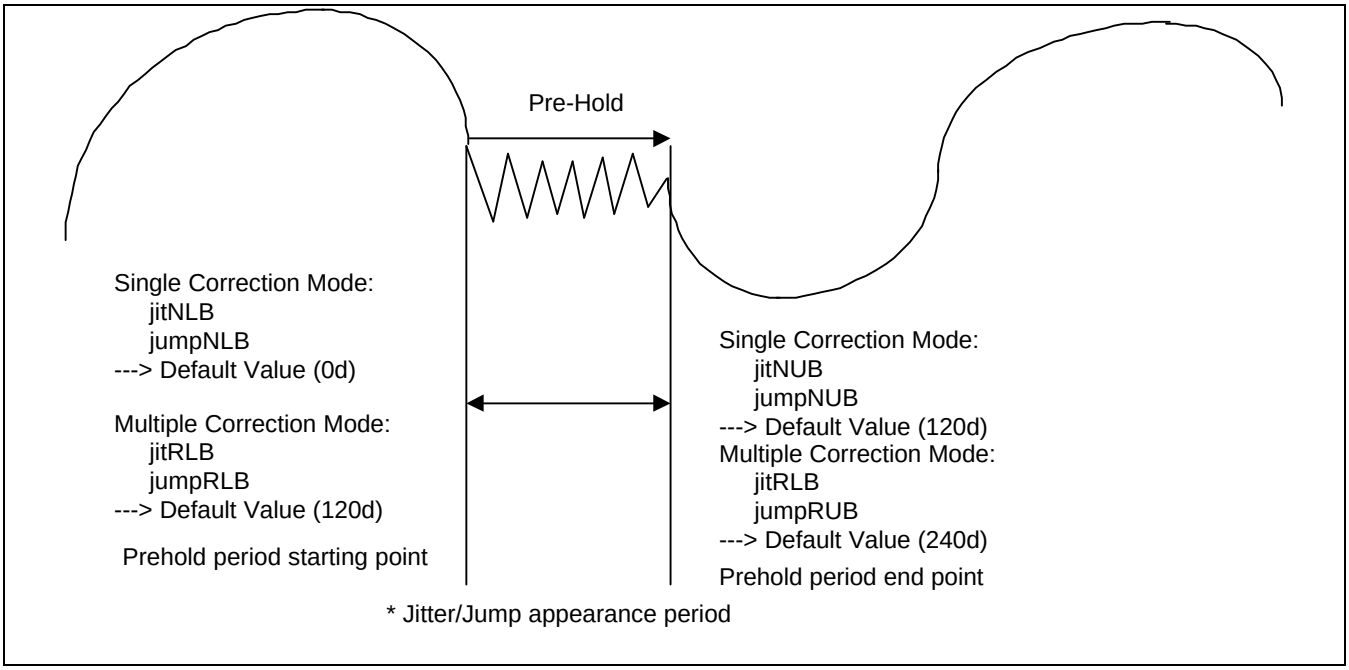
¾ Last Written Address Reading

Reads the buffer pointer (+1) written last to the buffer.



JITNLB, JITNUB, JITRLB, JITRUB								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
24	jitnl7	jitnl6	jitnl5	jitnl4	jitnl3	jitnl2	jitnl1	jitnl0
25	jitnu7	jitnu6	jitnu5	jitnu4	jitnu3	jitnu2	jitnu1	jitnu0
26	jitrl7	jitrl6	jitrl5	jitrl4	jitrl3	jitrl2	jitrl1	jitrl0
27	jitru7	jitru6	jitru5	jitru4	jitru3	jitru2	jitru1	jitru0
Reset Value								
illustration								

JUMPNLB[1:0], JUMPNUB[1:0], JUMPRLB[1:0], JUMPRUB[1:0]								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
28	jumpnl15	jumpnl14	jumpnl13	jumpnl12	jumpnl11	jumpnl10	jumpnl9	jumpnl8
29	jumpnl7	jumpnl6	jumpnl5	jumpnl4	jumpnl3	jumpnl2	jumpnl1	jumpnl0
2A	jumpnu15	jumpnu14	jumpnu13	jumpnu12	jumpnu11	jumpnu10	jumpnu9	jumpnu8
2B	jumpnu7	jumpnu6	jumpnu5	jumpnu4	jumpnu3	jumpnu2	jumpnu1	jumpnu0
2C	jumprl15	jumprl14	jumprl13	jumprl12	jumprl11	jumprl10	jumprl9	jumprl8
2D	jumprl7	jumprl6	jumprl5	jumprl4	jumprl3	jumprl2	jumprl1	jumprl0
2E	jumpru15	jumpru14	jumpru13	jumpru12	jumpru11	jumpru10	jumpru9	jumpru8
2F	jumpru7	jumpru6	jumpru5	jumpru4	jumpru3	jumpru2	jumpru1	jumpru0
Reset Value								
illustration								



WBAH, WBAL : Buffering Start Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
30	B9 - B8							
31	B7 - B0							
Reset Value	3FF							
illustration	Start sector unit number used to save the EFM data in the buffer. W sector unit is assigned.							

WEAH, WEAL : ECC Start Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
32	B9 - B8							
33	B7 - B0							
Reset Value	3FF							
illustration	Error correction sector unit number assignment. (Make B3 - B0 = '0' and assign in unit of block) X Sector Unit is assigned.							

WTAH, WTAL : Transfer Start Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
34	B9 - B8							
35	B7 - B0							
Reset Value	1FF							
illustration	Data transfer start sector unit number assignment. Z sector unit is assigned. ** The unit number above is automatically incremented in units of sectors when all applicable start signal are enabled and completed. ** Unit Number definition B9-8 : Bank 0-3, B7-4 : Block 0-12, B3-0 : Sector 0-15							

OTSH, OTSL : Over Threshold Size (Sector Unit Number) (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
36	B9 - B8							
37	B7 - B0							
Reset Value	all high							
illustration	Buffer memory over threshold size assignment (maximum of 16 blocks). That is, it assigns the maximum allowable absolute value of (Unit Number W - Unit Number Z). The Z-decoder outputs an over interrupt when the number of blocks in the memory exceeds this set value.							

UTSH, UTSL : Under Threshold Size (Sector Unit Number) (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
38	B9 - B8							
39	B7 - B0							
Reset Value	all zero							
illustration	Buffer memory under threshold size assignment (maximum of 16 blocks). That is, it assigns the maximum allowable absolute value of(Unit Number W - Unit Number Z). The Z-decoder outputs an under interrupt when the number of blocks in the memory exceeds this set value.							

TNH, TNL : Transmission Sector Numbers (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
3A	B15 - B8							
3B	B7 - B0							
Reset Value	all high							
illustration	Number of bits of the data to be transmitted to either the A/V decoder or ROM decoder; the maximum transmission sector number is 64K sectors. After the transmission sector number is sent, the Z-decoder outputs a transmission complete interrupt.							

MBS : Micom buffer size (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
3C	-	-	-	-	B3	B2	B1	B0
Reset Value	-	-	-	-	0	0	0	1
illustration	The Micom buffer size assignment. The size is in unit of ECC block (16KBytes). Maximum of 8 blocks / bank is possible. (LSB 4 bits : For DVD, '0001'[Block 1]-'1000'[Block 8] For CD, '0001'[Block 1]-'0111'[Block 7]) The initial value is set to block 1. - Bank : Exists in unit of 4 Mbits. For 16M bits requires 4 banks, and therefore a Micom buffer of maximum of 32 blocks can be formed.							

BCPSH, BCPSL : Decoder Direct Block copy source sector address (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
3D	B9 - B8							
3E	B7 - B0							
Reset Value	all zero							
illustration	Transfer data source sector address is used in the mode that automatically moves the address in sectors to the data buffer to be used by the Micom.							

BCPTH, BCPTL : Decoder Direct Block copy target sector address ÁöÁ¤ (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
40	B9 - B8							
41	B7 - B0							
Reset Value	all zero							
illustration	Transfer data target sector address is used in the mode that automatically moves the address in sectors to the data buffer to be used by the Micom.							

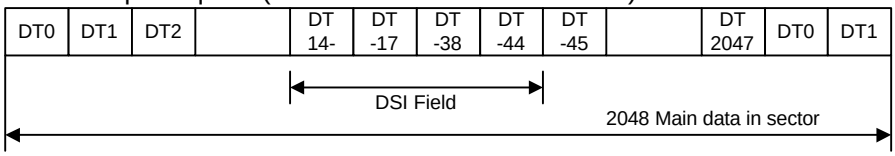
WDAH, WDAL : Descramble Start Sector Unit Number (¡Ø R/W)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
42	B9 - B8							
43	B7 - B0							
Reset Value	1FF							
illustration	Descramble Start Sector Unit Number Assignment. ** The unit number above is automatically incremented in units of sectors when all applicable start signal are enabled and completed. ** Unit Number definition B9 - 8 : Bank 0 - 3 B7 - 4 : Block 0 - 12 B3 - 0 : Sector 0 - 15							

44	**USERREG**			
bit	**Name**	**Description**		**def.**
7	-			x
6	-			x
5	TSTWRD		For ASIC TEST	0
4	ectest		For ECC Block Simulation (leave in Default state)	0
3	NMON3		Test command. Set to '0' during normal play.	x
2	NMON2		Test command. Set to '0' during normal play.	x
1	NMON1		Test command. Set to '0' during normal play.	x
0	NMON0		Test command. Set to '0' during normal play.	x

45	USRREG : ECC Operation Control / Memory Point Reset			
bit	**Name**	**Description**		**def.**
7	MONITOR3	For Internal Signal Monitoring in chip test mode		0
6	MONITOR2			0
5	MONITOR1			0
4	MONITOR0			0
3	MPRSTZ		BUNP,DUNP,EUNP,TUNP initial values REGISTER	1
		1	TUNP = " 1FF "	
		0	BUNP,DUNP,EUNP = " 3FF "	
2	TSTENDMUX	Used to forcibly stop the ECC mode during execution (PI read or PO read). Once the execution stops, the assigned ECC mode executes. In other words, in the PI+PO+PI MODE, when the first PI is forcibly stopped, the PO mode executes, and , if the PO mode is forcibly stopped during its execution, the next PI mode executes. If then the last PI is forcibly stopped during its execution, it skips to the first PI mode of the next ECC block. Stop sequence : (1) Set TSTENDMUX BIT to ¡°1¡±. (2) If PI, TSTPIREND If PO, set TSTPOREND BIT to ¡°1¡± ---> stop (3) Set TSTPIREND or TSTPOREND BIT to ¡°0". (4) Set TSTENDMUX BIT to ¡°0¡±. ¡Ø Can execute (3) and (4) together.		0
1	TSTPOREND			0
0	TSTPIREND			0

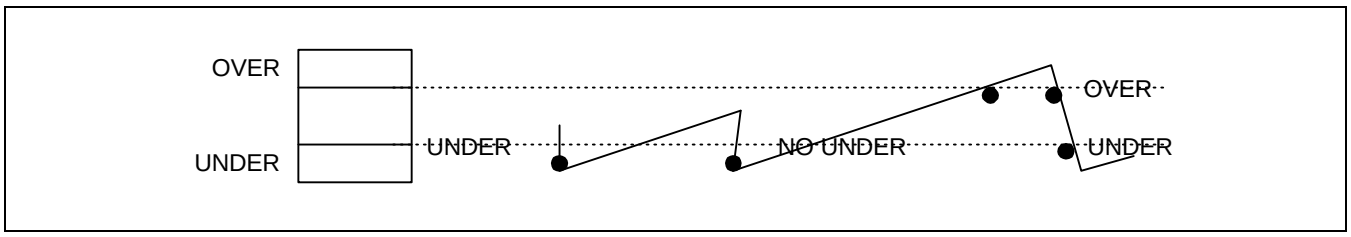
46	USRREG : DATA TRANSFER / TEST MODE REGISTER			
bit	**Name**	**Description**		**def.**
7	REQEG		Determines the transfer related signal's (DATREQ) active mode.	0
		1	Active High	
		0	Active Low	
6	ACKEG		Determines the transfer related signal's (DATACK) active mode.	0
		1	Active High	
		0	Active Low	
5	STREG		Determines the transfer related signal's (STROBE) active mode.	0
		1	Falling Edge	
		0	Rising Edge	
4	TOSEG		Determines the transfer related signal's (TOS) active mode.	0
		1	Active High	
		0	Active Low	
3	DTEREG		Determines the transfer related signal's (DTER) active mode.	0
		1	Active High	
		0	Active Low	
2	-			x
1	TSTID	For ASIC TEST		0
0	TSTIDSY			0

2) For DSP: Micom Read Register & Read/Write Register Table (R/W ; R)

4A	INTSTAT1 : Interrupt Status Register 1		
bit	**Name**	**Description**	**def.**
7	DVDSINT	DVD Sync Interrupt Request (When there is an abnormal play, such as a reset, search ,or jump etc., the first ID sync should not be used as an ID interrupt because it is a insertion ID sync.)	0
	1	Sets to '1' every time the DVD decoder sends the sync (ID sync).	
	0	This interrupt appears when CLRINT($0C) = 1 and is set to '0' when the micom reads according to the S4A4B[A8] REGISTER.	
6	DSINT	DSI Interrupt Request (DON'T CARE in the CD mode) 	0
	1	Among the 2048 Main Data in the DVD decoder * Starting from 15 Bytes, System Header Start_Code(00,00,01,BB) * Starting from 39 Bytes, Packet_Header (00,00,01,BF,**,**) Sub_Stream_id(00), the sector is determined to be a DSI pack and DSINT sets to '1' when the sector is treated as the DSI pack	
	0	Sets to '0' when the micom reads according to the S4A4B[A8] REGISTER when CLRINT($0C) = 1.	
5	TOSINT	Top of Sector Interrupt Request	0
	1	Indicates the start of the sector at data transfer	
	0	Sets to '0' when the micom reads according to the S4A4B[A8] REGISTER when CLRINT($0C) = 1.	
4	TRSCMPLT	Transfer Complete Interrupt Request when the number of specified bytes have been transferred.	0
	1	complete	
	0	in progress	
3	ECCMPLT	ECC Complete Interrupt Request	0
	1	Interrupt Request to indicate the completion of the error correction	
	0	Sets to '0' when the micom reads according to the S4A4B[A8] REGISTER when CLRINT($0C) = 1.	
2	EMPTY	Existence/No existence of data (sector) to be transferred to the memory	0
	1	Not existent	
	0	Existence	
1	OVER	Memory Overflow flag	0
	1	The Z-decoder sends an over interrupt when the number of blocks in the memory exceeds the set OTS (Over Threshold Size) value.	
	0	Sets to '0' when the micom reads according to the S4A4B[A8] REGISTER when CLRINT($0C)=1.	
0	UNDER	Memory Underflow Flag	0
	1	The Z-decoder sends an under interrupt when the number of blocks in the memory is less than the set OTS (Over Threshold Size) value.	
	0	Sets to '0' when the micom reads according to the S4A4B[A8] REGISTER when CLRINT($0C) = 1.	

— EMPTY, OVER, and UNDER are synchronized to the DVD Sync

— A new over interrupt occurs after an over interrupt and only in an over status after an under interrupt. In the same way, a new under interrupt only occurs in an under status after an existing under interrupt.



4B	INTSTAT2 : Interrupt Status Register 2			
bit	**Name**	**Description**		**def.**
7	SBQINT		Subcode Q Sync INTERRUPT	0
		1	Detects the subcode sync S0 and S1 and generates them as interrupts	
		0	default	
6	MCPINT		Micom Block Copy Complete INTERRUPT.	0
		1	complete	
		0	default	
5	-			x
4	-			x
3	-			x
2	-			x
1	-			x
0	-			x

4C	ERRSTAT : ERROR Status Register			
bit	**Name**	**Description**		**def.**
7	EIDERR		The DVDSINT (DVD ID SYNC INTERRUPT) state can indicate the error status of the data sector ID address data, to be EFM demodulated and input to the current buffer.	0
		1	Error(when there is an ID ECC Error)	
		0	No Error	
6	DSIERR		DVDSINT(DVD ID SYNC INTERRUPT) state can indicate the error status of the current generated 4A:DSINT.	0
		1	Possible error (when there is an EDC Error)	
		0	No Error	
5	IDCONERR		Possibility of continuous error in the EFM write sector ID address) (Checks the continuance of two adjacent ID numbers)	0
		1	continuous	
		0	discontinuous	
4	-			x
3	ECCERR		Error correction status of the current error-corrected data (1 ECC block) is indicated by the ECCMPLT(ECC Complete INTERRUPT) state.	0
		1	Error(ECC result of 1 Block)	
		0	No Error	
2	EDCFLG		Error correction status of the entire, current 2064 byte sector to be sent to the A/V decoder is indicated by the TOSINT (Top of Sector INTERRUPT) state.	0
		1	Error	
		0	No Error	
1	-			x
0	SBQERR		Error correction status of the current subcode data to be sent to the A/V decoder is indicated by the SBQINT (Subcode Q INTERRUPT) state.	0
		1	Error	
		0	No Error	

4D	DVDSTATUS : DVD Decoder Status Register			
bit	**Name**	**Description**		**def.**
7	-			x
6	-			x
5	-			x
4	-			x
3	SYOK		ID SYNC detection status at timing equal to the insertion timing	0
		1	detection	
		0	default	
2	NOSY		ID SYNC detection status in the window	0
		1	No detection	
		0	default	
1	ILSY		ID SYNC detection status outside the window	0
		1	detection	
		0	default	
0	-			x

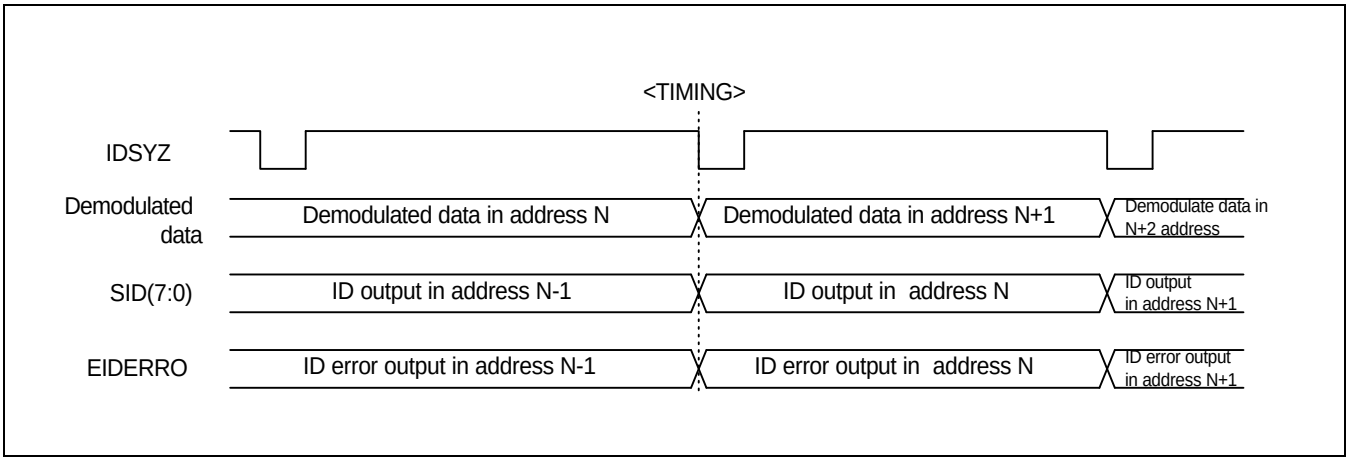
The Sync status of the interrupt, caused by the DVDSINT interrupt of INTSTAT1 Register ($4A), is indicated.

4E	DVDSVSTAT : DVD Decoder Servo Status Register			
bit	**Name**	**Description**		**def.**
7	-			x
6	LOCK		Locked spindle servo	0/x
		1	Lock	
		0	default	
5	GFS			0/x
		1	Play 16-8 frame sync (17.58kHz) is obtained with exact timing.	
		0	default	
4	-			x
3	-			x
2	-			x
1	-			x
0	-			x

* CDSUBQ : CD-DA Subcode Q Register								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
50	SBQ79 - SBQ72							
↓ ↓ ↓	↓ ↓ ↓							
59	SBQ07 - SBQ00							
Reset value	X	X	X	X	X	X	X	X
illustration	CD-DA Subcode Q data save. S0S1(Subcode Block Sync) This data continues to be valid in the low area.							

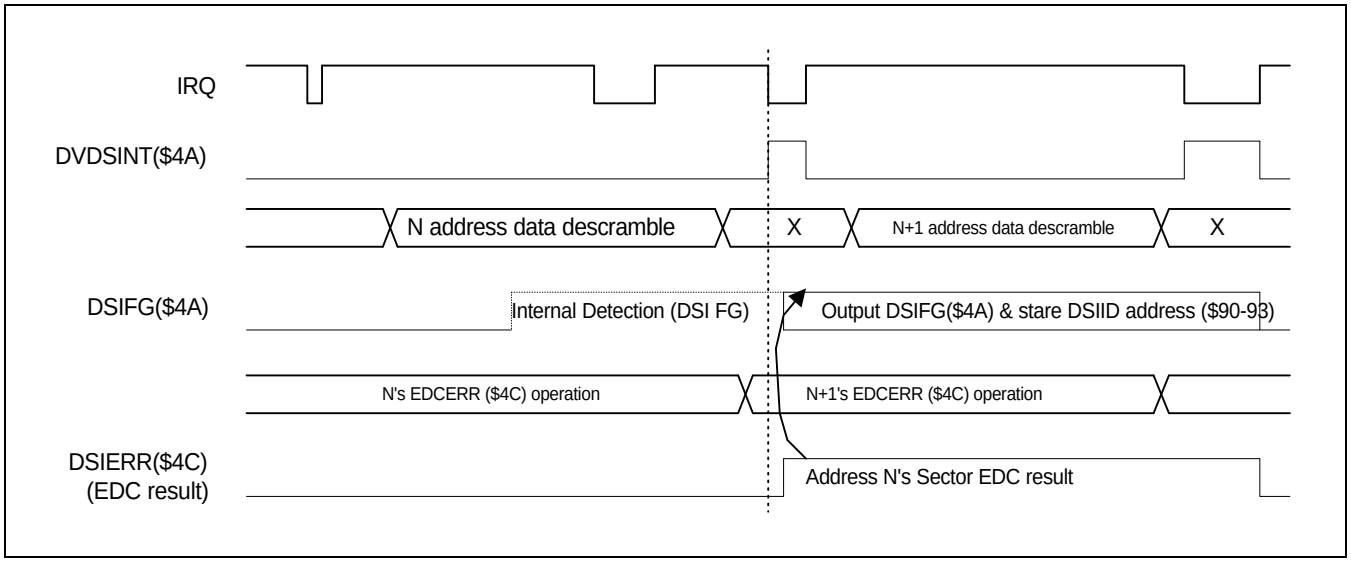
* SEEKIDADR : ID Data during EFM Demodulation								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
60	SID31 - SID24							
61	SID23 - SID16							
62	SID15 - SID08							
63	SID07 - SID00							
Reset value	X	X	X	X	X	X	X	X

This data, used for the current EFM demodulated data ID address, seamless buffering control and disc search, continues to be valid until the next DVDSINT interrupt.



* TRANSIDADR : ID Data during Data Transfers to A/V Decoder								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
64	TID31 - TID24							
65	TID23 - TID16							
66	TID15 - TID08							
67	TID07 - TID00							
Reset value	X	X	X	X	X	X	X	X

ID address of the data sent to either the A/V decoder or ROM decoder after decoding. This data is valid until the next TOSINT interrupt.

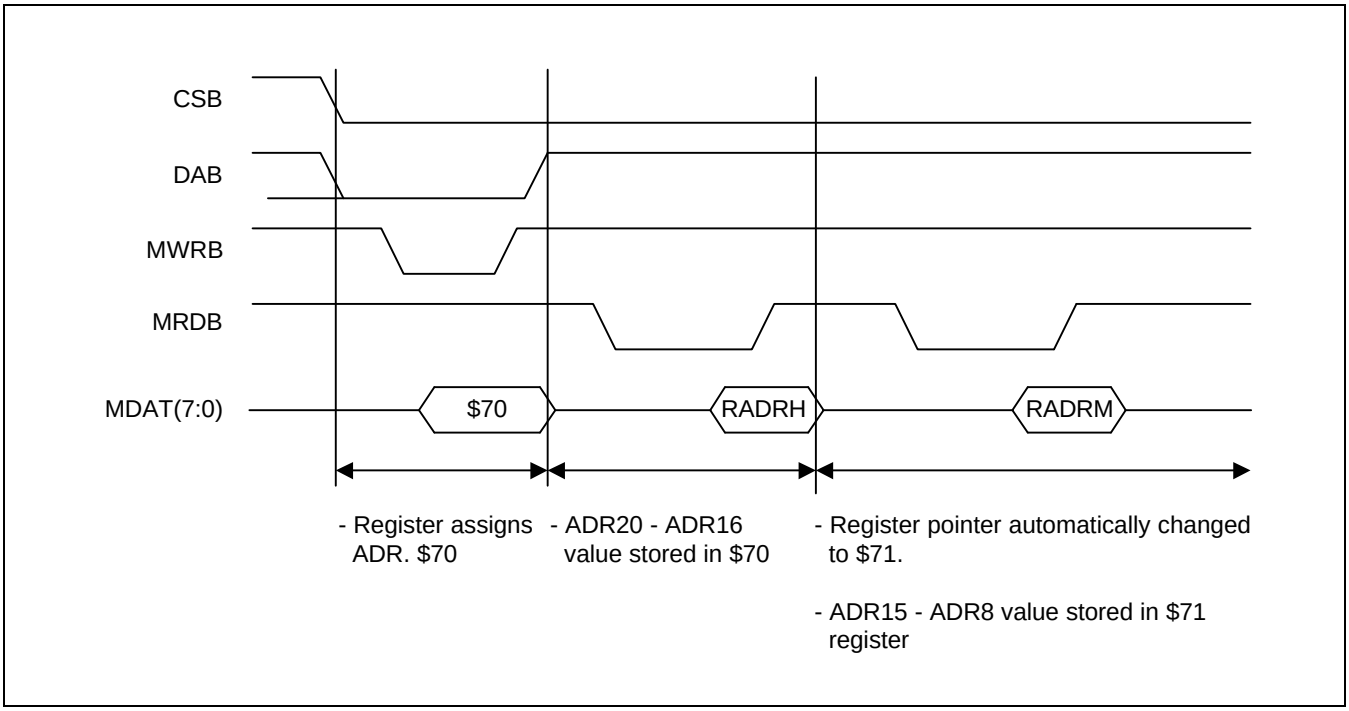


* RADR, RDATA: MDAB Register for Direct Access on DRAM (MDAB=1) (¡Ø Read/Write)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
70	-	-	-	ADR20	ADR19	ADR18	ADR17	ADR16
71	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
72	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
RDATA : Data Read from Buffer(when MDAB = 1)								
73	RDT7	RDT6	RDT5	RDT4	RDT3	RDT2	RDT1	RDT0
Reset value	70 - 73 register : all-zero							

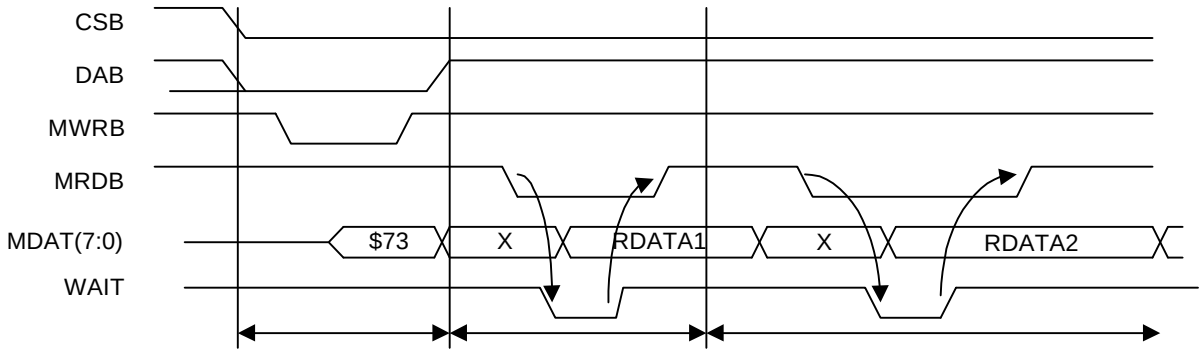
READ ACCESS

— Buffer Read Address Setting

— The MICOM must always set the register address number 70 because it does not automatically increment.



¾ Buffer Reading



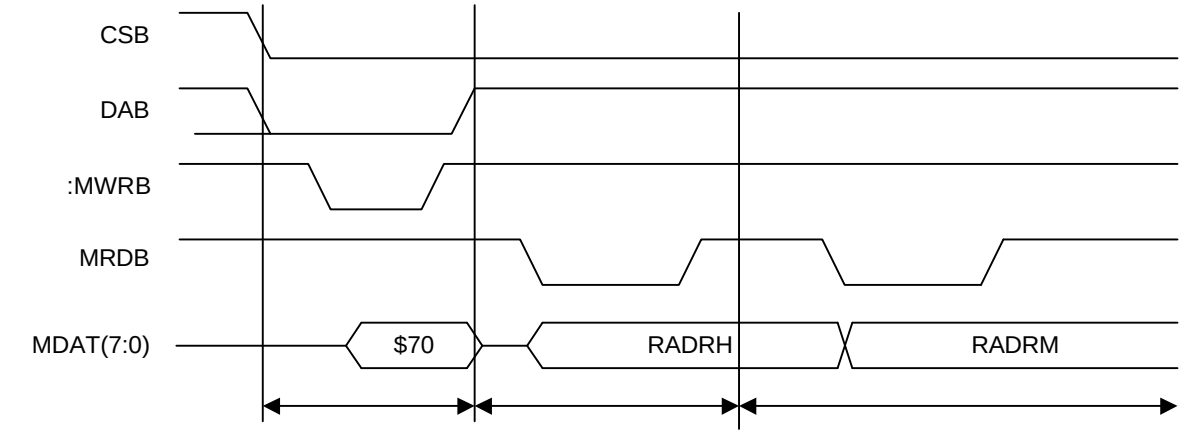
- Register assigns ADR $73

- Save RDATA1(RDT7-RDT0) value in ADR $73 as the data for the buffer assigned by the RADR ($70-72) buffer pointer.
- Wait signal enable (low) after verifying the MRDB fall and disable after RDATA1 has been saved in ADR $73.
- The MRDB rises after the micom reads the RDATA1 at disabled (high) wait signal.

- As the micom reads the RDATA1, the ADR $73 does not change. As the RDAT ($70-72) buffer pointer automatically increments, it moves the RDATA 2 into the ADR $73.
- Wait signal enable after verifying the MRDB fall and disable after RDATA2 has been saved in ADR $73.
- The MRDB rises after the micom reads RDATA2 at disable (high) wait signal.

¾ Last Read out Address Reading

Reads the buffer +1 value read last from the buffer



- Register assigns ADR. $70

- Reads the value in ADR $70

- Automatically change the register pointer to ADR $71.
- Reads the value in ADR $71.

* Buffering End Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
80	B9 - B8							
81	B7 - B0							
Reset value	B(9:0)=3FF							

Current EFM data written buffer sector unit number.
Valid until the next DVDSINT($4A) Interrupt. The saving of 1 sector at WRST($12) Low continues as is and it outputs the value of WRST($12)->'L' (completed sector no.) < valid after the first DVDSINT after WRST ($12)>

* ECC End Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
82	B9 - B8							
83	B7 - B0							
Reset value	B(9:0) = 3FF							

ECC end buffer start sector unit number of the current buffer.
This data is valid until the next ECCMPT($4A) Interrupt. Immediate ECC end when ECCST($12)->'L'. The value at ECCST($12)->'L'(ECC completed <or stopped> block no.>) is read.

* Transferring End Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
84	B9 - B8							
85	B7 - B0							
Reset value	B(9:0) = 1FF							

Current transfer data buffer unit number sent to the A/V decoder or ROM decoder after decoding. This data is valid until the next TOSINT($4A) Interrupt. Finishes up to the sector at TRST($12)->'L' and outputs the transfer end sector unit number.

* DSI Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
86	B9 - B8							
87	B7 - B0							
Reset value	B(9:0) = 000							

Buffer unit number that contains the DSIFG($4A) DSI sector.
This data is valid until the next DVDSINT($4A) Interrupt.

* Descramble End Sector Unit Number								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
88	B9 - B8							
89	B7 - B0							
Reset value	B(9:0) = 3FF							

Current descrambled buffer sector unit number.

* Remaining Data Size (Sector Unit Number)								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
8A	B9 - B8							
8B	B7 - B0							
Reset value								

The value remaining after subtracting the unit number transferred to either the A/V decoder or ROM decoder from the unit number of the descrambled sector in the buffer. This indicates the remaining transferrable data.

* ECC End ID Address								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
94	B31 - B24							
95	B23 - B16							
96	B15 - B8							
97	B7 - B0							
Reset value	X	X	X	X	X	X	X	X

ID address of the error corrected buffer start sector unit number. This data is valid until the next ECCMPT Interrupt.

* DSI ID Address								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
9C	B31 - B24							
9D	B23 - B16							
9E	B15 - B8							
9F	B7 - B0							
Reset value	X	X	X	X	X	X	X	X

The ID address of the DSI sector saved in the buffer after DSIFG($4A) start.
This data is valid until the next DVDSINT Interrupt.

For Servo: Micom Write Register & Read/Write Register Table (Samsung Pick-up Mecha Used)

Action Command

Commands A0-A6 are called action commands because they are directly related the actual servo and, if these commands are received during repeat jumps, they stop the jumps.

A0	STPcmd			
bit	**Name**	**Description**		**def.**
DH7	STOP		STOP mode. This bit can be used in any mode.	1
		1	STOP mode reserve.	
		0	Checks the lower bit without doing anything	
DH6	ABRT		Stops JMPcmd (A5H) or adjustment related servo operations.	0
		1	Stop	
		0	Checks the lower bit without doing anything.	
DH5	IDLE		IDLE (POWER SAVE) MODE. RAM DATA is present. However, this mode only operates in the STOP mode.	0
		1	IDLE MODE.(SSP1611 speed becomes 1/256.)	
		0	IDLE MODE changes to NORMAL MODE.	
DH4	LDX		Bit that turns on /off the laser diode. Only operates in the stop mode.	0
		1	Laser diode On	
		0	Laser diode Off	
DH3	0			0
DH2	0			0
DH1	0			0
DH0	0			0
DL7	x			x
:				
DL0				

It stops the JMPcmd ($A5) or Auto adjustment related servo actions or changes the servo to stop mode. Furthermore, it can reduce the power consumption when the servo has stopped by lengthening the ssp1611 frequency, and it can turn on/off the laser diode.
(It first checks to see if STOP>ABRT. IDLE and LDX are the same.) STOP reserve waits to stop the operating mode. When STOP is reserved, re-pull_in is not allowed. When MON signal becomes low, the servo enters the real stop mode. However, if the stop cmd (A080) is re-executed during reserve stop, then the servo immediately stops.
¢Ñ When STOP = 1 and ABRT = 0, the servo is initialized and automatically controlled values do not change.
When STOP = 1 and ABRT = 1, the servo is initialized and automatically controlled values change.
Sometimes, it is used during tray off.

A1	DDTcmd			
bit	**Name**	**Description**		**def.**
DH7	AUTO		FOCUS SEARCH MODE setting	0
		1	MANUAL MODE (SENSE : FZC)	
		0	AUTO MODE (SENSE : READY/BUSY)	
DH6	UPDN		Valid when AUTO BIT "1" . ¡Ø When AUTO=0 and UPDN=1, it reverses the focus search direction.	0
		1	DOWN ; ACTUATOR DOWN	
		0	UP ; ACTUATOR UP	
DH5	FIGA		Changes the focus input gain using the FE level.	1
		1	Sets to 0dB.	
		0	Changes	
DH4	FBAL		When DDTcmd executes, this controls the F-bal such that the absolute values of the focus S-curve minimum and maximum values are the same.	1
		1	No control	
		0	Control	
DH3	FoFa		Offset control status during DDTcmd	1
		1	No control	
		0	control	
DH2	FSP2	Bit that controls the DDTcmd and focus pull-in actuator speed. (only when k = 3)		0
DH1	FSP1			0
DH0	FSP0			1
DL7 : DL0	x			x

FPS2	FPS1	FPS0	SPEED
0	0	0	3.5Hz
0	0	1	1.7Hz
0	1	1	0.87Hz
1	1	1	0.43Hz

Automatically turns on the laser diode. It makes the focus actuator search at the speed set by Focus FSP[2:0] to determine the disc status . Furthermore, after this command, information such as disc status, cd or dvd disc, and dvd single or double are saved in buffer to be read by the SYSCON.

¢Ñ After DDTcmd, DATA that SYSCON can reference

1.S-curve Peak Data(Ram0 Bank0 1B address)

D15 D8				D7				D0
FE PEAK DATA	X	X	X	X	X	X	X	X

2) Individual data Flag (Ram0 Bank1 0A address)

D15 D8				D7				D0
X	DBL	FEpk	POS	0	0	0	DIN	X

	comment	1	0
DBL	layer type	DUAL LAYER	SINGLE LAYER
FEpk	decided level	greater	smaller
POS	distance from VREF to S-Curve	greater(likely CD)	smaller (likely DVD)

DIN	DISC status	yes	no

A2	FONcmd			
bit	**Name**	**Description**		**def.**
DH7	LYRX		Bit that selects the pull-in layer in the DVDP. (For CDP, set to 'L')	
		1	If the focus has not been pulled -in , pulls-in to layer 1. If the focus has been pulled in, jumps to layer 1. When FMTHD=H, try to pull in from the bottom to the top	
		0	If the focus has not been pulled -in , pulls-in to layer 0. If the focus has been pulled in, jumps to layer 0. When FMTHD=H, try to pull in from the top to the bottom	
DH6	FMTHD		Focus pull-in method	1
		1	Try to pull-in in one direction, to the top of the S-Curve or to the bottom.	
		0	Try to pull-in both directions, top of the S-Curve and bottom.	
DH5	FOPI		Select bit that decides whether to automatically focus pull-in in the set range after drop out	1
		1	No automatic pull -in	
		0	Automatic pull-in	
DH4	FSPC		Focus pull-in automatic speed control setting bit. (The search speed reduces by half as the focus actuator comes close to the pull-in location.)	0
		1	Automatic speed control	
		0	No automatic speed control	
DH3	0			0
DH2	0			0
DH1	0			0
DH0	0			0
DL7 : DL0	x			x

This command starts the focus pull-in and automatically turns on the laser diode. If the focus is on when this command is received, there is no movement. If FONcmd comes after the TONcmd (A3H), only the tracking servo turns off .

.Direct Acces Command : S-Curve ok Level : Fil (Ram0 Bank0 01 address)
S-Curve Pull in Level: Fpl (Ram0 Bank0 02 address)

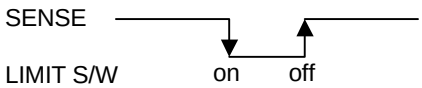
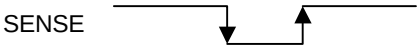
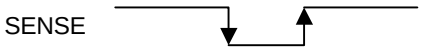
¢Ñ Example

S-Curve ok LEVEL : FOCUS Pull in level

4000H : 4000H FEpk/2 : FEpk/2
2000H : 2000H FEpk/4 : FEpk/4

A3	TONcmd			
bit	**Name**	**Description**		**def.**
DH7	TLRX		Tracking on after layer jump(For CDP, set to "L")	
		1	Starts tracking pull-in by jumping to layer 1.	
		0	Starts tracking pull-in by jumping to layer 0.	
DH6	SLSV		Sled Servo On.	0
		1	Does not turn on the sled servo during tracking pull-in.	
		0	Automatically turns on the sled servo during tracking pull-in.	
DH5	TRPI		Tracking pull-in method setting	1
		1	Does not use tracking kick pulse during pull - in.	
		0	Does use tracking kick pulse during pull-in	
DH4	TOLB		Lens brake when the tracking is on.	1
		1	Lens Brake	
		0	No Lens Brake	
DH3	MTLB		Manual Tracking Lens Brake	0
		1	Lens Brake	
		0	No Lens Brake	
DH2	SFOG		Search Focus Gain Setting	1
		1	Gain Down	
		0	Gain Normal	
DH1	STRG		Tracking gain setting at end of search	1
		1	Gain up	
		0	Gain Normal	
DH0	DGs		Tracking gain select during tDFCT period when defect had been detected.	0
		1	STRG invalid.(always tracking gain normal)	
		0	STRG valid.(gain determined by STRG)	
DL7 : DL0	x			x

Tracking Pull-in command.
If the tracking is on when this command is received, there is no movement.

<table>
<tr><th>A4</th><th colspan="3">SLDcmd</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>DH7</td><td>HOME</td><td></td><td>SLED HOME_IN MODE setting</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>AUTO SLED HOME_IN CONTROL MODE. When this bit is set, the sled motor moves backwards until the detection of the limit s/w and then, from this point on, it moves forward only for duration set by TMS3~0=1001 in the TMScmd (ACH).
 
</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Normal SLED CONTROL MODE</td><td></td></tr>
<tr><td>DH6</td><td>SMOV</td><td></td><td rowspan="2">Bit that controls the sled on/off and moves
<table><tr><th>SMOV</th><th>SPLY</th><th></th></tr><tr><td>0</td><td>0</td><td>Sled Off</td></tr><tr><td>0</td><td>1</td><td>Sled On</td></tr><tr><td>1</td><td>0</td><td>Sled Forward move. When the maximum outer track is reached, signal is transferred to sense.
 
</td></tr><tr><td>1</td><td>1</td><td>Sled Backward move. When the limit s/w is reached, signal is transferred to sense.
 
</td></tr></table></td><td></td></tr>
<tr><td>DH5</td><td>SPLY</td><td></td><td></td></tr>
<tr><td>DH4</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH3</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH2</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH1</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH0</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DL7</td><td rowspan="3">x</td><td></td><td></td><td rowspan="3">x</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>DL0</td><td></td><td></td></tr>
</table>

This command controls the sled motor. Bit check starts from the home bit.
¢Ñ SENSE data : When HOME=H,BUSY and ,when L, READY
¢Ñ This command can be used to manually move the sled in the focus pull-in state.
(In this case, sense produces the TZC or FG signal through sns of the HWDcmd.)

<table>
<tr><th>A5</th><th colspan="3">JMPcmd</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>DH7</td><td>DIR</td><td></td><td>Jump direction assignment</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Reverse jump</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>Forward jump</td><td></td></tr>
<tr><td>DH6</td><td>JPM1</td><td colspan="2">Jump type select bit
<table><tr><th>JPM1</th><th>JPM0</th><th></th></tr><tr><td>0</td><td>0</td><td>Tracking jump or sled jump is executed according the to the number of jump tracks. The jump type changes depending on the OKScmd (ADH)'s boundary.</td></tr><tr><td>0</td><td>1</td><td>Tracking jump</td></tr><tr><td>1</td><td>0</td><td>SLED MOVE</td></tr><tr><td>1</td><td>1</td><td>Repeat track jump for every interval set in JIT2-0.</td></tr></table></td><td></td></tr>
<tr><td>DH5</td><td>JPM0</td><td colspan="2"></td><td></td></tr>
<tr><td>DH4</td><td>JIT2</td><td colspan="2">Bit that sets the time interval for the repeat track jump.
This period starts from the jump start time to the next jump start time.
<table><tr><th>JIT[2]</th><th>JIT[1]</th><th>JIT[0]</th><th>XTAL = 0</th><th>XTAL = 1</th></tr><tr><td>0</td><td>0</td><td>0</td><td colspan="2">MANUAL JUMP MODE (When JPD9~0 are all' 0', use the syscon dirc pin)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>2.7Hz</td><td>5.4Hz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>5.4Hz</td><td>5.4Hz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8.1Hz</td><td>8.1Hz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>13.5Hz</td><td>13.5Hz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>21.6Hz</td><td>21.6Hz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>29.7Hz</td><td>29.7Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>40.5Hz</td><td>40.5Hz</td></tr></table></td><td></td></tr>
<tr><td>DH3</td><td>JIT1</td><td colspan="2"></td><td></td></tr>
<tr><td>DH2</td><td>JIT0</td><td colspan="2"></td><td></td></tr>
<tr><td>DH1</td><td>JPD9</td><td colspan="2">If the following conditions are satisfied, the manual jump mode stops and sets the sense output to 'H'.
<table><tr><th>JPD[9]</th><th>JPD[8]</th><th></th></tr><tr><td>0</td><td>0</td><td>X (not used)</td></tr><tr><td>0</td><td>1</td><td>COUNT(assigned track number)</td></tr><tr><td>1</td><td>0</td><td>Tstp (mirr period)</td></tr><tr><td>1</td><td>1</td><td>COUNT OR Tstp</td></tr></table></td><td></td></tr>
<tr><td>DH0</td><td>JPD8</td><td colspan="2"></td><td></td></tr>
<tr><td>DL7
:
DL1</td><td>JPD[7:0]</td><td></td><td>If the JPM[1:0] bit is not 11, JIT[2:0] bit changes to the JPD[12:10] bit.
The jump track number is DATA*8 only when JPM[1:0] BIT is 10, otherwise it remains the same.
When JMP[1:0]=10(SLED move), data *8 becomes the actual jump track number.</td><td></td></tr>
</table>

Sled and tracking jump command. Normal play mode after jump.

A6	CDScmd			
bit	**Name**	**Description**		**def.**
DH7	WHIN		Decides on how to use the Tilt input pin.	1
		1	Tracking Error for tracking average and anti shock aliasing.	
		0	Tilt input	
DH6	STSP		Spindle Filer on or off in standby (stop mode)	1
		1	Spindle Filter on.	
		0	Spindle Filter off.	
DH5	FSOS		S-curve DETECT only in one direction during focus search (DDT)	1
		1	Single direction DETECT.	
		0	Bi-directional DETECT.	
DH4	DPSI		Decides on the send method of the depth control output to the RF chip during depth control	1
		1	Transmission by I/F with MICOM	
		0	Transmission by servo	
DH3	PLLS		PLL Hold signal select	1
		1	Hold all areas of track under lens brake	
		0	Hold only those areas under lens brake	
DH2	JPCC		Changes the hardware counter clock during speed control sled move , which uses the Mirr or TZC.	0
		1	change	
		0	no change	
DH1	JPFC		Converts high speed search to fine search during speed control sled move , which uses the Mirr or TZC.	0
		1	Convert	
		0	No convert	
DH0	FSHF		DDT Half Search	0
		1	Half Search only	
		0	Full Search	
DL7				x
:				
DL0				

CONDITION COMMAND.
Can assign desired functions suitable to each system.

SYSTEM SETTING COMMAND

<table>
<tr><th>A7</th><th colspan="3">EMEcmd</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td rowspan="3">DH7</td><td rowspan="3">FDOL</td><td></td><td>Pull-in layer select bit at focus drops out</td><td rowspan="3">0</td></tr>
<tr><td>1</td><td>Pull-in without layer check.</td></tr>
<tr><td>0</td><td>Automatically finds the dropped out layer and pulls it in.</td></tr>
<tr><td rowspan="3">DH6</td><td rowspan="3">SLST</td><td></td><td>Select bit that decides whether to stop the sled when the lock signal is off.</td><td rowspan="3">1</td></tr>
<tr><td>1</td><td>STOP .</td></tr>
<tr><td>0</td><td>No STOP</td></tr>
<tr><td rowspan="3">DH5</td><td rowspan="3">RPT</td><td></td><td>Controls the number of actuator's up/down searches</td><td rowspan="3">0</td></tr>
<tr><td>1</td><td>REPEAT SEARCH (continue until next command input)</td></tr>
<tr><td>0</td><td>Search once</td></tr>
<tr><td rowspan="3">DH4</td><td rowspan="3">upFv</td><td></td><td>FSval(PICK UP location DATA)updating after focus pull</td><td rowspan="3">0</td></tr>
<tr><td>1</td><td>update</td></tr>
<tr><td>0</td><td>not update</td></tr>
<tr><td rowspan="3">DH3</td><td rowspan="3">DSAS</td><td rowspan="2"></td><td>Disable Anti-Shock
<table>
<tr><th>TRPI</th><th>DSAS</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>Track pull-in using kick pulse during ATSC at off track</td></tr>
<tr><td>0</td><td>1</td><td>Kick pull-in when Mirr appears during play at off track</td></tr>
<tr><td>1</td><td>0</td><td>Select among 3 (ASBR,ASFO,ASTR)</td></tr>
<tr><td>1</td><td>1</td><td>X (let alone and leave it to servo)</td></tr>
</table></td><td rowspan="3">1</td></tr>
<tr><td>1</td><td>Disable</td></tr>
<tr><td>0</td><td>Enable</td></tr>
<tr><td rowspan="3">DH2</td><td rowspan="3">ASFO</td><td></td><td>Select bit that decides whether to down the focus gain after a shock</td><td rowspan="3">1</td></tr>
<tr><td>1</td><td>Focus gain down.</td></tr>
<tr><td>0</td><td>Maintain normal focus gain</td></tr>
<tr><td rowspan="3">DH1</td><td rowspan="3">ASTR</td><td></td><td>Select bit that decides whether to up the tracking gain after a shock</td><td rowspan="3">1</td></tr>
<tr><td>1</td><td>Up tracking gain</td></tr>
<tr><td>0</td><td>Maintain normal tracking gain</td></tr>
<tr><td rowspan="3">DH0</td><td rowspan="3">ASBR</td><td></td><td>Lens brake during the anti-shock period</td><td rowspan="3">1</td></tr>
<tr><td>1</td><td>brake</td></tr>
<tr><td>0</td><td>no brake</td></tr>
<tr><td rowspan="3">DL7
:
DL0</td><td rowspan="3">-</td><td></td><td></td><td rowspan="3">x</td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
</table>

Defect/Shock emergency measures.

A8	HDWcmd			
bit	**Name**	**Description**		**def.**
DH7	enTT		Tilt control	0
		1	Normal Tilt .	
		0	"H" during a track jump or move	
DH6	LIM		Signal used for stopping at the innermost track	0
		1	Stops the sled if there is no FG pulse during the FG stop time of TMScmd (ACH).	
		0	Uses the limit S/W connected to the SSTOP pin. When it is "H", STOP.	
DH5	enASin		ANTI SHOCK FILTER Select	0
		1	Uses external filter	
		0	Uses internal filter	
DH4	SNS		Signal used at SLED MOVE	0
		1	FG PULSE	
		0	TZC and MIRR	
DH3	PCUP		PICK UP type	1
		1	Vibration non resistant PICK UP	
		0	Vibration resistant PICK UP	
DH2	DOFO		FOCUS HOLD status after defect	1
		1	not hold.	
		0	hold.	
DH1	DOTR		TRACKING HOLD status after defect	0
		1	not hold	
		0	hold	
DH0	XTAL		Bit that selects the external X-tal frequency	1
		1	X-tal = 33.9MHz, sampling frequency =151.2kHz	
		0	X-tal = 16.9MHz, sampling frequency =75.6kHz	
DL7				
:	-			x
DL0				

Changes the H/W specification of DSSP. After cancelling the reset, this command is the first command used. This command cannot be used in modes other than the standby mode.

A9	INIcmd			
bit	**Name**	**Description**		**def.**
DH7	SLDO		Decides on how to sled output (sled output) during speed control track jump.	0
		1	through the sled filter	
		0	as is	
DH6	JPCK		Signal used when sled moving using a sled motor without a sensor.(TRACK COUNTER CLOCK)	1
		1	MIRR	
		0	TZC	
DH5	TKJM		TRACKING JUMP method	0
		1	Speed control	
		0	No speed control	
DH4	JPEC		Error correction when the sled jump past the jump number during sled move or track jump.	0
		1	compensate	
		0	does not compensate	
DH3	BJJM		After a sled move using the JMPcmd(A5H) boundary, the status on the remaining number of tracks.	0
		1	Jumps the remaining number of tracks after a kick break sled move using the Mirr or PS	
		0	No jump	
DH2	BTS		The Mirr cycle that determines the where to stop during a track jump (Falling to Falling)	0
		1	Stops when it becomes greater than TMScmd(ACH)'s Jstp DATA	
		0	Stops when it becomes the same as the initial jump Mirr cycle (Rising to Rising).	
DH1	SMM		SLED MOVE Method(use in combination with SNS)	1
		1	Speed control move.	
		0	No speed control	
DH0	SLB		Lense Brake after jump.	0
		1	Brake only once for the duration of gain up time when mirror appears.	
		0	Brake everytime mirror appears.	
DL7	-			x
:				
DL0				

Initial value setting command.

AA	MSCcmd		
bit	**Name**	**Description**	**def.**
DH7	MD11	When data read, CMD FFF MSS[3:0] .MSS[3:0]: RAM SELECT bit to be set .MD[11:0]: DATA at write (MSS0h-ah:RAM D[15:4], MSSbh-fh:RAM D[11:0])	
DH6	MD10		
DH5	MD9		
DH4	MD8		
DH3	MD7		
DH2	MD6		
DH1	MD5		
DH0	MD4		
DL7 : DL0	MD[3:0] MSS[3:0]		

MSS [3:0]	Parameter Name	CONTENTS	Def.	Data area	RAM Address
0h	FSpk	Output control coefficient during focus search pull-in	4000	upper	0055
1h	TSpk	The maximum voltage applied to track out during depth control	0800	upper	0056
2h	tDFCT	No gain change for the duration of this time after DFCT.	1000	upper	0057
3h	tOFa	Focus Tracking offset measurement time	1B90	upper	0058
4h	FBpd	Focus balance period	3000	upper	0059
5h	TBwt	Tracking balance wait Time	2274	upper	005a
6h	Sbrk	MIRR OR TZC SLED MOVE BREAK TIME	14AC	upper	005b
7h	FGmax	top focus gain	0060	upper	005c
8h	FGmin	Minimum focus gain	0018	upper	005d
9h	TGmax	Maximum tracking gain	0018	upper	005e
ah	TGmin	Minimum tracking gain	0018	upper	005f
bh	tTpi	kick track pull in time	0018	lower	0060
ch	nTbal	Tracking balance track number	0010	lower	0061
dh	LTrN	Mirr or TZC high speed control brake constant	0014	lower	0062
eh	Ffrq	Focus Auto Gain unit bandwith	000A	lower	0074
fh	Tfrq	Track Auto Gain unit bandwith	000B	lower	0078

¢Ñ set time=Interrupt frequency * set value = 6.6 usec* set value(33.9MHz)

¢Ñ Except tDFCT, which is 16

= 12.2usec*set value(16.9MHz)
= 105 usec*set value(33.9MHz)
= 210 usec*set value(16.9MHz)

Remaining coefficient required for system operation.

AB	SPDcmd			
bit	Name	Description		def.
DH7	DKS1		CD-ROM/DVD/LD select bit	
		1	DVD	
		0	CD-ROM/CD/LD	
DH6	DKS0		Filter coefficient setting select	
DH5	0			0
DH4	VCT		Vector setting to read SQ/iD for DSK1	
		1	Not set	
		0	Set.	
DH3	0			0
DH2	0			0
DH1	SPD1		Speed select bit	
DH0	SPD0		Speed select bit	
DL7	-			x
:				
DL0				

DVD/CD-ROM and speed related command.

Xtal	DSK1	DSK0	SPD1	SPD0	Function
0	0	0	¡¿	¡¿	CD-ROM 1X/2X
0	0	1	¡¿	¡¿	CD-ROM 4X
0	1	0	¡¿	¡¿	DVD
0	1	1	¡¿	¡¿	DVD
1	0	0	0	0	CD-ROM 1X
1	0	0	0	1	CD-ROM 2X
1	0	0	1	0	CD-ROM 4X
1	0	0	1	1	CD-ROM 8X
1	0	1	¡¿	¡¿	LD
1	1	0	¡¿	¡¿	DVD
1	1	1	0	0	DVD 1X
1	1	1	0	1	DVD 2X
1	1	1	1	0	DVD
1	1	1	1	1	DVD

AC	TMScmd		
bit	Name	Description	def.
DH7	TD11	When DATA READ, CMD FFF TMS[3:0] .TMS[3:0] : TIME SELECT bit to be set .TD[11:0] : DATA(RAM:D[11:0])	
DH6	TD10		
DH5	TD9		
DH4	TD8		
DH3	TD7		
DH2	TD6		
DH1	TD5		
DH0	TD4		
DL7 : DL0	TD[3:0] TMS[3:0]	¢Ñ Setting time = Interrupt frequency* set value = 6.6usec* set value (33.9MHz) = 13.2usec* set value(16.9MHz)	

TMS [3:0]	Parameter Name	CONTENTS	Def.	Data area	RAM Addr
0h	Jstbl	Stable time after jump	0300	lower	0041
1h	tFpi	Tracking pull in time after focus pull in	0014	lower	0042
2h	Tstbl	Track jump stable time	0001	lower	0043
3h	Twin	TZC blind TIME at tracking jump	0014	lower	0044
4h	MSTP	Use the value obtained by subracting MSTP time from the first Mirr duty (rising to rising) during earch as the stop condition	0003	lower	0045
5h	GuT	Track Gain Up Time after jump	0300	lower	0046
6h	Jstp	Stops the track jump when Mirr cycle exceeds Jstp during track jump.	0060	lower	0047
7h	FGjsp	Track Pull in when PS is output for more than this time during PS jump.	0300	lower	0048
8h	FGstp	Track Pull in when position sensor is not output for more than this time at home in	0800	lower	0049
9h	tHFwd	Forward Move time after home -in	0300	lower	004a
ah	DFCTpd	DFCT continuous processing time	0040	lower	004b
bh	ATSCd	ATSC continuous processing time	0800	lower	004c
ch	FLoff	FLKB off time	0300	lower	004d
dh	FLon	FLKB on time	0014	lower	004e
eh	TLoff	TLKB off time	0001	lower	004f
fh	TLon	TLKB on time	0200	lower	0050

Initial value setting command1.

AD	OKScmd		
bit	Name	Description	def.
DH7	OD11	When DATA READ, CMD FFF OKS[3:0] .OKS[3:0] : TIME SELECT bit .OD[11:0] : DATA(RAM:D[11:0])	
DH6	OD10		
DH5	OD9		
DH4	OD8		
DH3	OD7		
DH2	OD6		
DH1	OD5		
DH0	OD4		
DL7	OD[3:0] OKS[3:0]		
:			
DL0			

OKS [3:0]	Parameter Name	CONTENTS	Def.	Data area	RAM Addr.
0h	FBok	Focus balance ok level	0800	lower	10b0
1h	TBok	Tracking balance ok level	0800	lower	10b1
2h	FGok	Focus gain ok level	0200	lower	10b2
3h	TGok	Tracking gain ok level	0080	lower	10b3
4h	DPok	Depth variance ok level	0080	lower	10b4
5h	FSjspd	Stop fine search speed control	0003	lower	10b5
6h	TSjspd	Stop track jump speed control	0003	lower	10b6
7h	PSjspd	Stop sled move speed control	0003	lower	10b7
8h	Cchg	(C.out)and (TZC/MIRR) select during track ump to ck.	0100	lower	10b8
9h	bound	Track jump and Sled move boundary	0100	lower	10b9
ah	bound2	Fine search and PS jump boundary	0281	lower	10ba
bh	SMcnt	Time from track kick to sled move	0008	lower	10bb
ch	SScnt	Sled move break time	0080	lower	10bc
dh	ENTc	Track number per PS pulse(from Micom)	0069	lower	10bd
eh	nDP	DEPTH CONTROL PICK UP frequency	0028	lower	10be
fh	Dialw	RESERVED (HST DISTANCE ALLOWANCE)	0100	lower	10bf

Initial value setting COMMAND2.
¢Ñ Detailed description of FSjspd, TSjspd and PSvjspd (TABLE Size:32)

1.FSjspd (default: 0803 :upper 13bit:080 lower 3bit:3)
upper 13bit: 080 : 0000 1000 0000 0:Number of '0' before 1 4-1=3 →2x2x2=8
8 : → Break start when the number of remaining tracks reaches 256.
lower 3bit : 3 : Pull in speed after jump(see Table below, 1.92kHz)
Example) FSjspd (0402 :upper 13bit:040 lower 3bit:2)
upper 13bit : 040 : 0000 0100 0000 0:Number of '0' before 1 5-1=4 →2x2x2x2=16
16 :→ Break start when the number of remaining tracks reaches 256x2.
lower 3bit : 2 : Pull in speed after jump(Table below, 2.26kHz)

2.TSjspd (default: 1003 :upper13bit:100 lower 3bit:3)
upper13bit : 100 : 0001 0000 0000 0:Number of '0' before 1 3-1=2 → 2x2=4
8 : →Break start when the number of remaining tracks reaches 256.
lower 3bit : 3 : Pull in speed after jump(see Table below, 1.92kHz)

3.PSvjspd (default: 0103 :upper13bit:010 lower 3bit:3)
upper13bit : 010 : 0000 0001 0000 0: Number of '0' before 1 7-1=6 → 2x2x2x2x2x2=64
128 : →Break start when the remaining number of remaining ps reaches 68
(mirr: applicable to 4352).
lower 3bit : 3 : Pull in speed after jump(see Table below, PS frequency = 169Hz)

Mirr frequency when system clock 34 MHz (same with 17MHz)					
FSjspd		TSjspd		PSvjspd (PS frequency)	
0h	3.04kHz	0h	3.04kHz	0h	263Hz
1h	2.67kHz	1h	2.67kHz	1h	232Hz
2h	2.26kHz	2h	2.26kHz	2h	200Hz
3h	1.92kHz	3h	1.92kHz	3h	169kHz
4h	1.55kHz	4h	1.55kHz	4h	137Hz
5h	1.18kHz	5h	1.18kHz	5h	105Hz
6h	0.81kHz	6h	0.81kHz	6h	73.5Hz
7h	0.5kHz	7h	0.5kHz	7h	41.8Hz

AE	AJKcmd		
bit	Name	Description	def.
DH7	AD11	When DATA READ, CMD FFF AJS[3:0] .AJS[3:0] : RAM SELECT bit .AD[11:0] : WRITE DATA(RAM D[15:4])	
DH6	AD10		
DH5	AD9		
DH4	AD8		
DH3	AD7		
DH2	AD6		
DH1	AD5		
DH0	AD4		
DL7 : DL0	AD[3:0] AJS[3:0]		

AJS [3:0]	Parameter Name	CONTENTS	Def.	data	RAM Add.
0h	FKLL	Brake point determination level during layer jump	3000	upper	0024
1h	TKj_k	Track Jump Kick Break Duty Coefficient	3D00	upper	0025
2h	FSj_k	Fine Search gain control coefficient	1800	upper	0026
3h	TSj_k	Tracking speed control jump gain coefficient	1800	upper	0027
4h	PSj_k	PS Sled move speed control gain coefficient	1000	upper	0028
5h	SL_k	Position sensor sled move kick break duty coefficient	5A00	upper	0029
6h	TKl_k	Track Break level coefficient during track jump(DATA)*2	4000	upper	002a
7h	SMl_k	Sled break level coefficient (DATA)*2 during track jump. During speed control track jump, (DATA)*32 to SLD0	4000	upper	002b
8h	FSPKL	LAYER JUMP BREAK Level	4000	upper	002c
9h	Jbuf	Mirr or Cout save buffer	-	-	002d
ah	DPk	DEPTH CONTROL GAIN	1000	upper	002e
bh	dXbuf	FOCUS BALANCE initial KICK LEVEL	3000	upper	002f
ch	FBk	Focus balance sensitivity coefficient	7FFF	upper	0030
dh	TBk	Tracking balance sensitivity coefficient	0A00	upper	0031
eh	Kcf	FGAcmd½Ã GAIN sensitivity coefficient	0800	upper	0032
fh	Kct	TGAcmd½Ã GAIN sensitivity coefficient	0800	upper	0033

Initial value setting COMMAND3.

AF	LEScmd

<table>
<tr><th>bit</th><th>Name</th><th>Description</th><th>def.</th></tr>
<tr><td>DH7</td><td>LD11</td><td rowspan="11">DATA READ, CMD FFF LES[3:0]
.LES[3:0] : RAM SELECT bit
.LD[11:0] : WRITE DATA(RAM D[15:4])

<table>
<tr><th>LES [3:0]</th><th>Parameter Name</th><th>CONTENTS</th><th>Def.</th><th>data</th><th>RAM Addr.</th></tr>
<tr><td>0h</td><td>TKCKd</td><td>Track Kick level during track jump</td><td>1000</td><td>upper</td><td>10c0</td></tr>
<tr><td>1h</td><td>SKCKd</td><td>Sled Move Level</td><td>4000</td><td>upper</td><td>10c1</td></tr>
<tr><td>2h</td><td>TKlvl</td><td>Track Kick level during sled move</td><td>7000</td><td>upper</td><td>10c2</td></tr>
<tr><td>3h</td><td>SMlvl</td><td>Sled Move Level during track jump</td><td>4000</td><td>upper</td><td>10c3</td></tr>
<tr><td>4h</td><td>xGwt</td><td>Loop gain stable time</td><td>7F00</td><td>upper</td><td>10c4</td></tr>
<tr><td>5h</td><td>xGcnt</td><td>Loop gain count time</td><td>1000</td><td>upper</td><td>10c5</td></tr>
<tr><td>6h</td><td>FSrng</td><td>Focus Search Limit Level</td><td>1000</td><td>upper</td><td>10c6</td></tr>
<tr><td>7h</td><td>POS_J</td><td>CD DVD determination level using the distance from Vref to layer</td><td>1B90</td><td>upper</td><td>10c7</td></tr>
<tr><td>8h</td><td>DDT_J</td><td>Disc status ;level</td><td>1000</td><td>upper</td><td>10c8</td></tr>
<tr><td>9h</td><td>Fpk_J</td><td>CD DVD determination level using the Scurve</td><td>3000</td><td>upper</td><td>10c9</td></tr>
<tr><td>ah</td><td>Bmin_k</td><td>Minimum brk time (kick time %)</td><td>1000</td><td>upper</td><td>10ca</td></tr>
<tr><td>bh</td><td>AS_J</td><td>ANTI SHOCK Level</td><td>1800</td><td>upper</td><td>10cb</td></tr>
<tr><td>ch</td><td>NZlvl</td><td>Focus search noise level</td><td>0800</td><td>upper</td><td>10cc</td></tr>
<tr><td>dh</td><td>SFok</td><td>DDT or Layer Jump hysteresis Level</td><td>1000</td><td>upper</td><td>10cd</td></tr>
<tr><td>eh</td><td>LYdt</td><td>CD DVD determination level using the dist between levels</td><td>0800</td><td>upper</td><td>10ce</td></tr>
<tr><td>fh</td><td>FZCofs</td><td>Focus zero crossing offset level</td><td>0A00</td><td>upper</td><td>10cf</td></tr>
</table>
</td><td></td></tr>
<tr><td>DH6</td><td>LD10</td></tr>
<tr><td>DH5</td><td>LD9</td></tr>
<tr><td>DH4</td><td>LD8</td></tr>
<tr><td>DH3</td><td>LD7</td></tr>
<tr><td>DH2</td><td>LD6</td></tr>
<tr><td>DH1</td><td>LD5</td></tr>
<tr><td>DH0</td><td>LD4</td></tr>
<tr><td>DL7
:
DL0</td><td>LD[3:0]
LES[3:0]</td></tr>
</table>

Initial value setting COMMAND4

B0	AARWcmd		
bit	**Name**	**Description**	**def.**
DH7	AA11	DATA READ, CMD FFF MSS[3:0] .AAS[3:0] : RAM SELECT bit to be set .AA[11:0] : WRITE DATA (RAM D[15:4])	
DH6	AA10		
DH5	AA9		
DH4	AA8		
DH3	AA7		
DH2	AA6		
DH1	AA5		
DH0	AA4		
DL7 : DL0	AA[3:0] AAS[3:0]		

AAS [3:0]	Parameter Name	CONTENTS	Def.	data	RAM Address
0h	FinG	Focus input Gain	0000	upper	10a6
1h	TinG	Tracking input Gain	0000	upper	10a7
2h	Fofst	Focus offset	0000	upper	1082-3
3h	Tofst	Tracking offset	0000	upper	1084-5
4h	Fbal	Focus balance	0000	upper	1086
5h	Tbal	Tracking balance	0000	upper	1087
6h	Fbias	Focus bias	0000	upper	1088
7h	Tbias	Tracking bias	0000	upper	1089
8h	FODbias	Focus output bias	0000	upper	1090
9h	Travrg	Tracking output average	0000	upper	10f3
ah	SLavrg	Sled output average	0000	upper	1095
bh	DPctl	Depth control result	0000	upper	10af
ch	GND	Vref average	0000	upper	1080-1
dh	RF_env	RF ENVELOPE average result	0000	upper	1092-3
eh	DDTdt	DATA after disc detect	0000	lower	100a

Auto Adjusted data can be read/written.

Automatic control command

B1	OFAcmd			
bit	**Name**	**Description**		**def.**
DH7	FTS		FOCUS or tracking offset adjust is selected.	0
		1	TRACKING OFFSET ADJUSTMENT.	
		0	FOCUS OFFSET ADJUSTMENT.	
DH6	LDOF		Offset Laser diode on/off status	0
		1	Turns off the laser diode	
		0	Turns on the laser diode.	
DH5	U/B		Focus actuator move direction when FOK is high during offset control	1
		1	Pulls down the actuator to control the offset until FOK becomes low.	
		0	Pulls up the actuator to control offset until the FOK becomes low.	
DH4	0			0
DH3	0			0
DH2	0			0
DH1	0			0
DH0	0			0
DL7 : DL0	-			x

Measures and adjusts the focus and tracking errors when the laser is on using the auto focus / tracking offset adjust command.

B2	FBAcmd			
bit	**Name**	**Description**		**def.**
DH7				
DH6				
DH5				
DH4				
DH3				
DH2				
DH1				
DH0				
DL7 : DL0				

Ends the focus balance adjust when the RF signal is the largest using the RF envelop signal. Use only after focus pull-in.

B3	TBAcmd			
bit	**Name**	**Description**		**def.**
DH7	TIGA		Changes the tracking input gain according to the TE level.	1
		1	No change	
		0	Change.	
DH6	RPTB		Determines repeat tracking balance control	1
		1	No repeat	
		0	repeat	
DH5	0			0
DH4	0			0
DH3	0			0
DH2	0			0
DH1	0			0
DH0	0			0
DL7 : DL0				x

Measures using the average of the TE max and min values, calculated from the deviation when the focus is on and tracking is off. Always use before entering play (tracking on).

B4	FGAcmd			
bit	**Name**	**Description**		**def.**
DH7				
DH6				
DH5				
DH4				
DH3				
DH2				
DH1				
DH0				
DL7 : DL0				

Auto Focus Gain Adjustment command.
Use only when focus and tracking servos are on.

B5	TGAcmd			
bit	Name	Description		def.
DH7				
DH6				
DH5				
DH4				
DH3				
DH2				
DH1				
DH0				
DL7 : DL0				

Auto Tracking Gain Adjustment Command.
Use only when focus and tracking servos are on.

B6	DPAcmd			
bit	Name	Description		def.
DH7				
DH6				
DH5				
DH4				
DH3				
DH2				
DH1				
DH0				
DL7 : DL0				

DEPTH CONTROL Command.
Controls when the focus servo is on but tracking servo is off.

<table>
<tr><th>B7</th><th colspan="3">EFMCcmd</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>DH31</td><td>LPFS</td><td></td><td>EFM LPF select</td><td>1</td></tr>
<tr><td></td><td></td><td>1</td><td>LPF_DVD select</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>LPF_CD select</td><td></td></tr>
<tr><td>DH30</td><td>RES2</td><td colspan="2">RFI HPF Input impedence
<table><tr><th>RES[2]</th><th>RES[1]</th><th>RES[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>0</td><td>47.0kΩ (X1 CD)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>23.5 kΩ (X2 CD)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>11.5 kΩ (X4 CD)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>6.0 kΩ (X8 CD)</td></tr><tr><td>1</td><td>0</td><td>0</td><td>7.5 kΩ (X1 DVD)</td></tr><tr><td>1</td><td>0</td><td>1</td><td>4.0 kΩ (X2 DVD)</td></tr></table></td><td>1</td></tr>
<tr><td>DH29</td><td>RES1</td><td colspan="2"></td><td>0</td></tr>
<tr><td>DH28</td><td>RES0</td><td colspan="2"></td><td>0</td></tr>
<tr><td>DH27</td><td>DSGA2</td><td colspan="2">DUTY SLICE FEEDBACK gain select
<table><tr><th>DSGA[2]</th><th>DSGA[1]</th><th>DSGA[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>0</td><td>x 0.50</td></tr><tr><td>0</td><td>0</td><td>1</td><td>x 1.00</td></tr><tr><td>0</td><td>1</td><td>0</td><td>x 2.50</td></tr><tr><td>0</td><td>1</td><td>1</td><td>x 3.75</td></tr><tr><td>1</td><td>0</td><td>0</td><td>x 5.00</td></tr><tr><td>1</td><td>0</td><td>1</td><td>x 7.50</td></tr><tr><td>1</td><td>1</td><td>0</td><td>x 10.00</td></tr><tr><td>1</td><td>1</td><td>1</td><td>x 10.00</td></tr></table></td><td>1</td></tr>
<tr><td>DH26</td><td>DSGA1</td><td colspan="2"></td><td>0</td></tr>
<tr><td>DH25</td><td>DSGA0</td><td colspan="2"></td><td>0</td></tr>
<tr><td>DH24</td><td>ENV_SEL</td><td></td><td>ENVELOPE SLICE select</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>ENVELOPE SLICE select</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>DUTY FEEDBACK SLICE select</td><td></td></tr>
</table>

EFM asymmetry and PLL control command.

<table>
<tr><th>B7</th><th colspan="3">EFMCcmd</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>DH23</td><td>ESGA1</td><td colspan="2" rowspan="2">.ESGA[1:0] : ENVELOPE SLICE GAIN control
<table><tr><th>ESGA[1]</th><th>ESGA[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>x 1.0</td></tr><tr><td>0</td><td>1</td><td>x 1.5</td></tr><tr><td>1</td><td>0</td><td>x 1.5</td></tr><tr><td>1</td><td>1</td><td>x 2.0</td></tr></table></td><td>0</td></tr>
<tr><td>DH22</td><td>ESGA0</td><td>1</td></tr>
<tr><td rowspan="3">DH21</td><td rowspan="3">PK_EN</td><td></td><td>DEFECT RF PEAKING prevention select (used with PK_CTL[1:0])</td><td rowspan="3">1</td></tr>
<tr><td>1</td><td>DEFECT HPF resistance open</td></tr>
<tr><td>0</td><td>DEFECT HPF resistance ignore (connect to GND)</td></tr>
<tr><td>DH20</td><td>PK_CTL1</td><td colspan="2" rowspan="2">Peaking prevention signal select based on PK_EN
<table><tr><th>PK_CTL[1]</th><th>PK_CTL[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>PEAKING PREVENTION OFF</td></tr><tr><td>0</td><td>1</td><td>PLLDFCT</td></tr><tr><td>1</td><td>0</td><td>CPEAK</td></tr><tr><td>1</td><td>1</td><td>PLLDFCT + CPEAK</td></tr></table></td><td>0</td></tr>
<tr><td>DH19</td><td>PK_CTL0</td><td>0</td></tr>
<tr><td>DH18</td><td>DFRL2</td><td colspan="2" rowspan="4">DEFECT(CPEAK) detection minimum cycle.
<table><tr><th>DFRL[2]</th><th>DFRL[1]</th><th>DFRL[0]</th><th>T</th></tr><tr><td>0</td><td>0</td><td>0</td><td>12</td></tr><tr><td>0</td><td>0</td><td>1</td><td>16</td></tr><tr><td>0</td><td>1</td><td>0</td><td>20</td></tr><tr><td>0</td><td>1</td><td>1</td><td>24</td></tr><tr><td>1</td><td>0</td><td>0</td><td>28</td></tr><tr><td>1</td><td>0</td><td>1</td><td>32</td></tr><tr><td>1</td><td>1</td><td>0</td><td>36</td></tr><tr><td>1</td><td>1</td><td>1</td><td>40</td></tr></table></td><td>0</td></tr>
<tr><td>DH17</td><td>DFRL1</td><td>0</td></tr>
<tr><td>DH16</td><td>DFRL0</td><td>0</td></tr>
</table>

EFM asymmetry and PLL control command.

B7	EFMCcmd			
bit	**Name**	**Description**		**def.**
DH15	EQ_HD		EQ CONTROL VOLTAGE HOLD	0
		1	HOLD ON(HOLD FOR CPEAK)	
		0	HOLD OFF	
DH14	EQ_FIX		EQ CONTROL VOLTAGE FIX	0
		1	VDD/2	
		0	NORMAL OPERATION	
DH13	DBAS		DOUBLE ASYMMETRY SLICE select	1
		1	DOUBLE ASYMMETRY	
		0	NORMAL ASYMMETRY	
DH12	DBASG		DOUBLE ASYMMETRY GAIN select	0
		1	2x	
		0	1X	
DH11	-			x
DH10	-			x
DH9	-			x
DH8	-			x

EFM Asymetry circuit and PLL control command.

<table>
<tr><th>B7</th><th colspan="3">EFMCcmd</th></tr>
<tr><th>bit</th><th>Name</th><th>Description</th><th>def.</th></tr>
<tr><td>DH7</td><td>PLLDFCT_SEL1</td><td rowspan="2">PLL HOLD C-PEAK AND DEFECT USE STATUS control bit

<table><tr><th>PLLDFCT_SEL[1]</th><th>PLLDFCT_SEL[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>PLL HOLD PLLDFCT USE.</td></tr><tr><td>0</td><td>1</td><td>PLL HOLD PLLDFCT AND CPEAK NOT USED.</td></tr><tr><td>1</td><td>0</td><td>PLL HOLD PLLDFCT AND CPEAK ARE 'OR' USED.</td></tr><tr><td>1</td><td>1</td><td>PLL HOLD CPEAK USED.</td></tr></table></td><td>0</td></tr>
<tr><td>DH6</td><td>PLLDFCT_SEL0</td><td>0</td></tr>
<tr><td>DH5</td><td>SLPD1</td><td rowspan="2">PD CONTROL

<table><tr><th>SLPD[1]</th><th>SLPD[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>Control Every 0.5 PLCK at EFM Rising And Falling Edges.</td></tr><tr><td>0</td><td>1</td><td>Control Every 1.0 PLCK at EFM Rising And Falling Edges.</td></tr><tr><td>1</td><td>0</td><td>Control Every 0.5 PLCK at EFM Rising Edge.</td></tr><tr><td>1</td><td>1</td><td>Control Every 1.0 PLCK at EFM Rising Edge.</td></tr></table></td><td>0</td></tr>
<tr><td>DH4</td><td>SLPD0</td><td>0</td></tr>
<tr><td>DH3</td><td>FRAME_SEL1</td><td rowspan="2">FD RLL MAX DETECTION CYCLE

<table><tr><th>FRAME_SEL[1]</th><th>FRAME_SEL[0]</th><th></th></tr><tr><td>0</td><td>0</td><td>OUTPUT FD CONTROL RLL MAX detect data every 64 EFM rising and falling edges.</td></tr><tr><td>0</td><td>1</td><td>OUTPUT FD CONTROL RLL MAX detect data every 128 EFM rising and falling edges.</td></tr><tr><td>1</td><td>0</td><td>OUTPUT FD CONTROL RLL MAX detect data every 256 EFM rising and falling edges. (CD)</td></tr><tr><td>1</td><td>1</td><td>OUTPUT FD CONTROL RLL MAX detect data every 512 EFM rising and falling edges. (DVD)</td></tr></table></td><td>1</td></tr>
<tr><td>DH2</td><td>FRAME_SEL0</td><td>1</td></tr>
<tr><td>DH1</td><td>-</td><td></td><td>x</td></tr>
<tr><td>DH0</td><td>-</td><td></td><td>x</td></tr>
</table>

EFM Asymetry circuit and PLL control command.

SYSTEM COMMAND

B8	FcScmd			
bit	**Name**	**Description**		**def.**
DH7	0			0
DH6	0			0
DH5	0			0
DH4	0			0
DH3	0			0
DH2	0			0
DH1	HWO1		pin MDOUT[1] adaptable	0
DH0	HWO0		pin MDOUT[0] adaptable	0
DL7 : DL0	-			x

general pin output control

B9	SQJcmd			
bit	**Name**	**Description**		**def.**
DH7	JPLY		Current layer status input when it is dual layer.	
		1	LAYER 1	
		0	LAYER 0	
DH6	-			x
DH5	-			x
DH4	-			x
DH3	-			x
DH2	-			x
DH1	-			x
DH0	-			x
DL7 : DL0	-			x

Current layer status input when layer jump has failed.

BA	FLGcmd			
bit	Name	Description		def.
DH7	stp		STOP flag	0
		1	stop .(When MON = L, stop and standby)	
		0	No stop.	
DH6	Fptmg		FOCUS SERVO DROP FLAG	0
		1	FOK	
		0	FLK	
DH5	enMH		Mirr detection when the tracking gain is normal during play.	0
		1	Output tracking input hold during Mirr	
		0	maintain present state	
DH4	HOME		HOME position flag	0
		1	Homming. (Don't use this cmd for direct setting)	
		0	No homming.	
DH3	itvJ		interval jump flag	0
		1	interval jump (Don't use this cmd for direct setting)	
		0	No interval jump	
DH2	TSV		Automatic determination within the program	0
DH1	SSV		Automatic determination within the program	0
DH0	enTJn		TRACK PULL IN when the target number of tracks are reached during track jump	0
		1	yes	
		0	no	

DL7	DFCTed		decided within the program	0
DL6	ATSCed		decided within the program	0
DL5	tbmthd		TRACKING BALANCE	0
		1	BIAS	
		0	BALANCE	
DL4	fbmthd		FOCUS BALANCE	1
		1	BIAS	
		0	BALANCE	
DL3	dsaSQ		SQJump/iDJump related flag	0
		1	Jump once	
		0	Jump repeat until the number of tracks set by dialw is reached.	
DL2	FSend		Pick up standby at this level after focus search	0
		1	FSrng	
		0	Vref	
DL1	enSPi		sled pull in routine use status	0
		1	use	
		0	not used	
DL0	enLOCK		Tracking gain when the lock is dropped	1
		1	up	
		0	normal	

Current servo state.

<table>
<tr><th>BB</th><th colspan="3">SNSCcmd</th></tr>
<tr><th>bit</th><th>Name</th><th colspan="2">Description</th><th>def.</th></tr>
<tr><td>DH7</td><td>RWB</td><td></td><td>Monitor signal read or write</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td>read</td><td></td></tr>
<tr><td></td><td></td><td>0</td><td>write</td><td></td></tr>
<tr><td>DH6</td><td>-</td><td></td><td></td><td>0</td></tr>
<tr><td>DH5</td><td>NORM</td><td colspan="2" rowspan="2">Sense Pin output control bit
<table><tr><th>NORM</th><th>FTLK</th><th></th></tr><tr><td>0</td><td>0</td><td>Normal sense output (READY/BUSY)</td></tr><tr><td>0</td><td>1</td><td>-</td></tr><tr><td>1</td><td>0</td><td>FLKB output</td></tr><tr><td>1</td><td>1</td><td>TLKB output</td></tr></table></td><td>0</td></tr>
<tr><td>DH4</td><td>FTCK</td><td>0</td></tr>
<tr><td>DH3</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH2</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH1</td><td>0</td><td></td><td></td><td>0</td></tr>
<tr><td>DH0</td><td>bank</td><td></td><td>MONITOR RAM BANK</td><td>0</td></tr>
<tr><td>DL7
:
DL0</td><td>MOD[7:0]</td><td></td><td>MONITOR RAM ADDRESS</td><td>0</td></tr>
</table>

Controls the sense pin output and can monitor the ram data in DSSP. The output passes through test dac and sent to the TDAC output. (Monitoring possible for Page 0)

BC	DPRWcmd			
bit	Name	Description		def.
DH7	DD11			
DH6	DD10			
DH5	DD9			
DH4	DD8			
DH3	DD7			
DH2	DD6			
DH1	DD5			
DH0	DD4			
DL7 : DL0	DD[3:0] st6 DPS[2:0]			

DIRECT PORTREAD/WRITE COMMAND.
ST6,DPS2-0 : output port select
¢Ñ DATA input method: Set all DD11~0 DATA 12BIT to 1. Not related to ST6.
Example: "After 1CFFF3 is sent, the STATUS DATA is read.
¢Ñ DATA output method: Selected through the combination of ST6 and DPS2-0
Example: "After 1C100B is sent, 0010 is written to the DSSP CNTbuf.

	ST6	DPS[2]	DPS[1]	DPS[0]	
Input	x	0	0	0	Reads the digital data ,an ADC analog input.
	x	0	0	1	Reads the Free Running Counter Interrupt Vector
	x	0	1	0	-
	x	0	1	1	Reads the status
	x	1	0	0	Reads the hard track counter HCT value.
	x	1	0	1	Reads the data sent by the micom
	x	1	1	0	Reads the command sent by the micom.
	x	1	1	1	-
Output	0	0	0	0	Upper DD[11:2] bit is sent to the focus drive FOD.
	0	0	0	1	Upper DD[11:2] bit is sent to the tracking drive TRD.
	0	0	1	0	Upper DD[11:4] bit is sent to the sled drive SLD.
	0	0	1	1	Upper DD[11:4] bit is sent to the spindle drive SPD.
	0	1	0	0	Upper DD[11:2] bit is sent to the focus gain select register FIG.
	0	1	0	1	Upper DD[11:2] bit is sent to the tracking gain select register TIG.
	0	1	1	0	Upper DD[11:4] bit is sent to he focus balance FBAL
	1	0	0	0	DD[8:0] is sent to the analog select register ASEL
	1	0	0	1	DD[7:0] bit is sent to the interrupt vector register VCT
	1	0	1	0	DD[11:4] bit is sent to the tilt drive TLTD.
	1	0	1	1	The upper 4bit ,'0000', and lower 12 bit, the DD[11:0] bit, of the dssp control register cntbuf16bits, are sent.
	1	1	0	0	Hard ware counter HCT is cleared with '0000h'.
	1	1	0	1	DD[11:00] and '1101' for the upper 12 bits and lower 4 bits, respectively, of the data16 bits are sent to the micom.
	1	1	1	0	DD[11:4] and DD[3:0] * 16 + "1110"are sent to the tracking balance output, TBAL, and depth compensation output, DPCTL, respectively.

BD	FTSTcmd			
bit	**Name**	**Description**		**def.**
DH7	-			x
DH6	-			x
DH5	-			x
DH4	WTF		Tracking filter test	
		1	Tracking filter up test	
		0	Tracking filter normal test	
DH3	-			x
DH2	-			x
DH1	-			x
DH0	WFF		Focus filter test	
		1	Focus filter down test	
		0	Focus filter normal test	
DL7 : DL0	-			x

Test command used to measure the digital servo filter characteristics.
¢Ñ TEALI input becomes the sled filter test input.

BE	RamRcmd			
bit	**Name**	**Description**		**def.**
DH7	NEXT		SRAMÀÇ address becomes +1.	
		1	SRAMÀÇ address becomes the RMD7~RMD0+1.	
		0	SRAMÀÇ address is selected in the RMD7~RMD0 bit.	
DH6	0			0
DH5	0			0
DH4	BANK		Bank Select	
		1		
		0		
DH3	0			0
DH2	0			0
DH1	0			0
DH0	PAGE		Page Select	
		1		
		0		
DL7 : DL0	RMD[7:0]		Assigns the internal SRAM address. The SRAM is composed of pages 0 and 1 and bank0 512 words and bank2 512 words for a total of 1024 words. BANK : BANK 0 and 1 assignment PAGE : PAGE 0 and 1 assignment RMD[7:0]: SRAM address assignment	

This command accesses and directly reads the SRAM, the digital servo internal data.

BF	RamWcmd		
bit	**Name**	**Description**	**def.**
DH7	RD15	.RD15-RD0 : data	
DH6	RD14	-BIT DIRECT ACCES COMMAND	
DH5	RD13	-(EMEc)15 :Transference of the tracking lense brake to the sled.	
DH4	RD12	Address:Ram0 Bank1 02	
DH3	RD11	"0" : No	
DH2	RD10	"1" : Yes	
DH1	RD9	-(HDWc)14 : Use of Mirr or Mirr TZC Latch signal for tracking speed control	
DH0	RD8	Address:Ram0 Bank1 01	
DL7 : DL0	RD[7:0]	"0" : Mirr "1" : Mirr and TZC Latch signal -(HDWc)13 :DFECT HOLD method ADDRESS:Ram0 Bank1 01 "0" : hold signal during defect period "1" : hold using pre-defect hold value	

This command accesses and writes the SRAM, the digital servo internal data.
The SRAM address must be saved beforehand according to RamRcmd(BEh). After the data is set, the address increments by 1 as the data is written.

FILTER COEFFICIENT SETTING COMMAND

Command		DHH				DHL				DL	comment
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7-DL0	
Fxkcmd	C0 : D3	RWB	Fxk14	Fxk13	Fxk12	Fxk11	Fxk10	Fxk9	Fxk8	Fxk7-Fxk0	
SPKxcmd	D4 : D8	RWB	SPk14	SPk13	SPk12	SPk11	SPk10	SPk9	SPk8	SPk7-SPk0	
SRDcmd	D9										
SLKxcmd	DA : DE	RWB	SLk14	SLk13	SLk12	SLk11	SLk10	SLk9	SLk8	SLk7- SLk0	

* You must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

Fxkcmd (Address C0h - D3h)

: Focus Compensation filter coefficient

CxFFFF : Read the (x+1) place coefficient.

Cx<coefficient> : Write the coefficient in the (x+1) Address.

:C0-C7 : Focus normal coefficient setting command.(C0-C7 ↔ K1-K8)

:C8-CF : Focus down coefficient setting command.(C8-CF ↔ K1-K8)

:D0-D1 : Focus normal coefficient setting command.(D0 ↔ K0, D1 ↔ nsk)

:D2-D3 : Focus down coefficient setting command.(D2 ↔ K0, D3 ↔ nsk)

SPKxcmd (Address D4h - D8h)

: Spindle Compensation filter coefficient.

: D4-D7 : Spindle coefficient setting command.(D4 ↔ Ka, D5 ↔ K1,D6 ↔Kb , D7 ↔ K2)

: D8 : Spindle output gain setting command(D8 ↔ nsk)

SRDcmd (Address D9h)

: Servo read address.

SLKxcmd (Address DAh - DEh)

:DA-DD : Sled coefficient setting command.(DA ↔ Ka, DB ↔ K1,DC ↔ Kb, DD ↔ K2)

:DE : Sled output gain setting command(DE ↔ nsk)

PLLcmd (Address DFh)

: Digital servo PLL control command.

Command		DHH				DHL				comment
Name	code	DH31	DH30	DH29	DH28	DH27	DH26	DH25	DH24	
PLLcmd	DF	IDACN[5:0]							SHIFT_G	
		DL23	DL22	DL21	DL20	DL19	DL18	DL7	DL6	
		IDACP[5:0]						PLOCKSL	IS_UP	
		DL15	DL14	DL13	DL12	DL11	DL10	DL9	DL8	
		RARR[2:0]			VARI_G[2:0]				VCOSL	
		DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	
		PWM[7:0]								

* You must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

: IDACN[5:0] : CHARGE PUMP down current setting
In = (Vdd-Vrpd)/Rpd X (n+1), n is the register value (Decimal)
08h is recommended

: SHIFT_G : VCO GAIN shift enable bit
"1" : fixed bias(2.0V) (recommended)
"0" : enable

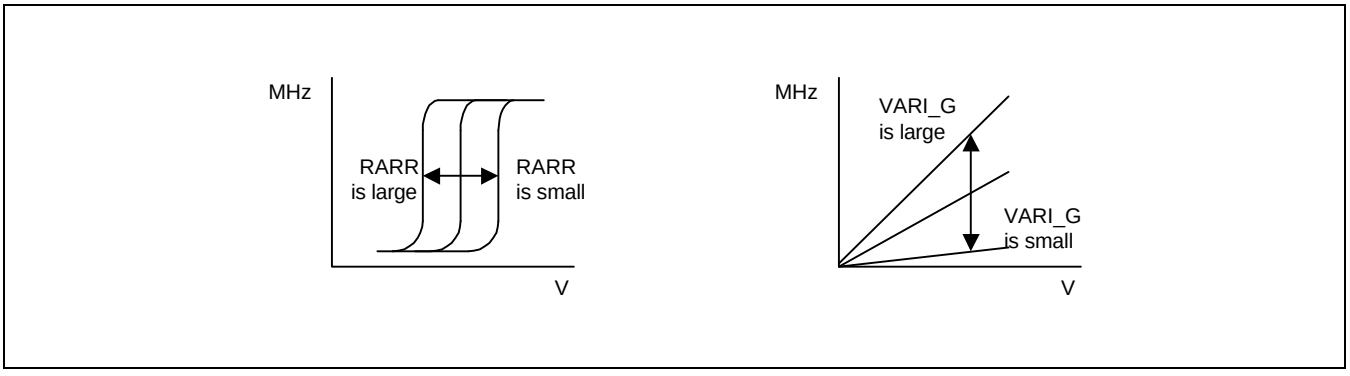
: IDACP[5:0] : CHARGE PUMP up current setting
In=(Vdd-Vrpd)/Rpd X (n+1), n is the register value (Decimal)
08h is recommended

: PLOCKSL : PD/FD control
"1" : PLL_CLOCK + CLV_LOCK reference
"0" : PLL_LOCK reference (recommended)

: IS_UP : Analog test mode(charge pump) current direction setting (Test mode only)
"1" : UP current measurement
"0" : DOWN current measurement

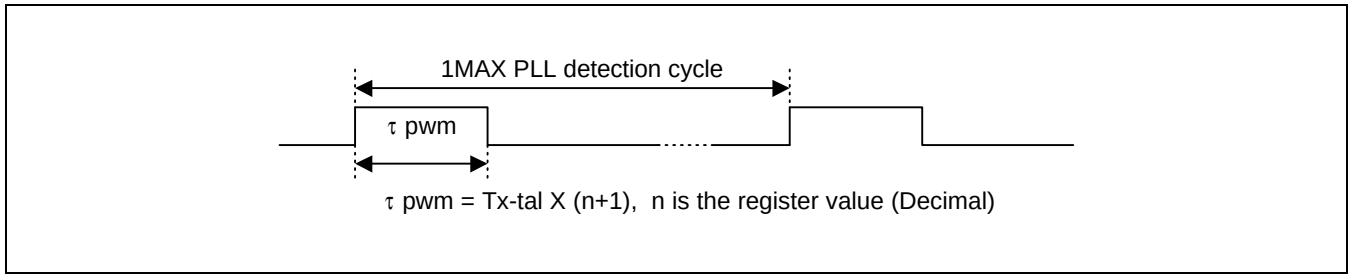
: RARR[2:0] : Gain band-width shift amount setting when the VCO gain shift has been enabled

: VARI_G[2:0] : VCO gain setting



: VCOSL : VCO select
"1" : external VCO(clock input to VCOCKEX)
"0" : internal VCO(recommended)

:PWM[7:0] : FD gain setting
40h is recommended



Txkcmd (Address E0h - F3h)

: Tracking Compensation filter coefficient setting.

Command		DHH				DHL				DL	comment
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7-DL0**	
Txkcmd	E0 : EF	RWB	THk14	THk13	THk12	THk11	THk10	THk9	THk8	THk7-THk0	
	F1 : F3	RWB	TLK14	TLk13	TLk12	TLk11	TLk10	TLk9	TLk8	TLk7- TLk0	

* You must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.
: E0-E7 : Tracking normal coefficient setting command.(E0-E7 ↔ K1-K8)
: E8-EF : Tracking down coefficient setting command.(E8-EF ↔ K1-K8)
: F0-F1 : Tracking normal coefficient setting command.(F0 ↔ K0, F1 ↔ nsk)
: F2-F3 : Tracking down coefficient setting command.(F2 ↔ K0, F3 ↔ nsk)

MNIcmd (Address F4h)

:Defect select and Monitor command

Command		DHH				DHL				DL	comment
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7-DL0	
MNIcmd	F4	MNI1	MNI0	CSEL	DSEL	DCUT[3:0]					
Reset value											

* You must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

: MNI1-0 :Change the monitor signal according to each bit.
- 00 : EFMRTD PLCK PLLLOCK
- 01 : TLKB FLKB COUT
- 10 : INT0_224
- 11 : EFMRTD PLCK PLLLOCK

: CSEL : C-PEAK use status control bit.
- 1 :'OR' operated on C-peak and servo defect and result used.
- 0 : C-PEAK not used.

: DSEL : DEFECT length control bit.
- 1 : DEFECT length is controlled according to DCUT[3:0].
- 0 : DEFECT length is not controlled.

: DCUT[3:0]: DEFECT length limit bit(use when DSEL = 1).

0000 : 0.8ms	0100 : 1.2ms	1000 : 1.6ms	1100 : 2.0ms
0001 : 0.9ms	0101 : 1.3ms	1001 : 1.7ms	1101 : 2.1ms
0010 : 1.0ms	0110 : 1.4ms	1010 : 1.8ms	1110 : 2.2ms
0011 : 1.1ms	0111 : 1.5ms	1011 : 1.9ms	1111 : 2.3ms

ASKxcmd (Address F5h - F6h)

Command		DHH				DHL				DL	comment
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7-DL0	
ASKxcmd	F5	RWB	AHK 14	AHk 13	AHk 12	AHk 11	AHk 10	AHk 9	AHk 8	AHk7 - ALk0	
	F6	RWB	ALK 14	ALk 13	ALk 12	ALk 11	ALk 10	ALk 9	ALk 8	AHk7- ALk0	
Reset value											

* You Must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

: F5 : Anti shock coefficient setting command.(F5 ↔ K1)
: F6 : Anti shock output gain setting command(F6 ↔ K)

EVAcmd (Address F7h) : Reserved.

: EVA chip up-load and down-load control command.

Command		DHH				DHL				DL	comment
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7-DL0**	
EVAcmd	F7	UP	DOWN								
Reset value											

* You Must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

: UP,DOWN : EVA chip up-load and down-load control .
00 : normal mode
01 : down-load mode
10 : up-load mode
11 : normal mode

TTKxcmd (Address F8h - FAh)

Command		DHH				DHL				DL	comment
Name	**code**	**DH7**	**DH6**	**DH5**	**DH4**	**DH3**	**DH2**	**DH1**	**DH0**	**DL7-DL0**	
TTKxcmd	F8 : FA	RWB	TTK 14	TTk 13	TTk 12	TTk 11	TTk 10	TTk 9	TTk 8	TTk7 - TTk0	
Reset value											

* You Must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.
: F8-F9 : Tilt filter coefficient setting command.(F8 ↔ K0, F9 ↔ K1)
: FA : Tilt filter output gain setting command(FA ↔ nsk)

FTGcmd (Address FBh)

:MANUAL Focus Tracking gain control command

Command		DHH				DHL				DL	comment
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7-DL0	
FTGcmd	FB	Fchg	DWN	Tchg	UP						
Reset value											

* You Must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

: Fchg : Focus gain change status.
"1" : change
"0" : no change

: DWN : Focus gain
"1" : Down
"0" : Normal

: Tchg : Tracking gain change status
"1" : change
"0" : no change

: UP : Focus gain
"1" : Up
"0" : Normal

AVkcmd (Address FCh)

:Average Filter coefficient.

Command		DHH				DHL				DL	comment
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7-DL0	
AVkcmd	FC	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4-AD0 AVS2-AVS0	
Reset value											

* You Must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

WHEN DATA READ,
CMD FFF AVS2-0 (AD0 = high)
: AVS2-0 : RAM SELECT bit to be set
: AD12-0 : WRITE DATA

AVS2-0	Parameter Name	CONTENTS	RAM Address (K,K0)
0h	offset	Focus, Tracking offset average coefficient	03d
1h	To_avrg	Tracking output average coefficient	03f
2h	Favrg	Focus input average coefficient	06d
3h	Tavrg	Tracking input average coefficient	06f
4h	SLavrg	Sled output average coefficient	07f
5h	ENVavrg	RF envelope average coefficient	01d
6h	VREFavrg	Reference Voltage average coefficient	01f
7h	K1,K2	Gain Band Pass Filter K1 and K2(same) K0 = 1-K1	

xGkxcmd (Address FDh - FFh)

:Loop gain band pass filter coefficient setting command.

Command		DHH				DHL				DL	comment
Name	code	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	DL7-DL0	
xGkxcmd	FD : FF	RWB	GK14	Gk13	Gk12	Gk11	Gk10	Gk9	Gk8	Gk7 ~ Gk0	
Reset value											

* You Must first select this filter's coefficient using the SPDcmd(ABh) command before selecting other speed-related components.

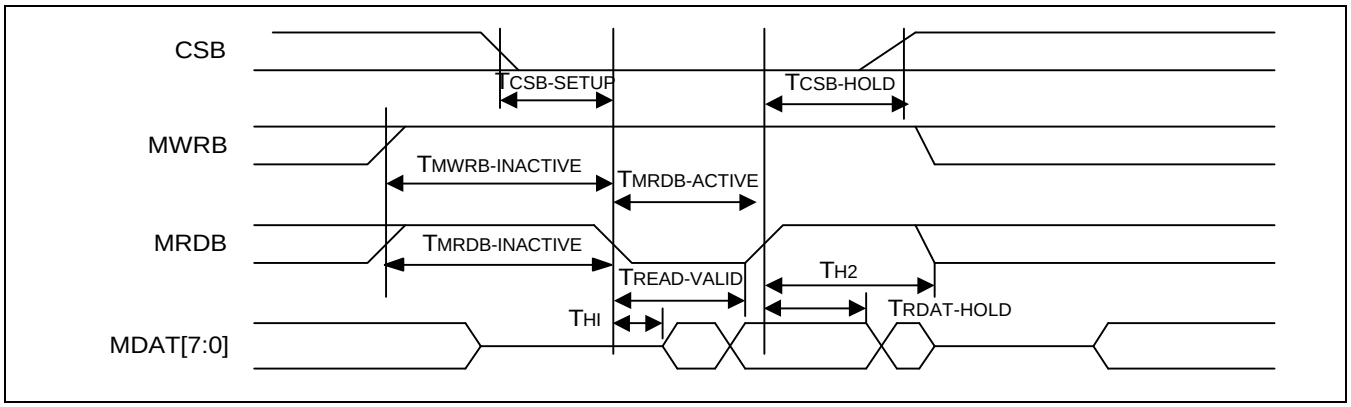
: FD : Input Attenuater.(FD ↔ K0)
: FE : Pole Point(FE ↔ K1)
: FF : Pole Point(FF ↔ K2)

INTERFACE TIMING SPEC

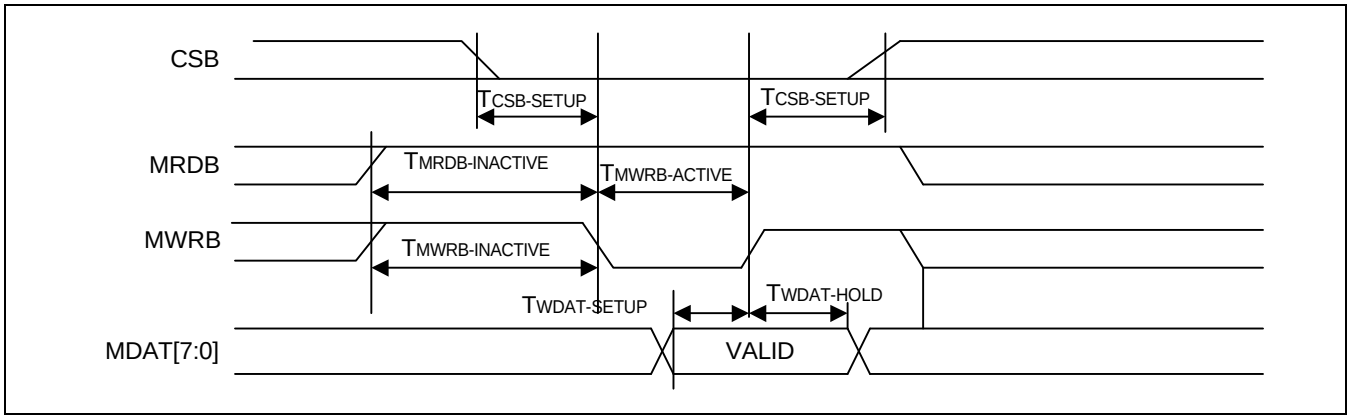
Micom I/F Timing Spec

Time	Description	Min	Max	unit
$T_{CSB-SETUP}$	CSB SETUP	10		ns
$T_{CSB-HOLD}$	CSB HOLD	10		ns
$T_{MWRB-INACTIVE}$	MWRB INACTIVE	30		ns
$T_{MWRB-ACTIVE}$	MWRB ACTIVE PULSE WIDTH	30		ns
$T_{MRDB-INACTIVE}$	MRDB INACTIVE	30		ns
$T_{MRDB-ACTIVE}$	MRDB ACTIVE PULSE WIDTH	120		ns
$T_{READ-VALID}$	MRDB ACTIVE TO READ DATA VALID		60	ns
T_{H1}	MRDB ACTIVE TO MDATA[7:0] LOW-IMPEDANCE	-		ns
T_{H2}	MRDB INACTIVE TO MDAT[7:0] HIGH-IMPEDANCE	-	-	ns
$T_{RDAT-HOLD}$	READ DATA HOLD AFTER MRDB INACTIVE	10		ns
$T_{WDAT-SETUP}$	WRITE DATA SETUP	20		ns
$T_{WDAT-HOLD}$	WRITE DATA HOLD	10		ns

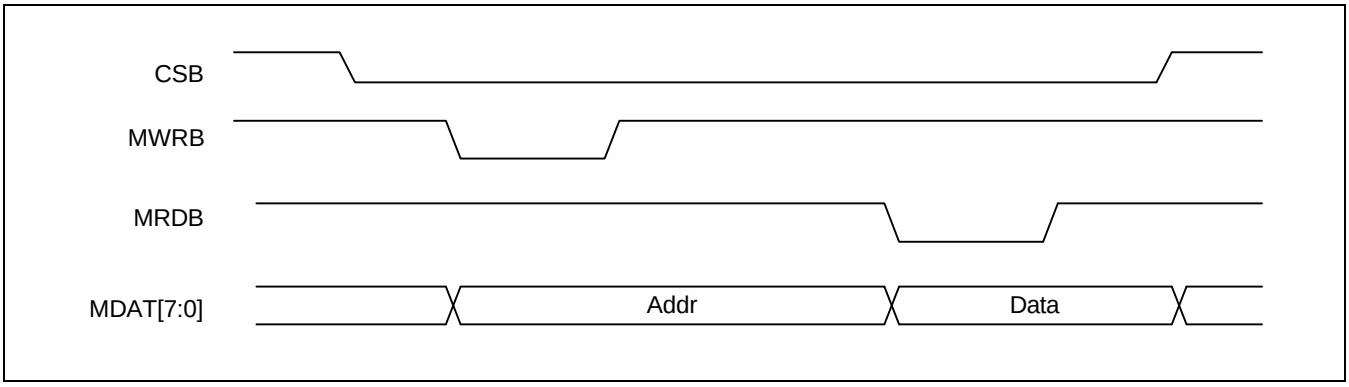
— Read Cycle



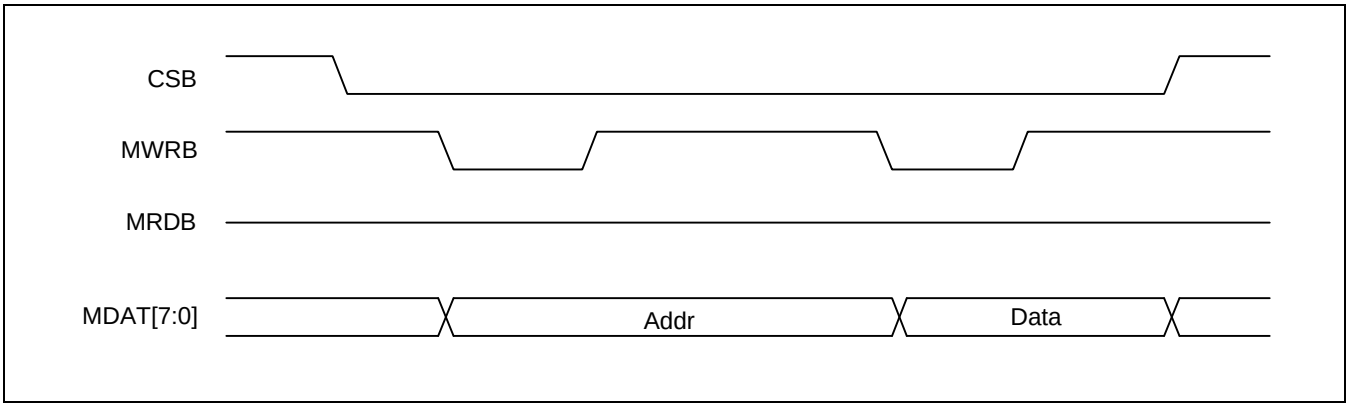
— Write Cycle



— Read Cycle

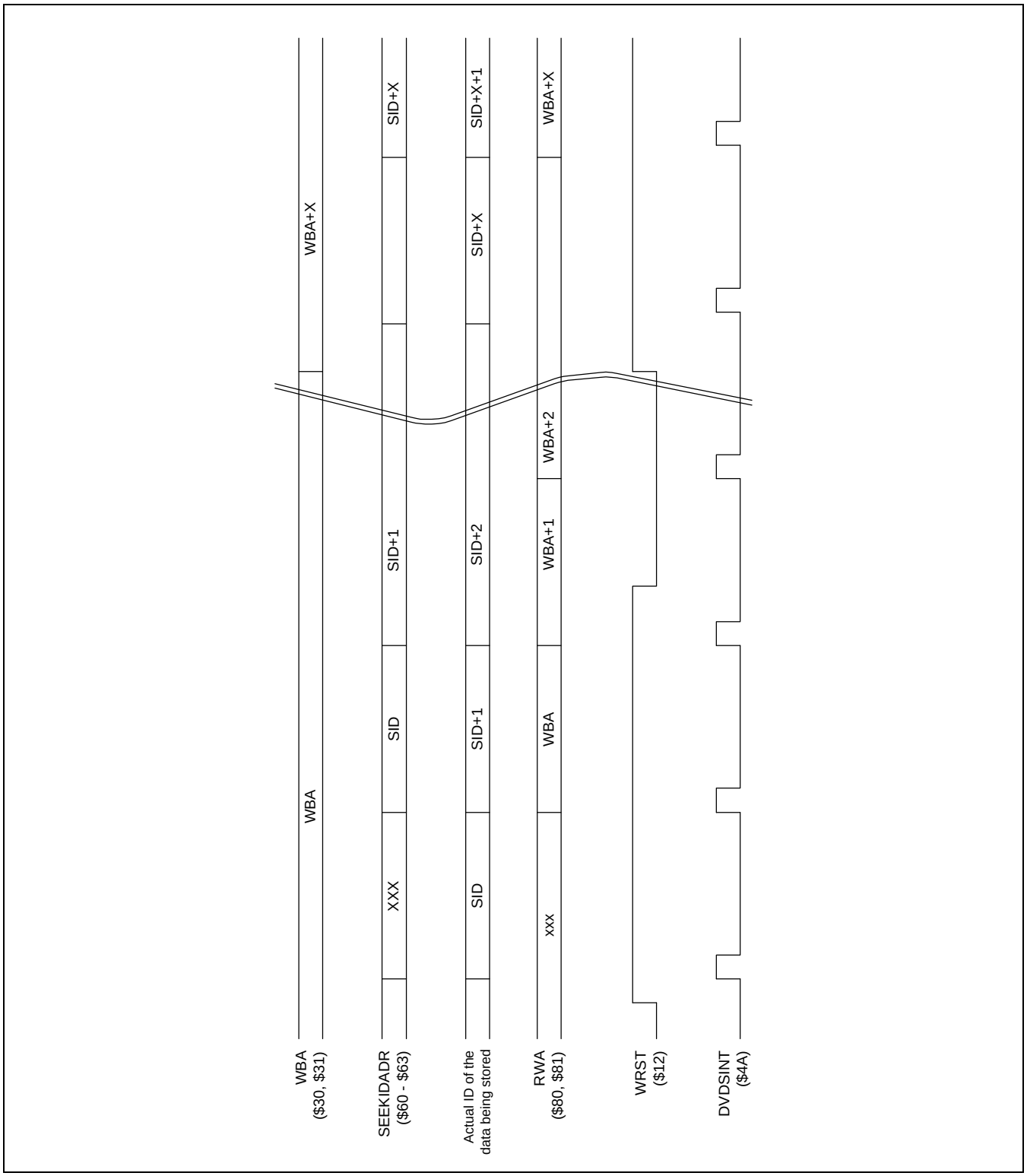


— Write Cycle



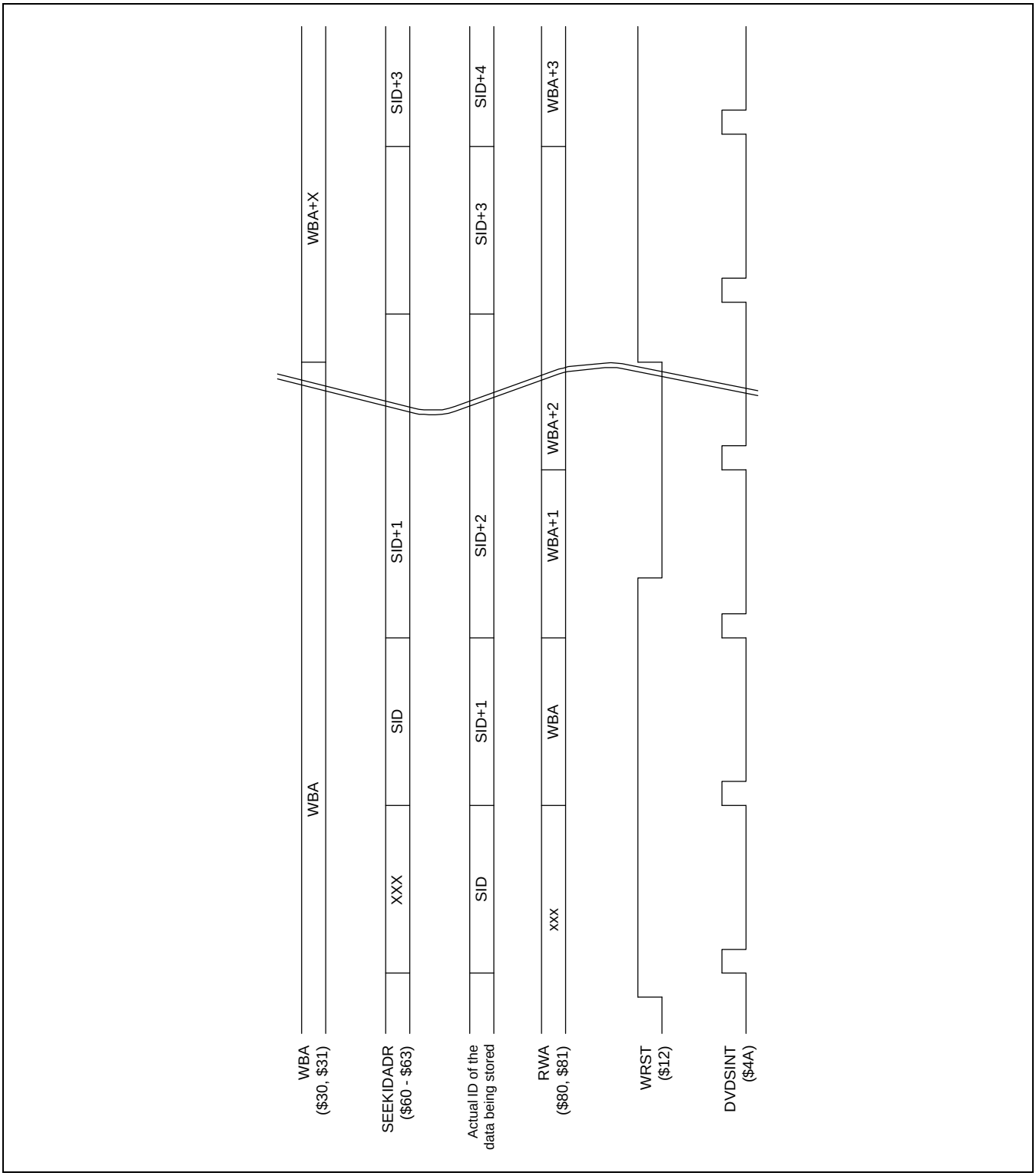
Buffer Write

1) During Re-search or Jump Control
— Set WRST out of write to "0", reassign the memory address to WBA, and write.



Buffer Write

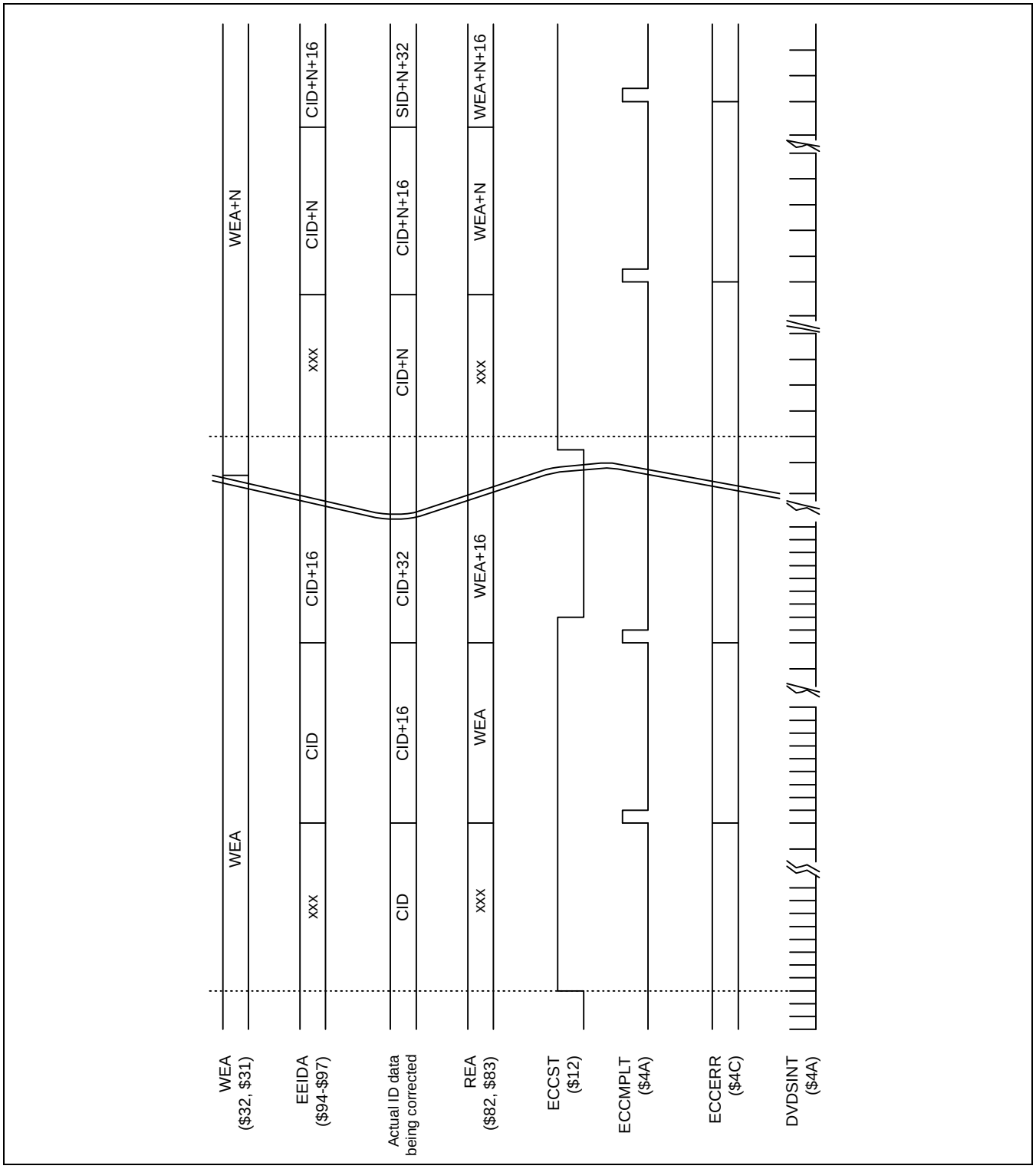
2) Write according to the over or under interrupt.
— Only controls WRST. It controls write stop and start functions, and does not reload the write location in WBA.



ECC Control

— If ECCST is set to 0 during ECC, the next ECC address to be executed must be saved in WEA.

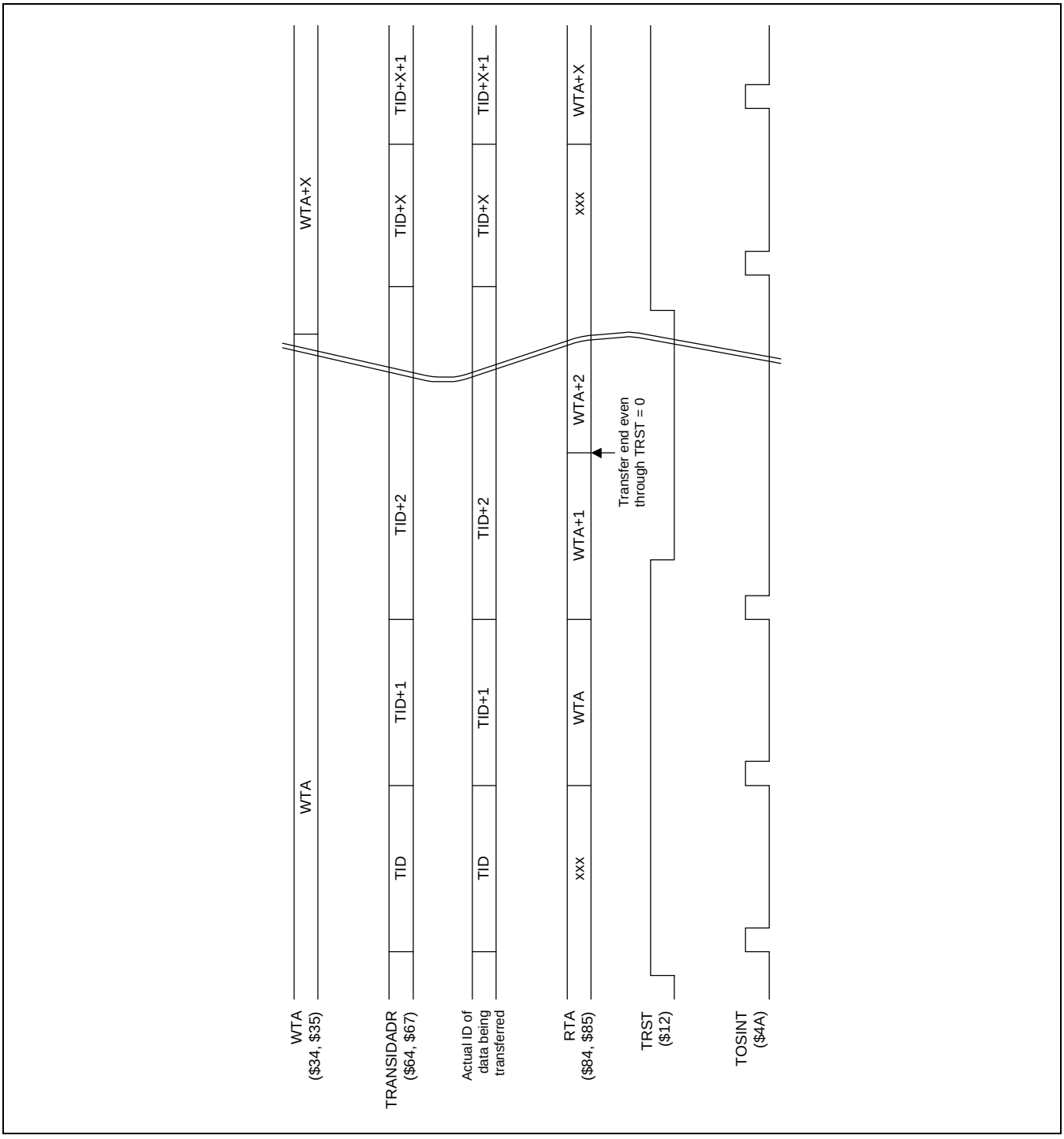
— If ECCST is set 0, the current ECC stops.



Transfer Control

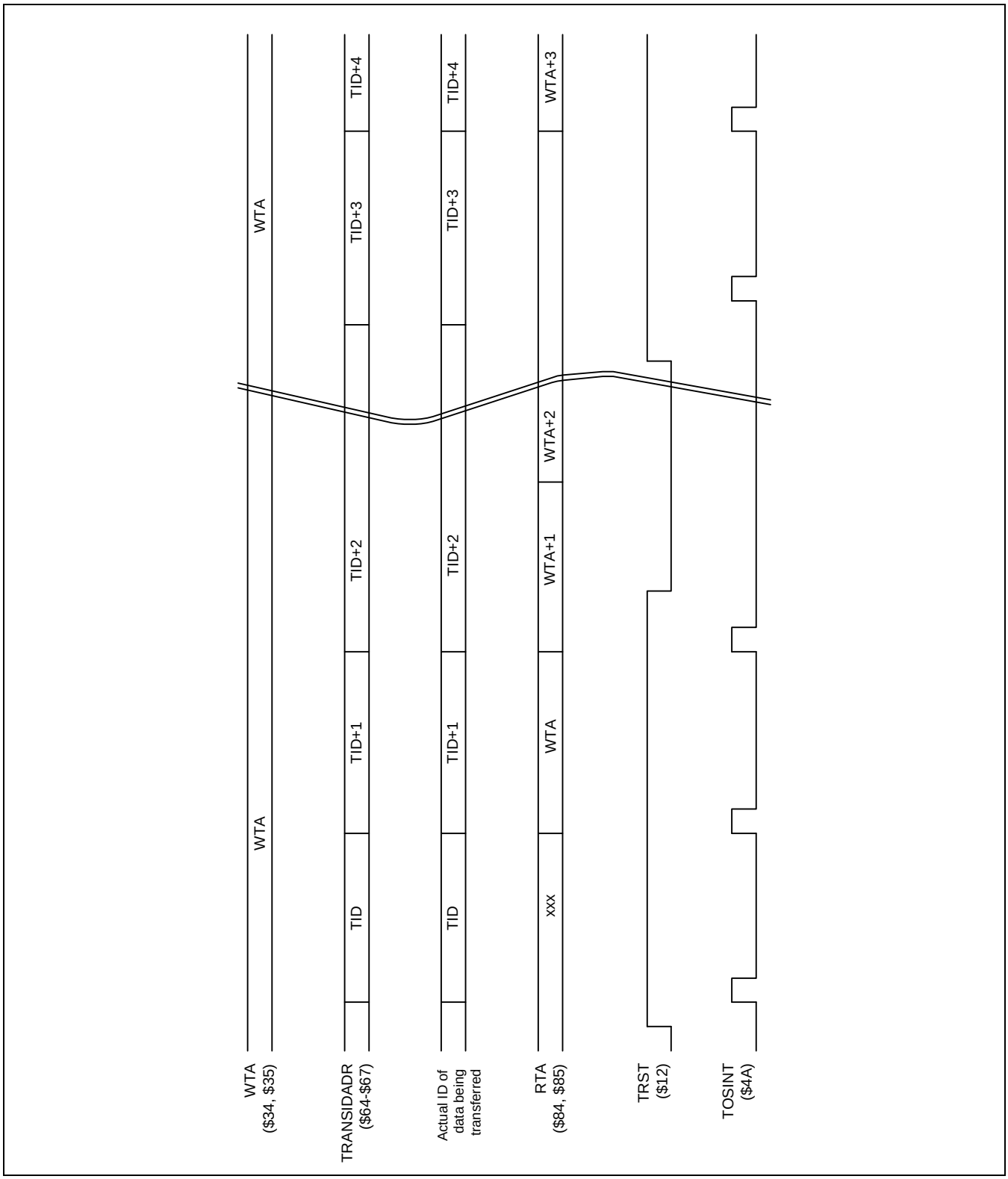
1.Transfer after reassigning the memory address to be sent

— After setting TRST to 0 and reassigning the new address in WTA, start transfer by setting TRST to 1.
* Tough TRST is set to 0, it must be reassigned after transferring the amount of assigned sectors)
* Example below illustrate a case where the transfer sector number has been set to 1.

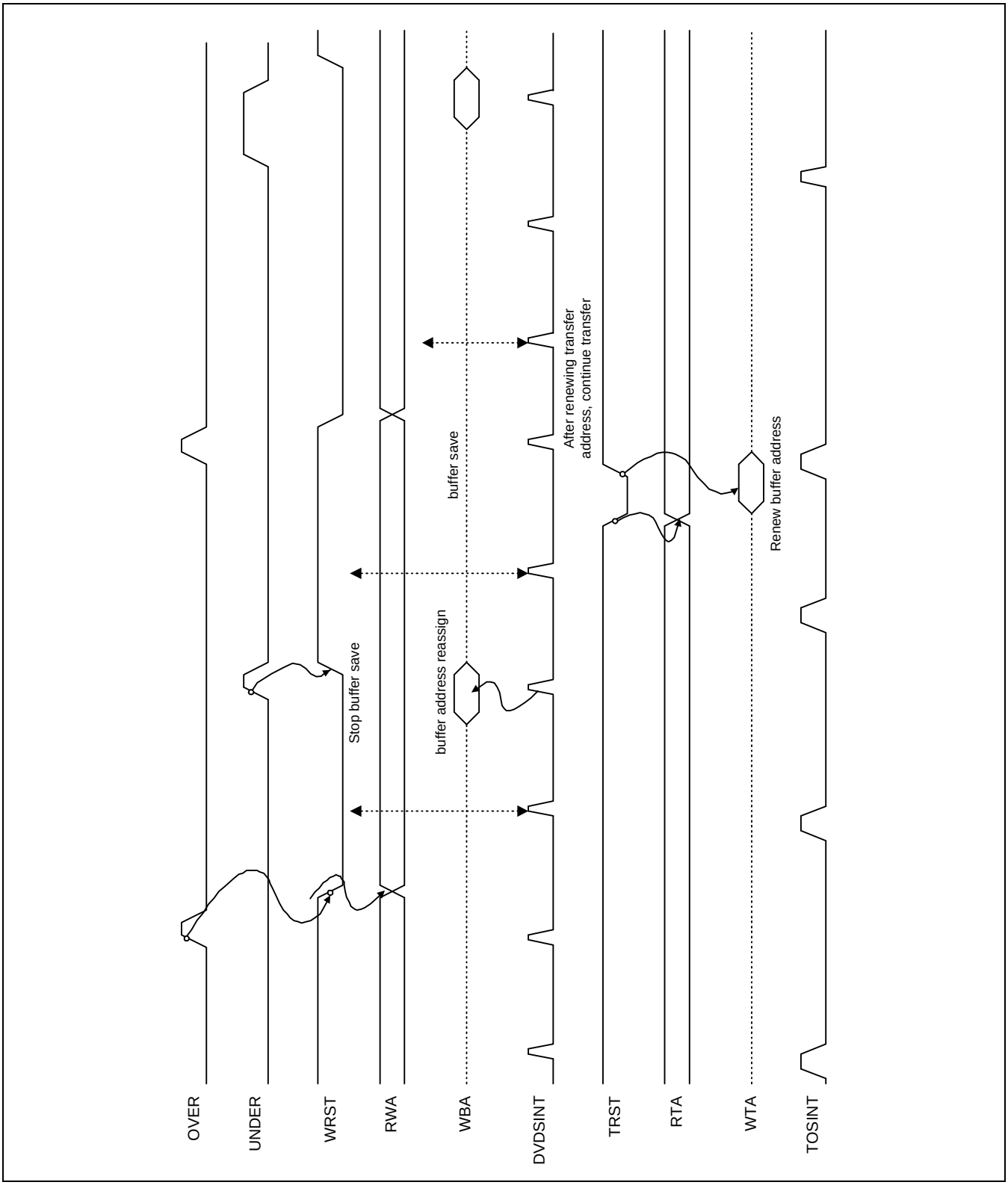


Transfer Control

2. Transfer stop and start through only TRST control

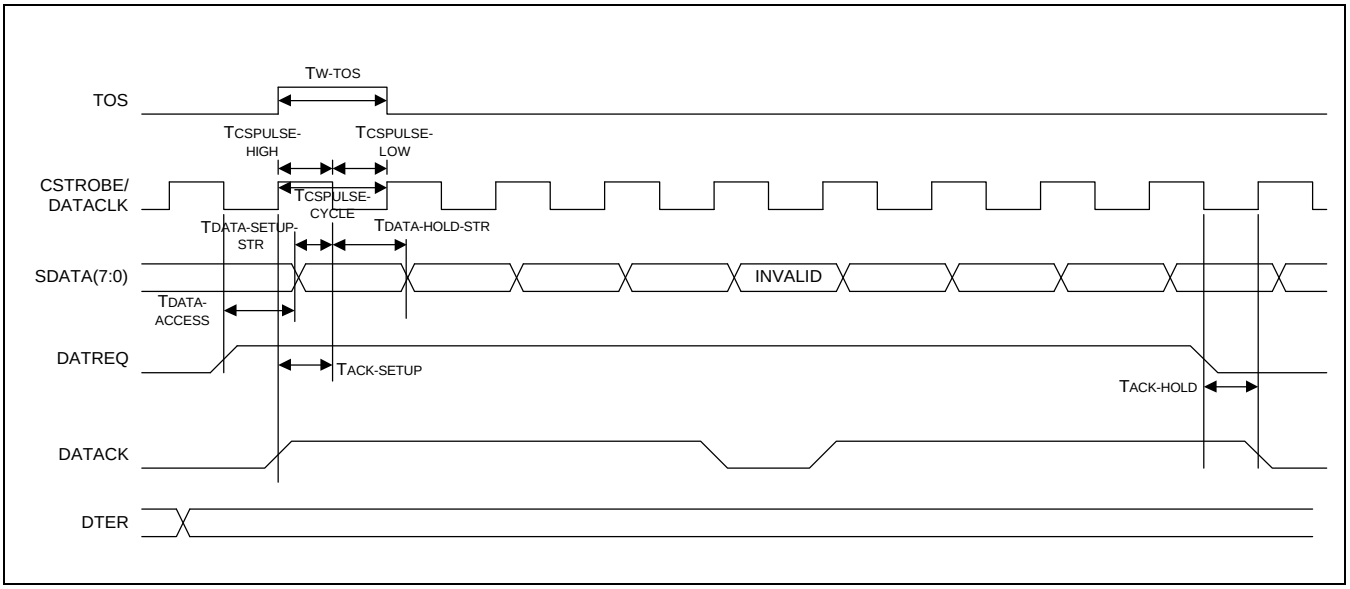


Over and Under interrupt ($4A)



AV Decoder I/F

:Burst out mode (DVD-P I/F) Synchronous, samsung multi, synyo)



MODE 1: 2048 Bytes main data only -> $T_{DATA\ ACCESS}$ is delayed more than mode 2 by about T.

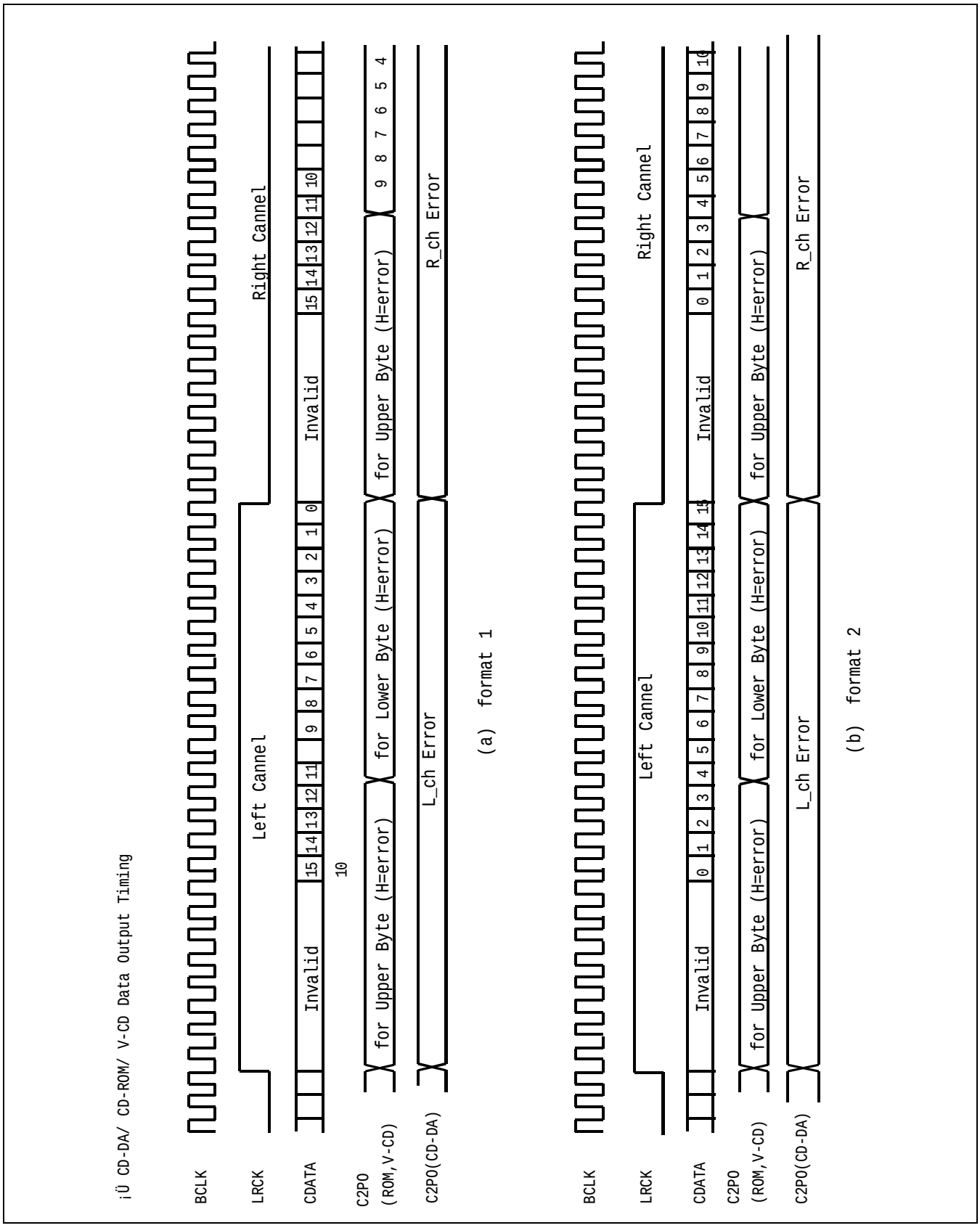
MODE 2: 2064 Bytes data in a sector
(4bytes ID + 2 Bytes IEC + 6 Bytes RSV + 2048 Bytes main data + 4 bytes EDC)

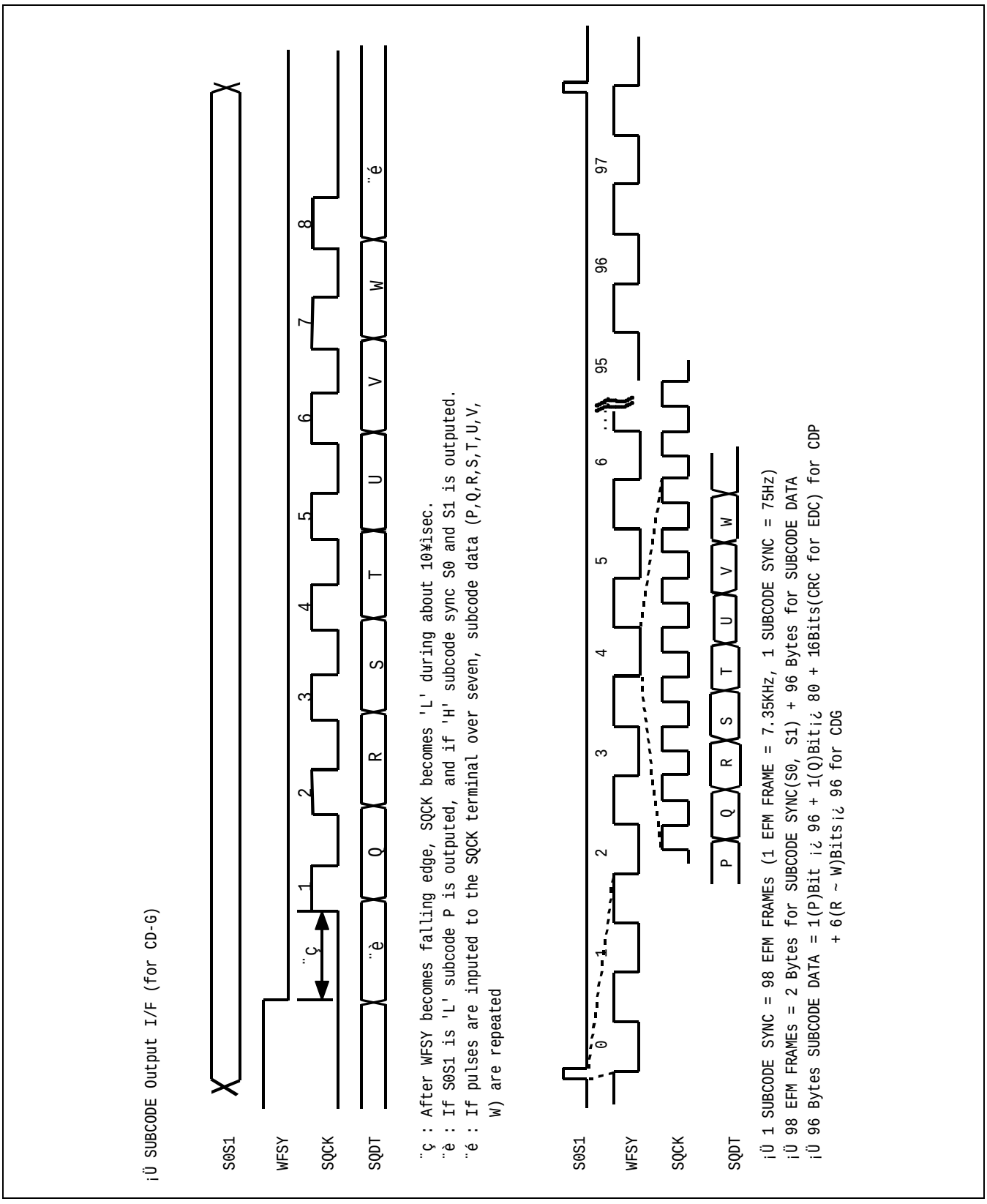
- The DTER signal is output in units of sector.
- Data is taken at CSTROBE/DATACLK's falling edge (rising edge in reverse mode).
- CSTROBE/DATACLK's duty cycle is not regular.
- TCSPULSE-HIGH/LOW: 4T
- TCSPULSE-CYCLE: 8T (240 ns)
- CSTROBE, DATREQ, DATACK's edge is programmable (reversible).

<AV Decoder I/F Timing Spec>

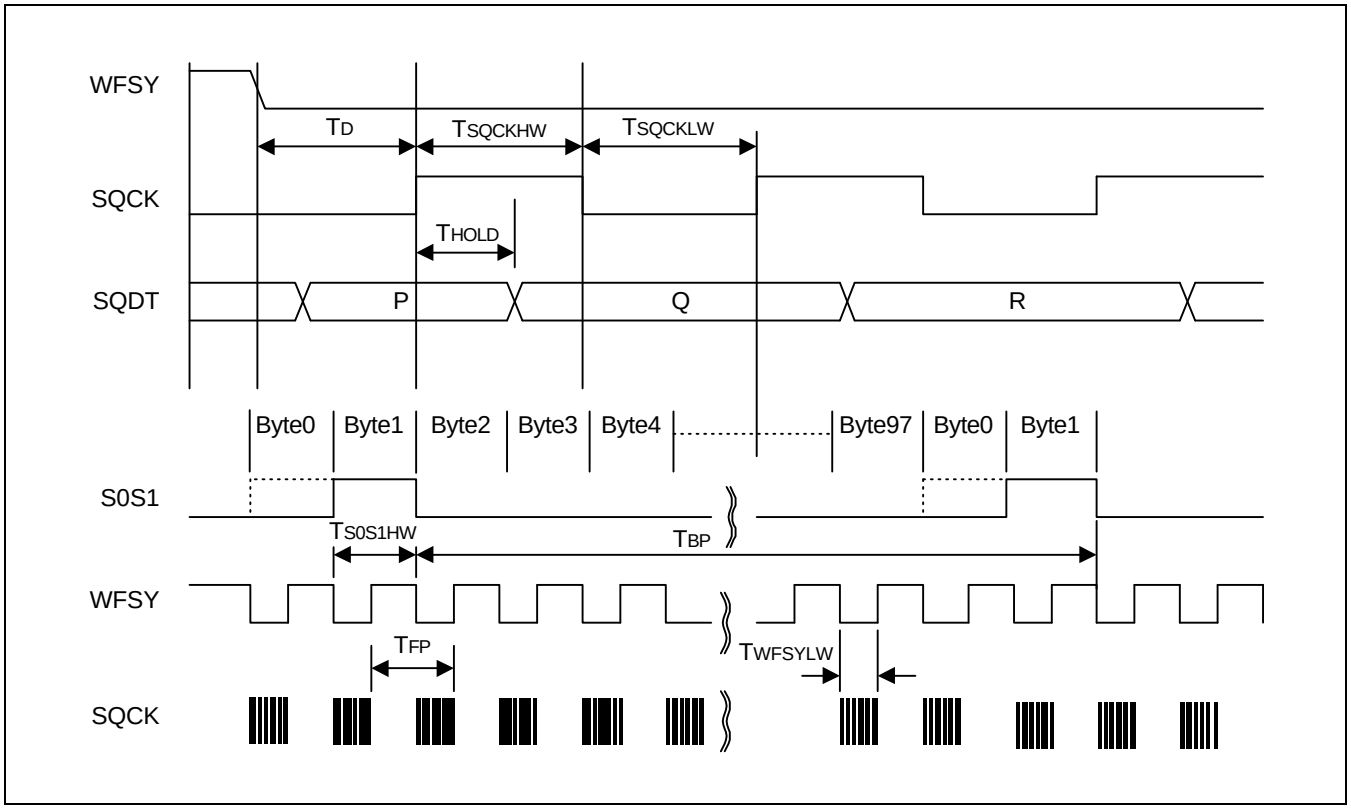
Time	Description	Min	Max	unit
$T_{DATA-SETUP-STR}$	SDATA(7:0) SETUP TO CSTROBE ASSERTED (SYNCHRONOUS)	5		ns
$T_{SDATA-D}$	SDATA(7:0) HOLD FROM CSTROBE ASSERTED (SYNCHRONOUS)	5		ns
T_D	DELAY FROM DATREQ ASSERTED TO DATACK (ASYNCHRONOUS)	0		ns
$T_{ACK-LOW}$	DATACK LOW TIME (ASYNCHRONOUS)	50		ns
T_{ACK-P}	DATACK PERIOD	75		ns
$T_{ACK-DIS}$	DATACK DISABLED TIME	12		ns
$T_{SDATA-D}$	SDATA(7:0) DELAY FROM DATACK FALLING		10	ns
$T_{ACK-SETUP}$	DATACK SETUP TO CSTROBE (SYNCHRONOUS)	5		ns
$T_{ACK-HOLD}$	DATACK HOLD FROM CSTROBE (SYNCHRONOUS)	5		ns

DVD-P Asynchronous I/F Mode and DVD-ROM I/F(SAMSUNG,SYNYO) are deleted.


¡Ü CD-DA/ CD-ROM/ V-CD Data Output Timing
BCLK
LRCK
Left Cannel
Right Cannel
CDATA
Invalid
15 14 13 12 11 9 8 7 6 5 4 3 2 1 0
Invalid
15 14 13 12 11 10
10
C2PO (ROM,V-CD)
for Upper Byte (H=error)
for Lower Byte (H=error)
for Upper Byte (H=error)
9 8 7 6 5 4
C2PO(CD-DA)
L_ch Error
R_ch Error
(a) format 1
BCLK
LRCK
Left Cannel
Right Cannel
CDATA
Invalid
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Invalid
0 1 2 3 4 5 6 7 8 9 10
C2PO (ROM,V-CD)
for Upper Byte (H=error)
for Lower Byte (H=error)
for Upper Byte (H=error)
C2PO(CD-DA)
L_ch Error
R_ch Error
(b) format 2


¡Ü SUBCODE Output I/F (for CD-G)
S0S1
WFSY
SQCK
SQDT
¨ç
¨è
¨é
Q
R
S
T
U
V
W
1
2
3
4
5
6
7
8
¨ç : After WFSY becomes falling edge, SQCK becomes 'L' during about 10¥isec.
¨è : If S0S1 is 'L' subcode P is outputed, and if 'H' subcode sync S0 and S1 is outputed.
¨é : If pulses are inputed to the SQCK terminal over seven, subcode data (P,Q,R,S,T,U,V,
W) are repeated
S0S1
WFSY
SQCK
SQDT
0
1
2
3
4
5
6
95
96
97
P
Q
R
S
T
U
V
W
¡Ü 1 SUBCODE SYNC = 98 EFM FRAMES (1 EFM FRAME = 7.35KHz, 1 SUBCODE SYNC = 75Hz)
¡Ü 98 EFM FRAMES = 2 Bytes for SUBCODE SYNC(S0, S1) + 96 Bytes for SUBCODE DATA
¡Ü 96 Bytes SUBCODE DATA = 1(P)Bit ¡¿ 96 + 1(Q)Bit¡¿ 80 + 16Bits(CRC for EDC) for CDP
+ 6(R ~ W)Bits¡¿ 96 for CDG

SUBCODE Output I/F (for CD-G)



Time	Description	Min	Typ	Max	UNIT
T_D	Delay Time from WFSY Low to SQCK High edge for "P" Subcode bit(SQCK input)	1	-	-	us
T_{SQCKHW}	SQCK(input) High Pulse Width	1	-	3	us
T_{SQCKLW}	SQCK(input) Low pulse Width	1	-	3	us
T_{HOLD}	SQDT Hold Time from SQCK High	0	-	-	ns
T_{S0S1HW}	S0S1 High Pulse Width	-	136	-	us
T_{BP}	Block Period	-	13	-	ms
T_{FP}	Frame Period	-	136	-	us
T_{WFSYLW}	WFSY Low Pulse Width	-	68	-	us

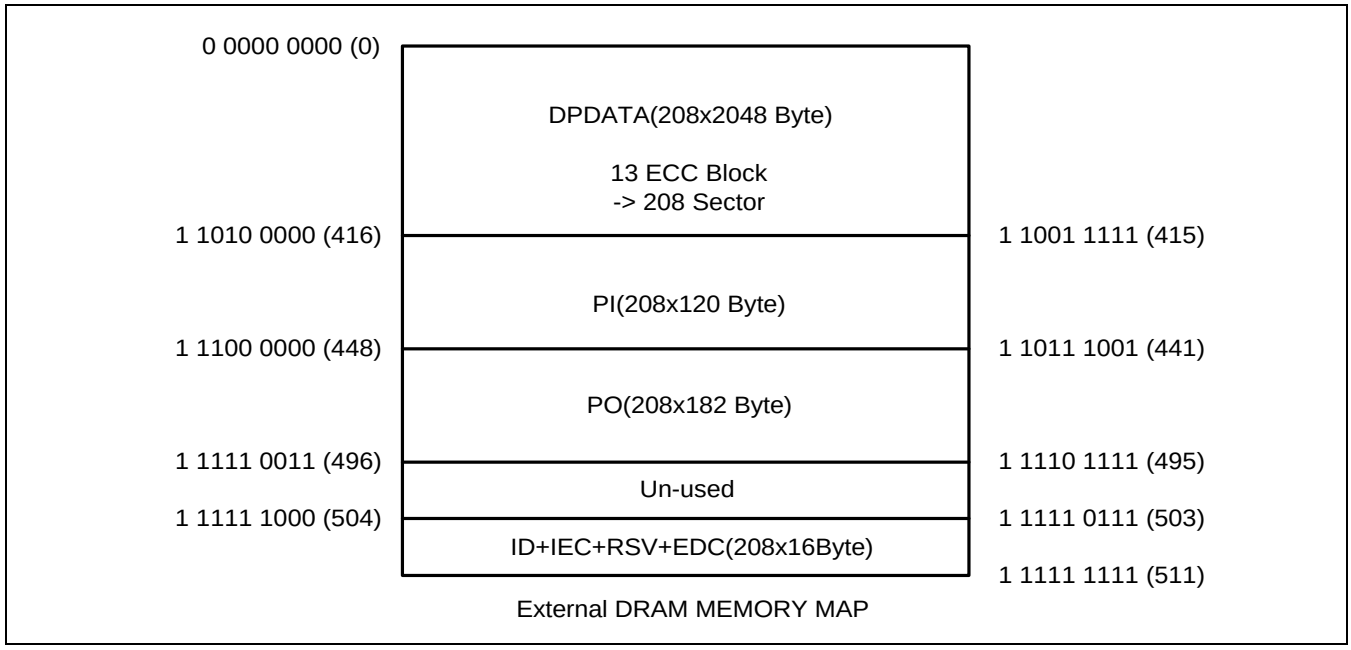
¡Ø SQDT read completion in wfsy low period (T_{WFSYLW}).

EXTERNAL DRAM MEMORY MAP

ECC 13 blocks can be saved using 4M DRAM. EFM+demodulated 1 block, ECC 1 block, DESCRAMBLE 1 block and TRANS 1 block are executed successively.

: DVDP Memory Mapping (512x512x16)

¢¡ 1 Sector base : ID(4),IEC(2),RSV(6),DPDATA(2048),EDC(4),PI(120),PO(182)



External DRAM MEMORY MAP

Sector Memory Mapping Defined

1) PI : 128 Bytes are assigned per sector.
   ⇒ 1 Row Address increments per 8 sectors.
2) PO :256 Bytes are assigned per sector.
   ⇒ 1 Row Address increments per 4 sectors.
3) ID,IEC,RSV,EDC : 32 Bytes are assigned per sector.
   ⇒ 1 Row Address increments per 32 sectors.

1) Data Mapping

ECC Block Number	ID Sector Number	Row Address									Column Address									
0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x
	1	0	0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x
	:	:									:									
	15	0	0	0	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x
1	0-15	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
2	0-15	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
:	:	:									:									
12	0	1	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x
	:	:									:									
	15	1	1	0	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x

2) PI Mapping

ECC Block Number	ID Sector Number	Row Address									Column Address								
0	0	1	1	0	1	0	0	0	0	0	0	0	0	x	x	x	x	x	x
	1	1	1	0	1	0	0	0	0	0	0	0	1	x	x	x	x	x	x
	:	:									:								
	15	1	1	0	1	0	0	0	0	1	1	1	1	x	x	x	x	x	x
1	0-15	1	1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x
2	0-15	1	1	0	1	0	0	1	0	x	x	x	x	x	x	x	x	x	x
:	:	:									:								
12	0	1	1	0	1	1	1	0	0	0	0	0	0	x	x	x	x	x	x
	:	:									:								
	15	1	1	0	1	1	1	0	0	1	1	1	1	x	x	x	x	x	x

3) PO Mapping

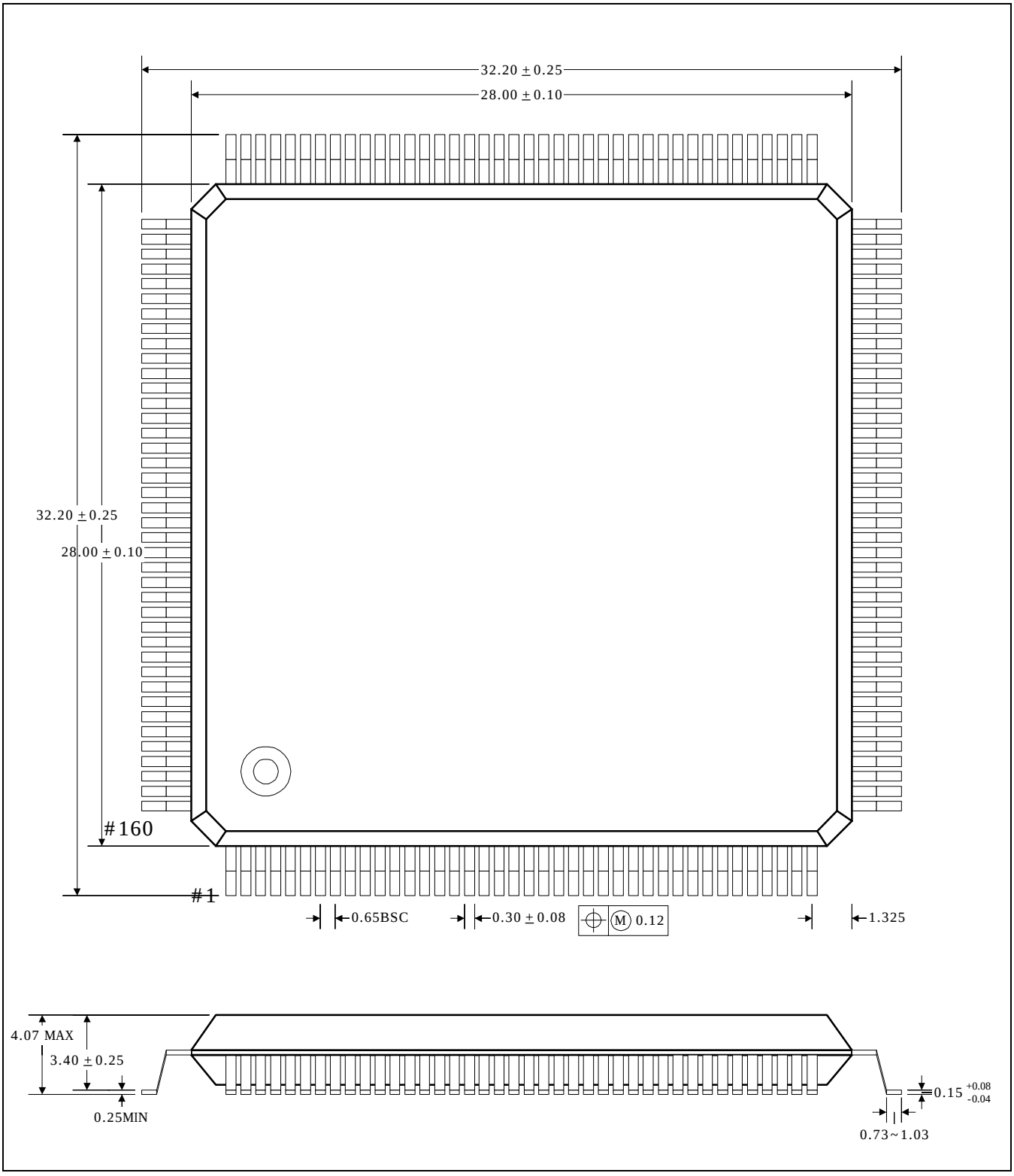
ECC Block Number	ID Sector Number	Row Address									Column Address								
0	0	1	1	1	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x
	1	1	1	1	0	0	0	0	0	0	0	1	x	x	x	x	x	x	x
	:	:									:								
	15	1	1	1	0	0	0	0	1	1	1	1	x	x	x	x	x	x	x
1	0-15	1	1	1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x
2	0-15	1	1	1	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x
:	:	:									:								
12	0	1	1	1	1	1	0	0	0	0	0	0	x	x	x	x	x	x	x
	:	:									:								
	15	1	1	1	1	1	0	0	1	1	1	1	x	x	x	x	x	x	x

4) ID(4) + IEC(2) + RSV(6) + EDC(4)

ECC Block Number	ID Sector Number	Row Address									Column Address								
0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	x	x	x	x
	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	x	x	x	x
	:	:									:								
	15	1	1	1	1	1	1	0	0	0	0	1	1	1	1	x	x	x	x
1	0-15	1	1	1	1	1	1	0	0	0	1	x	x	x	x	x	x	x	x
2	0-15	1	1	1	1	1	1	0	0	1	0	x	x	x	x	x	x	x	x
:	:	:									:								
12	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	x	x	x	x
	:	:									:								
	15	1	1	1	1	1	1	1	1	0	0	1	1	1	1	x	x	x	x

* 4 lower 4Bit Sector Mapping
→ ID:¡®0000¡¯-¡®0001¡¯, IEC:¡®0010¡¯, RSV:¡®0011¡¯-¡®0110¡¯, EDC:¡®1000¡¯-¡®1001¡¯

PACKAGE DIMENSIONS



APPENDIX : TEST MODE SETTING MAP

TESTM	TEST0	TEST1	TEST2	Operation MODE
0	0	0	0	Normal Play Mode
0	0	0	1	CDP Test Mode, Newly Added
0	0	1	0	-
0	0	1	1	-
0	1	0	0	Memory Bist Test Mode
0	1	0	1	Scan Test Mode
0	1	1	0	NAND Tree Test Mode
0	1	1	1	-
1	0	0	0	-
1	0	0	1	Equalizer & Slice Circuit Test Mode 1
1	0	1	0	PLL Test Mode
1	0	1	1	Servo Test Mode 1
1	1	0	0	Servo Test Mode 2
1	1	0	1	Servo Test Mode 3
1	1	1	0	Servo Test Mode 4
1	1	1	1	Servo Test Mode 5

Mode		NORMAL						
Mode Select	nmon [3:0]	0000	0001	0010	0011	0100	0101	xxxx
	BISTMODE	0	0	0	0	0	0	1
PIN Number	P122	FRSY	clvlock	efmjunk		clvlock	TLKB	DONE
	P88	GFS	efmjunk	efmsymck		TODR_test	FLKB	DIAG_rom
	P100	CK16M	efmsymck	scor		adc_data_ test[9]	COUT	ERRORB
	P90	WFCK	scor	rfck_i		PEAK_MON	INT0_224	0
	P91	RFCK	rfck_i	-		EFM	plllock	0

Mode		NORMAL	SRAM TEST	ECC Monitor					
Mode select	MONITOR [3:0]	0000	0000	0001	0010	0011	0100	0101	0110
	SRAM_ TEST	0	1	X					
PIN Number	P139	PCD7	isdout [1]	modeofECC [1]	EPInum_p [7]	EPIerr [10]	EPIerr [2]	shiftII	Lcount [1]
	P140	PCD6	isdout [0]	modeofECC [0]	EPInum_p [6]	EPIerr [9]	EPIerr [1]	shiftIII	Lcount [0]
	P141	PCD5	tstdout [1]	cor_jjongn	EPInum_p [5]	EPIerr [8]	EPIerr [0]	Qcofena	MaxEra
	P142	PCD4	tstdout [0]	eccend_in	EPInum_p [4]	EPIerr [7]	exFlag [1]	CoefEn	Maxm1Era
	P143	PCD3	numErr [4]	indtruction [3]	EPInum_p [3]	EPIerr [6]	exFlag [0]	c2eu	MaxCorr
	P144	PCD2	numErr [3]	indtruction [2]	EPInum_p [2]	EPIerr [5]	synen	EUend	CECend
	P145	PCD1	numErr [2]	indtruction [1]	EPInum_p [1]	EPIerr [4]	eusften	FirstECC	Ctable
	P146	PCD0	numErr [1]	indtruction [0]	EPInum_p [0]	EPIerr [3]	Epolysft	initStart	rptmod

Mode		NORMAL	CD ECC Monitor	EFM Dem. Monitor		CD Mode Monitor		EFM Dem. data Monitor	Servo Monitor
Mode select	MONITOR [3:0]	0000	0111	1000	1001	1010	1011	1100	1110
	SRAM_TEST	0	x						
PIN Number	P139	PCD7	modeofECC [1]	mid_adr [3]	mfcnt [4]	demdatckZ	demdat [7]	efmdata [7]	TLKB
	P140	PCD6	numErr [2]	mid_adr [2]	mfcnt [3]	zfrsyi	demdat [6]	efmdata [6]	FLKB
	P141	PCD5	numErr [1]	mid_adr [1]	mfcnt [2]	mic_en	demdat [5]	efmdata [5]	COUT
	P142	PCD4	numErr [0]	mid_adr [0]	mfcnt [1]	ecc_en	demdat [4]	efmdata [4]	INT0_224
	P143	PCD3	0	idsyZ	mfcnt [0]	efm_en	demdat [3]	efmdata [3]	plllock
	P144	PCD2	0	miderr	siderr	tran_en	demdat [2]	efmdata [2]	flag_for
	P145	PCD1	0	idconerr	scor	up_low	demdat [1]	efmdata [1]	flag_bak
	P146	PCD0	0	syok	scand	ref_en	demdat [0]	efmdata [0]	0

MONITORING SIGNAL DESCRIPTION

Monitoring Condition		Monitoring Signal Name	Signal Description
SRAM_TEST	MONITOR [3:0]		
1	0000	isdout[1:0]	Internal SRAM(edcram) Data Out
		tstout[1:0]	Internal SRAM(FR) Data Out
		numErr[4:1]	Number of Ecc Error
x	0001	modeofECC[1:0]	PI/PO, Error/Erasure Correction Mode
		cor_jjongn	ECC Codeword Separation Signal
		eccend_in	ECC end interrupt
		instruction[3:0]	ECC command
	0010	EPInum_p[7:0]	Number of codewords with errors (first PI correction)
	0011	EPIerr[10:3]	Number of errors in first PI correction
	0100	EPIerr[2:0]	Number of errors in the first PI correction
		exFlag[1:0]	Flag Overflow
		synen	Syndrome Enable
		eusften	EU Block Signal Shift Period
		Epolysft	EU Block Signal Shift Period
	0101	shiftII	EU Block Signal Shift Period
		shiftIII	EU Block Signal Shift Period
		Qcofena	EU Block Internal Signal Monitor
		CoefEn	EU Block Internal Signal Monitor
		c2eu	EU Block Internal Signal Monitor
		EUend	EU Block end signal
		FirstECC	'High' for the first PI
		initStart	ECC Block initial signal
	0110	Lcount[1:0]	Control Block internal signal
		MaxEra	Erasure correction mode
		Maxm1Era	Erasure correction mode
		MaxCorr	Maximum correction errors
		CECend	Control signal
		Ctable	Correctable Codeword identification
		rptmod	Repeat Mode

Monitoring Condition		Monitoring Signal Name	Signal Description
SRAM_ TEST	MONITOR [3:0]		
x	0111	modeofECC[1]	PI/PO, Error/Erasure Correction Mode
		numErr[2:0]	Number of ECC Error
	1000	mid_adr[3:0]	ID sync address
		idsyZ	ID sync
		miderr	ID data error flag (Active 'H'), generate after one ID sector
		idconerr	ID data continuance check flag (error ---> 'H')
		syok	insertion ID sync and detect id sync comparison flag sync (match --> 'H')
	1001	mfcnt[4:0]	frame sync count value
		siderr	ID data error flag (active 'H'), generate at generation time
		scor	s0,s1 (CD Mode sub sync) Oring signal
		scand	s0,s1 (CD Mode sub sync) Anding signal
	1010	demdatckZ	efm data catch clock
		zfrsyi	rfck base frame sync
		mic_en	micom direct enable
		ecc_en	ecc read/write enable
		efm_en	efm data write enable
		tran_en	transfer data read enable
		up_low	micom data up/low
		ref_en	refresh enable
	1011	demdat[7:0]	demodulation data
	1100	efmdata[7:0]	EFM/EFM+ demodulation data
	1110	TLKB	Tracking LOCK (when "L", LOCK)
		FLKB	Focus LOCK (when "L", LOCK)
		COUT	Tracking counter clock out
		INT0_224	224 step (151.2kHz) interrupt signal
		plllock	PLL LOCK signal
		flag_for	Spindle motor bidirectional overflow indicator
		flga_bak	Spindle motor reverse direction overflow indicator
		0	