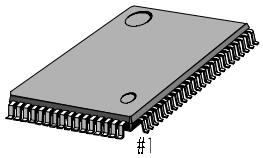
DIGITAL SIGNAL PROCESSOR

80-QFP-1420C



The S5L9826F01 is a CMOS integrated circuit designed for the Digital Audio Signal Processor for Compact Disc Player. It is a monolithic IC that builts-in 16-bit Digital Analog Convertor, ESP Interface and Digital De-emphasis additional conventional DSP function.

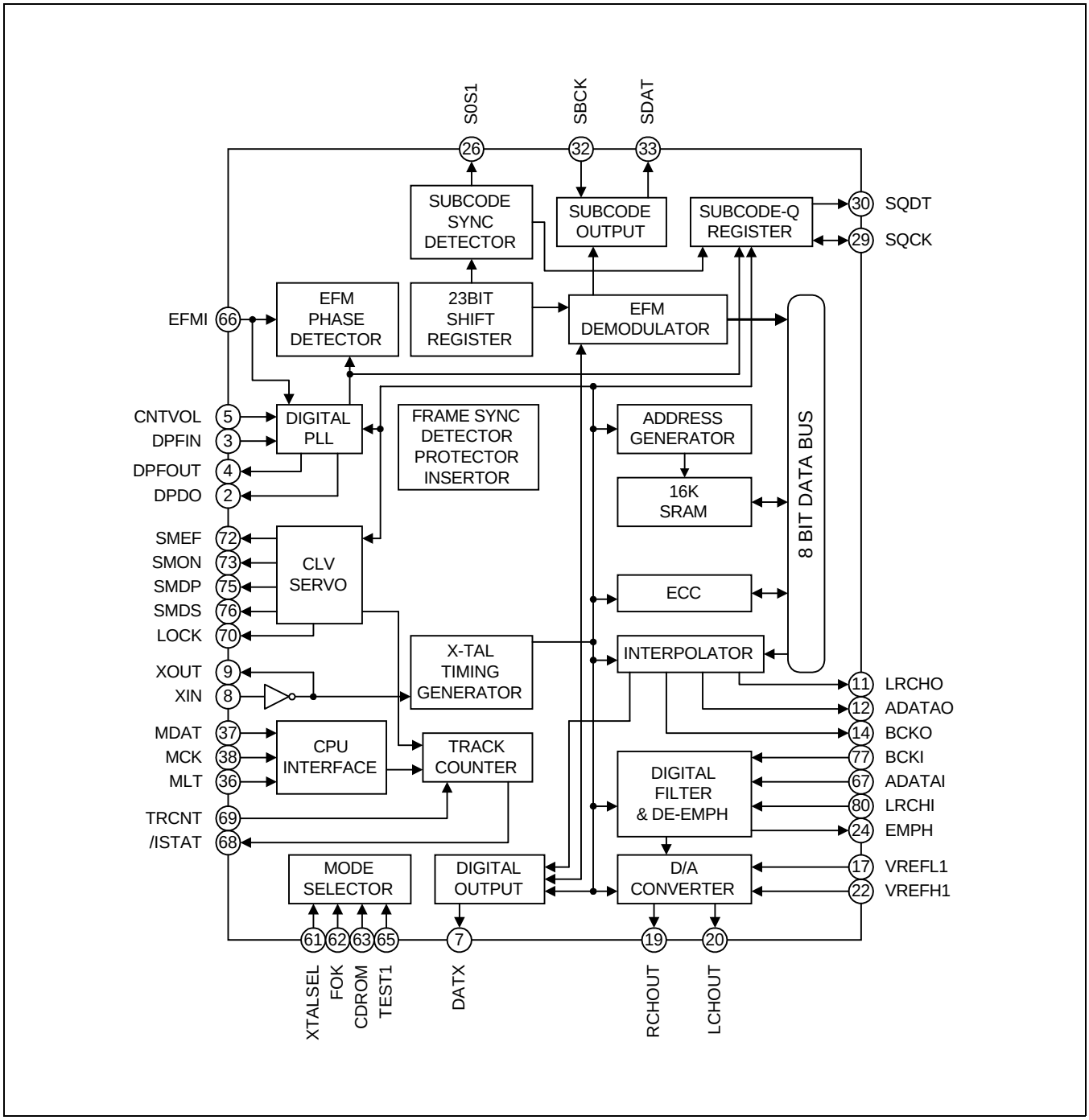
FEATURES

- EFM data demodulation
- Frame sync detection / protection / insertion
- Powerful error correction (C1: 2 error; C2: 4 erasure)
- Interpolation
- 8fs digital filter (51th+13th+9th)
- Subcode data serial output
- CLV servo controller
- MICOM interface
- Digital audio output
- Digital de-emphasis
- ESP interface
- Built-in 16K SRAM
- Built-in digital PLL
- Double speed play available
- Built-in 16-bit D/A converter
- V_{DD} = 5V

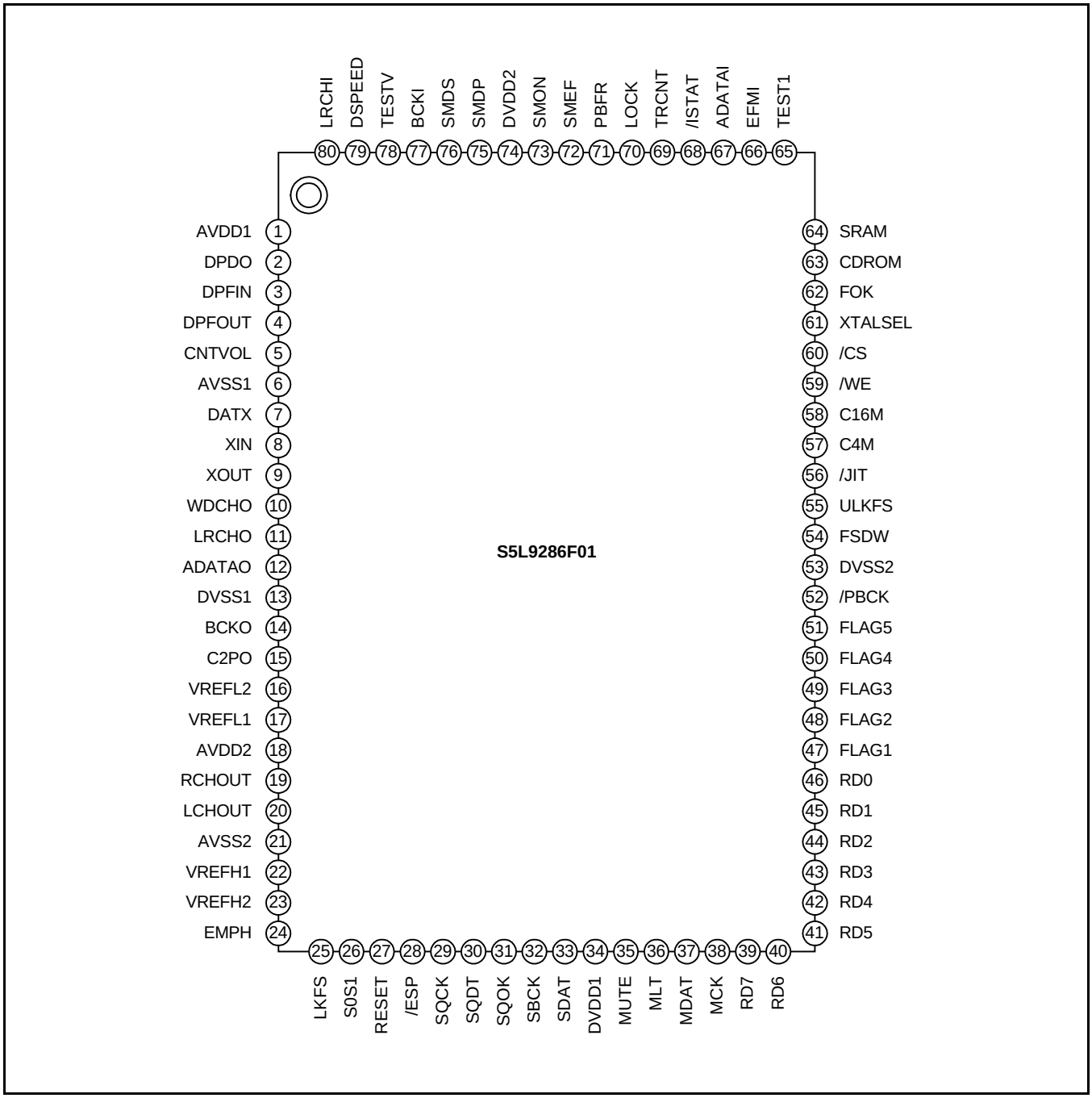
ORDERING INFORMATION

Device	Package	Tempe. Range
S5L9286F01-Q0R0	80-QFP-1420C	-20°C – +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	SYMBOL	IO	DESCRIPTION
1	AVDD1	-	Analog VCC1
2	DPDO	O	Charge pump output for Digital PLL
3	DPFIN	I	Filter input for Digital PLL
4	DPFOUT	O	Filter output for Digital PLL
5	CNTVOL	I	VCO control voltage for Digital PLL
6	AVSS1	-	Analog Ground1
7	DATX	O	Digital Audio output data
8	XIN	I	X'tal oscillator input
9	XOUT	O	X'tal oscillator output
10	WDCHO	O	Word clock output of 48bit/Slot (88.2kHz)
11	LRCHO	O	Channel clock output of 48 bit/Slot (44.1kHz)
12	ADATAO	O	Serial audio data output of 48 bit/Slot (MSB first)
13	DVSS1	-	Digital Ground1
14	BCKO	O	Audio data bit clock output of 48 bit/Slot (2.1168MHz)
15	C2PO	O	C2 Pointer for output audio data
16	VREFL2	I	Input terminal2 of reference voltage "L" (Floating)
17	VREFL1	I	Input terminal1 of reference voltage "L" (GND connection)
18	AVDD2	-	Analog VCC2
19	RCHOUT	O	Right-Channel audio output through D/A converter
20	LCHOUT	O	Left-Channel audio output through D/A converter
21	AVSS2	-	Analog ground2
22	VREFH1	I	Input terminal1 of reference voltage "H" (VDD connection)
23	VREFH2	I	Input terminal2 of reference voltage "H" (Floating)
24	EMPH	O	H: Emphasis ON, L: Emphasis OFF
25	LKFS	O	The Lock Status output of frame sync
26	S0S1	O	Output of subcode sync signal(S0+S1)
27	RESET	I	System reset at "L"
28	/ESP	I	ESP function ON/OFF control ("L": ESP function ON, "H": ESP function OFF)
29	SQCK	I	Clock for output Subcode-Q data

PIN DESCRIPTION (continued)

PIN NO	SYMBOL	IO	DESCRIPTION
30	SQDT	O	Serial output of Subcode-Q data
31	SQOK	O	The CRC (Cycle Redundancy Check) check result signal output of Subcode-Q
32	SBCK	I	Clock for output subcode data
33	SDAT	O	Subcode serial data output
34	DVDD1	-	Digital VDD1
35	MUTE	I	Mute control input ("H": Mute ON)
36	MLT	I	Latch Signal Input from Micom (Schmit Trigger)
37	MDAT	I	Serial data input from Micom (Schmit Trigger)
38	MCK	I	Serial clock input from Micom (Schmit Trigger)
39	RD7	I/O	SRAM data I/O port 8 (MSB)
40	RD6	I/O	SRAM data I/O port 7
41	RD5	I/O	SRAM data I/O port 6
42	RD4	I/O	SRAM data I/O port 5
43	RD3	I/O	SRAM data I/O port 4
44	RD2	I/O	SRAM data I/O port 3
45	RD1	I/O	SRAM data I/O port 2
46	RD0	I/O	SRAM data I/O port 1 (LSB)
47	FLAG1	I/O	Monitoring output for error correction (RA0)
48	FLAG2	I/O	Monitoring output for error correction (RA1)
49	FLAG3	I/O	Monitoring output for error correction (RA2)
50	FLAG4	I/O	Monitoring output for error correction (RA3)
51	FLAG5	I/O	Monitoring output for error correction (RA4)
52	/PBCK	I/O	Output of VCO/2 (4.3218MHz) (RA5)
53	DVSS2	I/O	Digital ground 2
54	FSDW	I/O	Window or unprotected frame sync (RA6)
55	ULKFS	I/O	Frame sync protection state (RA7)
56	/JIT	I/O	Display of either RAM overflow or underflow for $\pm$ 4 frame jitter margin (RA8)
57	C4M	I/O	Only monitoring signal (4.2336MHz) (RA9)
58	C16M	I/O	16.9344MHz signal output(RA10)
59	/WE	I/O	Terminal for test
60	/CS	I/O	Terminal for test

PIN DESCRIPTION (continued)

PIN NO	SYMBOL	IO	DESCRIPTION
61	XTALSEL	I	Mode Selection1 (H: 33.8688MHz, L: 16.9344MHz)
62	FOK	I	The input for FOK signal of servo
63	CDROM	I	Mode Selection2 (H: CD-ROM, L: CDP)
64	SRAM	I	TEST input terminal (GND connection)
65	TEST1	I	TEST input terminal (GND connection)
66	EFMI	I	EFM signal input
67	ADATAI	I	Serial audio data input of 48 bit/Slot (MSB first)
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking counter input signal
70	LOCK	O	Output signal of LKFS condition sampled PBFR/16 (if LKFS is "H", LOCK is "H", if LKFS is sampled "L" at least 8 times by PBFR/16, LOCK is "L".)
71	PBFR	O	Write frame clock (Lock: 7.35KHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spindle servo
74	DVDD2	-	Digital VDD2
75	SMDP	O	Spindle Motor drive (Rough control in the SPEED mode, Phase control in the PHASE mode)
76	SMDS	O	Spindle Motor drive (Velocity control in the PHASE mode)
77	BCKI	I	Audio data bit clock input of 48 bit/Slot (2.1168MHz)
78	TESTV	I	TEST input terminal (GND connection)
79	DSPEED	I	TEST input terminal (VDD connection)
80	LRCHI	I	Channel clock input of 48 bit/Slot (44.1KHz)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 – 7.0	V
Input Voltage	V_I	-0.3 – 7.0	V
Output Voltage	V_O	-0.3 – 7.0	V
Operating Temperature	T_{OPR}	-20 – 75	^oC
Storage Temperature	T_{STG}	-40 – 125	^oC

ELECTRICAL CHARACTERISTIC

DC Characteristic

(Vcc = 5V, Vss = 0V, Ta=25^{o}C, unless otherwise specified)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
High input voltage1	V_{IH1}	(note1)	$0.7V_{DD}$	–	–	V
Low input voltage1	V_{IL1}		–	–	$0.3V_{DD}$	V
High input voltage2	V_{IH2}	(note2)	$0.8V_{DD}$	–	–	V
Low input voltage2	V_{IL2}		-	–	$0.2V_{DD}$	V
High output voltage1	V_{OH1}	I_{OH} = –1mA, (note3)	V_{DD}–0.5	–	V_{DD}	V
Low output voltage1	V_{OL1}	I_{OL} = 1mA, (note3)	0	–	0.4	V
High output voltage2	V_{OH2}	I_{OH} = –1mA, (note4)	V_{DD}–0.5	–	V_{DD}	V
Low output voltage2	V_{OL2}	I_{OL} = 2mA, (note4)	0	–	0.4	V
Input leakage current	I_{LKG}	V_I = 0–V_{DD}, (note5)	–5	–	5	µA
Tri-state output leakage current	I_{OLKG}	V_O = 0–V_{DD}, (note5)	–5	–	5	µA

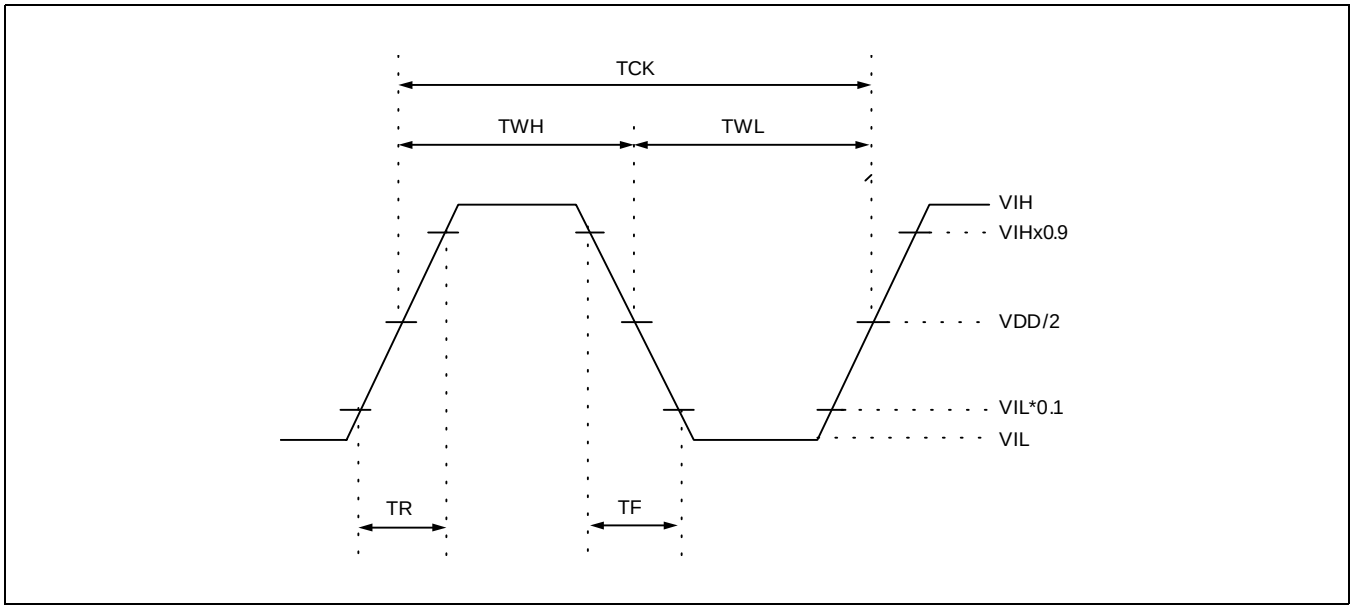
NOTES: Related pins

1 XTALSEL, TEST0, CDROM, SRAM, TEST1, EFMI, ADATAI, BCKI, DSPEED & LRCHI
2. All bi-directional pins, RESET, MLT, MCK, MDAT, MUTE, TRCNT
3. All output pins except /ISTAT, OSCILATOR, DPFOUT
4. /ISTAT
5. SMEF, SMDP, SMSD, DPDO

AC Characteristic

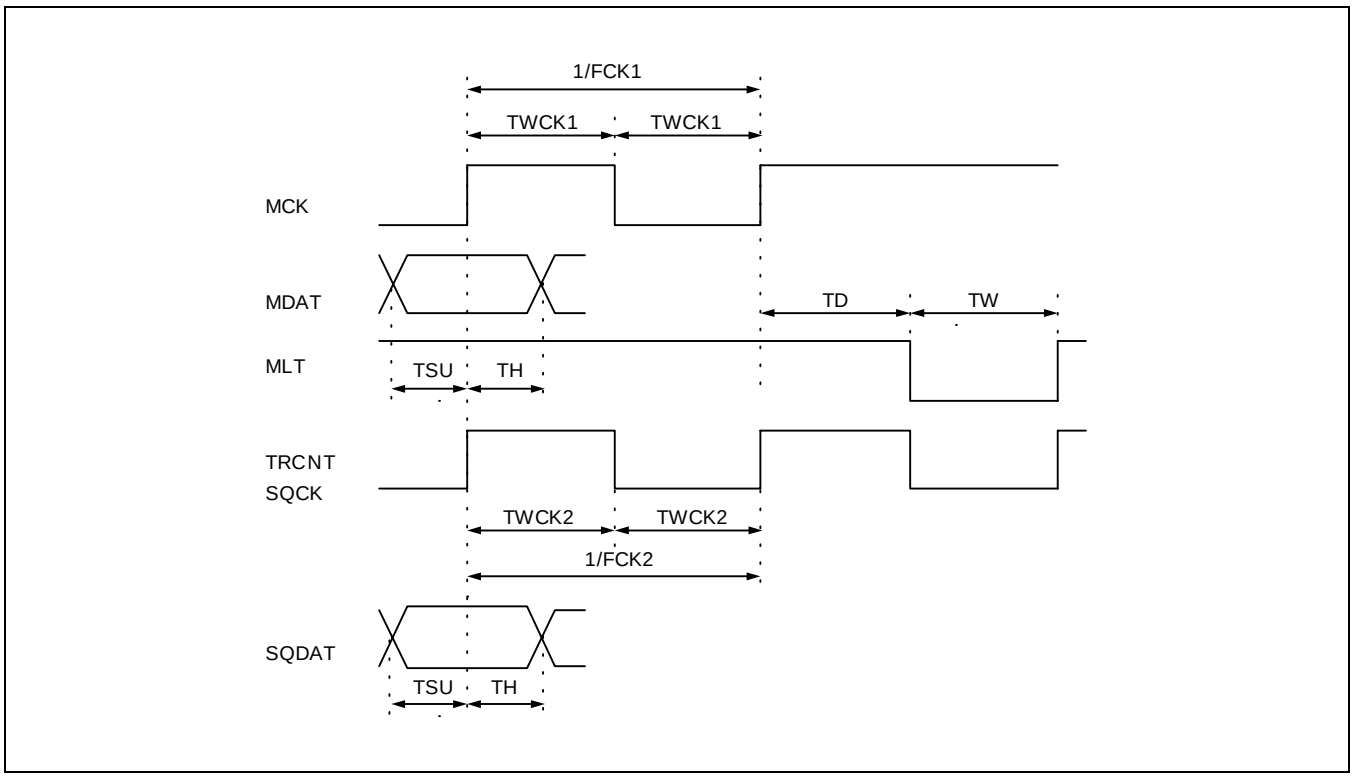
When pulse is input to XIN, VCOI pin (Vcc=5V, Vss=0V, Ta=25°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit
High Level Pulse Width	T_{WH}	13	–	–	ns
High Level Pulse Width	T_{WL}	13	–	–	ns
Pulse Frequency	T_{CK}	26	–	–	ns
Input High Level	V_{IH}	V_{DD}–1.0	–	–	V
Input Low Level	V_{IL}	–	–	0.8	V
Rising & Falling Time	t_R,t_F	–	–	8	ns



MCK, MDAT, MLT & TRCNT (Vcc=5V, Vss=0V, Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	F_{CK1}	-	-	1	MHz
Clock Pule Width	T_W	300	-	-	ns
Setup Time	T_{SU}	300	-	-	ns
Hold Time	T_H	300	-	-	ns
Delay Time	T_D	300	-	-	ns
Latch Pulse Width	T_{WCK1}	300	-	-	ns
TRCNT, SQCK Frequency	F_{CK2}	-	-	1	MHz
TRCNT, SQCK Pulse Width	T_{WCK2}	300	-	-	ns



FUNCTION DESCRIPTION

Micom Interface

The data inputted from Micom is inputted to MDAT and transfered by MCK, and the inputted signal is loaded to control register by means of MLT. The timing chart is as follows.

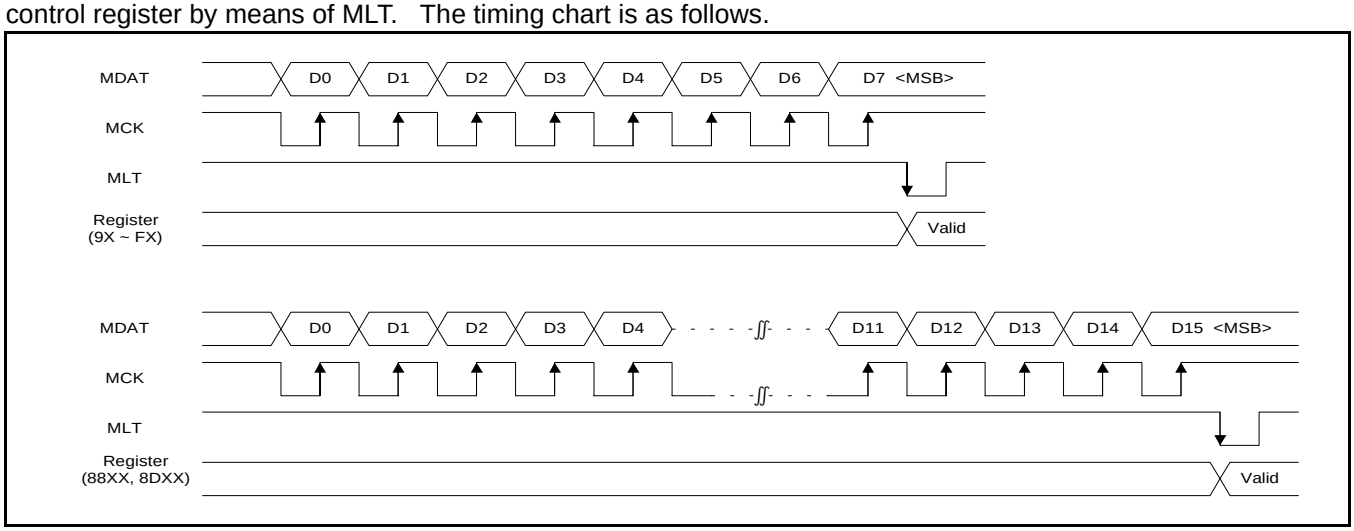


Figure 1. MICOM data input timing chart

Table 1. Control register & data

Control Regster	Comment	Address D7~D4	Data				/ISTAT Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	9X	ZCMT	-	NCLV	CRCQ	S0S1
CNTL-S	Frame Sync Protection Attenuation Control	AX	FSEM	FSEL	WSEL	ATTM	LKFS
CNTL-L	Tracking Counter Lower 4 Bits	BX	TRC3	TRC2	TRC1	TRC0	/COMPLETE
CNTL-U	Tracking Counter Upper 4 Bits	CX	TRC7	TRC6	TRC5	TRC4	/COUNT
CNTL-W	CLV Control	DX	-	WB	WP	GAIN	FOK
CNTL-C	CLV-Mode	EX	CM3	CM2	CM1	CM0	/(Pw ≥ 64)
CNTL-D	Double-speed	FX	0	0	DS1	DS2	TRCNT

Control Regster	Comment	Address D15-D8	Data								/ISTAT Pin
			D7	D6	D5	D4	D3	D2	D1	D0	
CNTL-F	Function Control	88XX	-	-	DEEM	ERA_ OFF	-	-	-	-	Hi-Z
CNTL-H	ESP,monitor Pin Control	8DXX	-	-	-	-	-	-	ESP_ ON	DUMB	Hi-Z

NOTE: –;Reserved

CONTROL REGISTER DESCRIPTION

• CNTL-Z This register carries out the following functions: audios zero cross mute, phase pin control, phase servos control signal management, and the decision whether or not to include SQOK data in SQDT.

Bit	3	2	1	0
Identifier	**ZCMT**	**-**	**NCLV**	**CRCQ**

ZCMT Zero cross mute

0	Zero cross mute is OFF
1	Zero cross mute is ON

NCLV Phase servos control

0	Phase Servo operated by frame sync
1	Phase Servo controlled by base counter

CRCQ Decide whether or not to include SQOK data in SQDT

0	SQDT output not including SQOK
1	SQDT = SQOK, when SOS1 is “H”.

• CNTL-S This register sets the frame sync protection and attenuation. FWSEL of CNTL-D is added to define window size. .

Bit	3	2	1	0
Identifier	**FSEM**	**FSEL**	**WSEL**	**ATTM**

FSEM, FSEL Frame sync protection

0	0	2
0	1	4
1	0	8
1	1	13

WSEL Frame Sync protection window size

0	± 3T
1	± 7T

ATTM, MUTE Control the Frame Sync attenuation

0	0	0 dB
0	1	- ∞ dB
1	0	-12 dB
1	1	-12 dB

• CNTL-L, U When the number of tracks to be counted is input from MICOM, the CNTL-L, or CNTL-U register loads the data into the tracking counter. This tracking counter is used for improving track jump characteristics.

• CNTL-W This register sets the CLV-Servos control period and gain..

Bit	3	2	1	0
Identifier	**-**	**WB**	**WP**	**GAIN**

WB Bottom hold period control in speed mode

0	XTFT/32
1	XTFR/16

WP Peak hold period control in speed mode

0	XTFR/4
1	XTFR/2

GAIN SMDS gain control in speed mode

0	- 12 dB
1	0 dB

• CNTL-C This register sets the CLV-Servos operating Mode.

D3 — D0	**MODE**	**SMDP**	**SMSD**	**SMEF**	**SMON**
1000	Forward	H	Hi-Z	L	H
1010	Reverse	L	Hi-Z	L	H
1110	Speed	Speed-mode	Hi-Z	L	H
1100	Hspeed	Hspeed-mode	Hi-Z	L	H
1111	Phase	Phase-mode	PHASE-MODE	Hi-Z	H
0110	Xphsp	Speed or Phase-mode	Hi-Z or PHASE-MODE	L, Hi-Z	H
0101	Vphsp	Speed or Phase-mode	Hi-Z or PHASE-MODE	L, Hi-Z	H
0000	Stop	L	Hi-Z	L	L

• CNTL-D This register sets the normal speed and double speed mode.

Bit	3	2	1	0
Identifier	**.3**	**.2**	**.1**	**.0**

.3 - .0 Speed control

0	0	0	0	Normal Speed
0	0	1	1	Double Speed (2X)

• CNTL-E This register controls the de-emphasis. .

Bit	3	2	1	0
Identifier	**.3**	**.2**	**.1**	**.0**

.3 - .0 CLV-servo mode control. Refer to WB of CNTL-W Register.

×	×	1	×	Internal digital de-emphasis
×	×	0	×	External analog de-emphasis

NOTE: D1 bit becomes to “L” when reset. MICOM must give the commands of attenuation and mute, when forward / backward searching. If not, the wrong operation ocurrs easilly during the execution when fast searching.

TRACKING COUNTER BLOCK

When the number of tracks to be jumped is input from MICOM, the track number is loaded from MLTs positive edge to the register. If CNTL-L is selected, /COMPLETE signal is output to the /ISTAT pin, and if CNTL-U is selected, /COUNT signal is output. The Timing Diagrams of the tracking counters are Figure-3 and Figure-4.

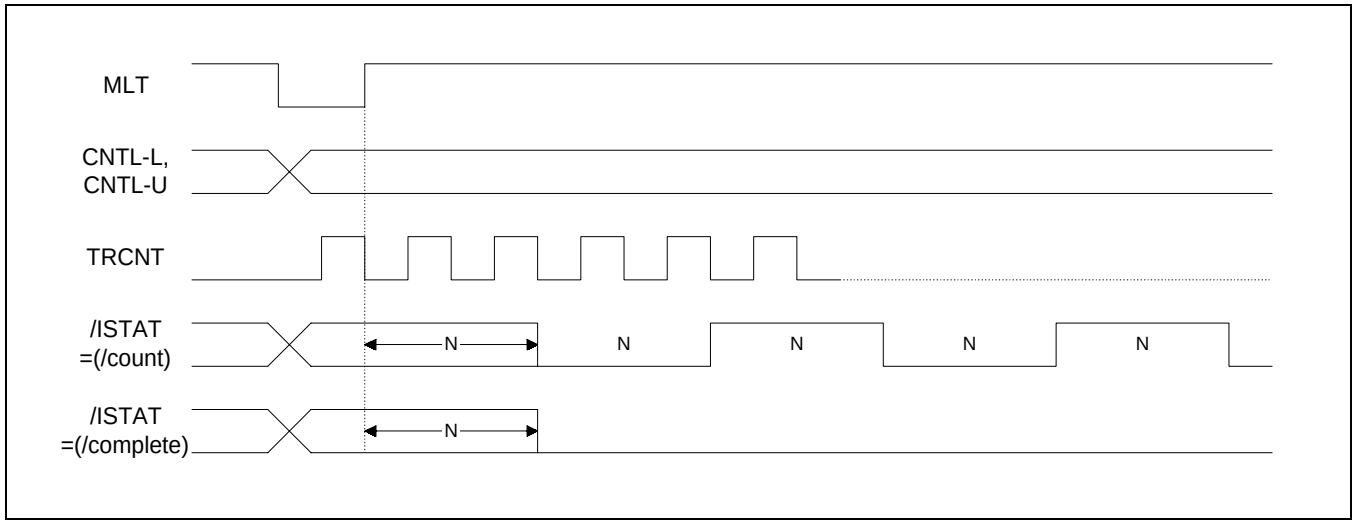


Figure 2. Tracking Counter Timing Diagram

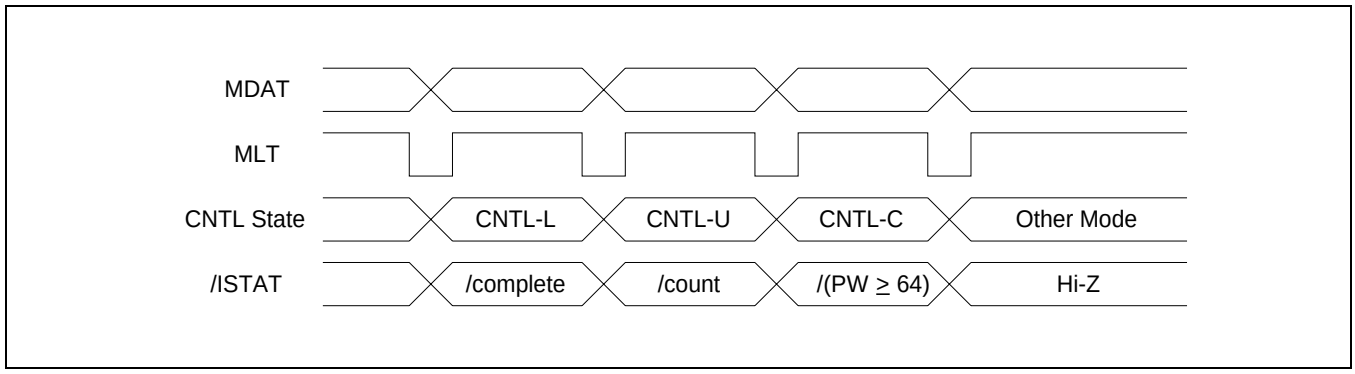


Figure 3. /ISTAT Output Signal According to the CNTL Register

EFM DEMODULATION

The EFM block is composed of the following parts: EFM demodulator to demodulate the EFM signal read from the disc, EFM phase detector, and the control signal generator.

EFM DEMODULATOR

The modulated 14 channel bit data is demodulated into 8-bit data. There are two types of demodulated data: subcode data and audio data. Subcode data is input into the subcode handling block, and the audio data is stored in the internal 16 K SRAM, and its errors are corrected.

EFM PHASE DETECTOR

The EFM signal input from the Disc includes 2.1609 MHz components. To detect the phase of this signal, a Bit Clock (/PBCK) of 4.3218 MHz is used. PBCK detects the phase of the EFM signals Edge, and sends the results to the APD0 pin.

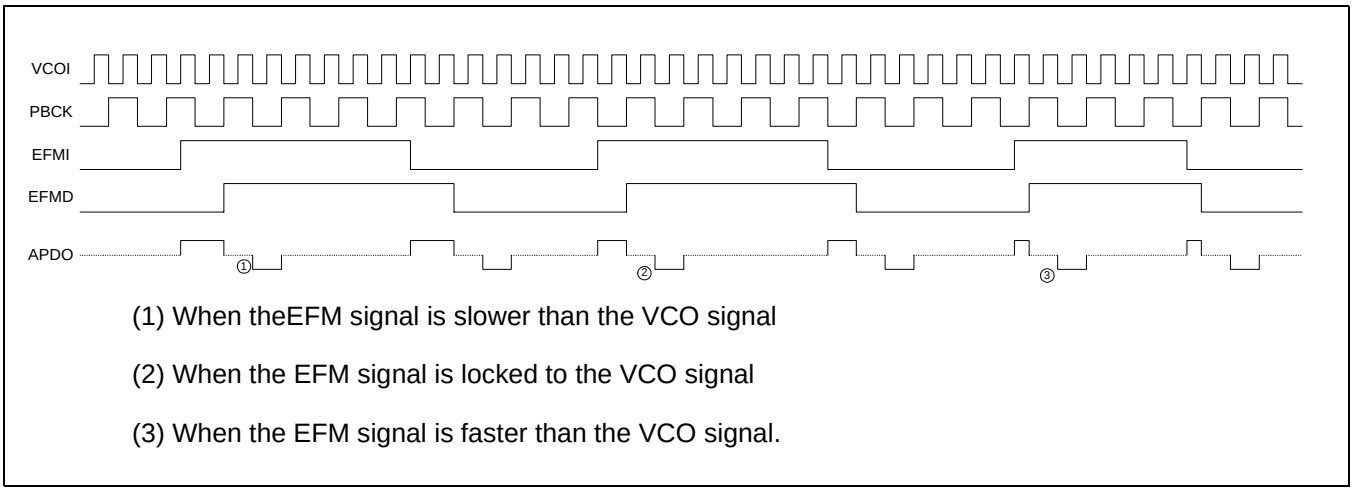


Figure 4. EFM Phase Detector Timing Diagram

FRAME SYNC DETECT/PROTECT/INSERT

• Frame Sync Detect
Data is composed of units of frame, and a frame is composed of frame sync, subcode data, audio data, and redundancy data. This IC detects frame sync to maintain synchronization.

• Frame Sync Protect/Insert
There are some cases in which frame sync is not detected, or detected it from other data which does not include frame sync, due to disc error or jitter. In these cases, the frame sync must be protected and inserted.
To protect frame sync, a window is made by WSEL of the CNTL-S register. The frame sync entering this window is considered valid data, and the frame sync which leaves this window is ignored. If frame sync is not detected within the frame sync protect window, insert instead the frame sync made in the internal counter. If frame sync is inserted continuously, reaching the number of frames set by FSEM and FSEL of the CNTL-S register, the following occurs: ULKFS becomes high, the frame sync protect window is ignored, and the frame sync detected next is accepted unconditionally. When a frame sync is accepted, the ULKFS signal becomes L, and accepts the frame sync detected within the window (refer to below Table).

LKFS	ULKFS	Comment
1	0	Play back frame sync and the generated sync coincide.
0	0	1) The play back frame sync and the generated frame sync do not coincide, but PBFR sync is detected from within the window selected by WEL. 2) PBFR sync and XTFR sync do not coincide, and are not detected from within the window selected by WSEL. Sync insert is carried out.
0	1	1) Immediately after the following situation: Frame sync is not detected within the window, so frame is inserted in the amount set by CNTL-S registers FSEM and FSEL. 2) If PBFR sync is still undetected after 1).

SUBCODE BLOCK

The subcode sync signals S0 and S1 are detected in the Subcode sync block. S1 is detected one frame after S0 is detected. At this time, S0+S1 signal is output to the S0S1 pin, and when the S0S1 signal is high, the S0S1 signal is output to the SDAT pin. Out of the data input into the EFMI pin, the 14-bit subcode data is EFM demodulated to 8-bit (P, Q, R, S, T, U, V, W) subcode data, synchronized with the WBCK signal, and output to SDAT by the SBCK clock. Out of the 8 subcode data, only Q data is stored in the 80 shift registers by the WBCK signal.

If the CRC result is error, low is output to the SQCK pin, and if not, high is output.
If the CNTL-Z registers CRCQ is high, the CRC result is output to the SQDT pin from when the S0 and S1 are high to SQCKs negative edge. The subcode blocks timing diagram is as follows:

Timing Relation of SQCK, SQDT and S0S1 when SQEN = H

If subcode-Q datas CRCQ is high, the SQOK signal is output to SQDT according to the SQCK, and if CRCQ is low, the SQOK signal is not output to SQDT.

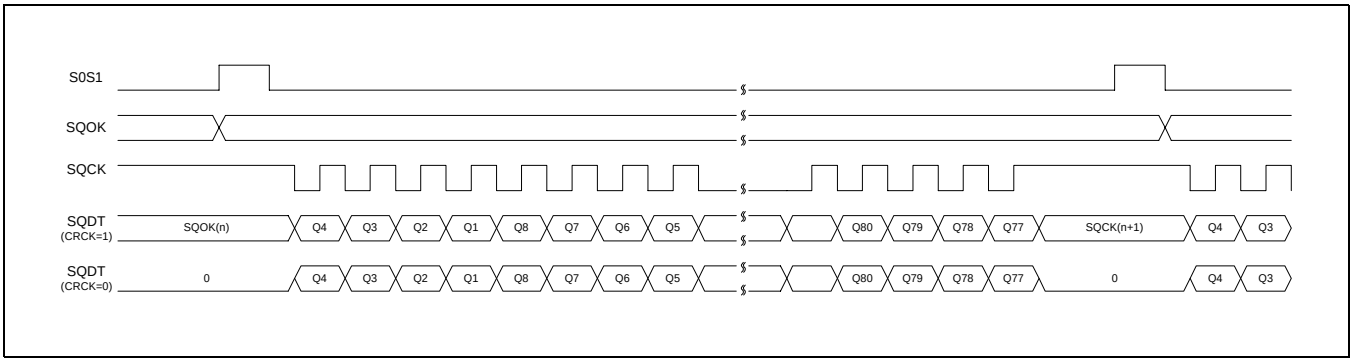
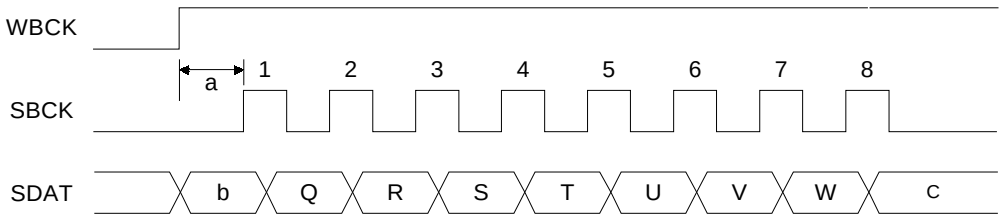


Figure 5. Subcode-Q Timing Diagram

Timing Relation of SDAT and SBCK



a) After PBFR goes negative edge, SBCK is set to L for about 10 µs.
b) If S0S1 is L, subcode P is output, and if S0S1 is high, S0S1 is output.
c) If there are more than 7 pulses input into the SBCK pin, the subcode data P, Q, R, S, T, U, V, and W data are output repeatedly.

ERROR CORRECTING CODE (ECC)

When disc data is damaged, it is corrected using the ECC (Error Correcting Code) block. It uses the CIRC (Cross Interleaved Reed-Solomon Code), correcting up to 2 errors when C1 (32, 28), and up to 4 erasures when C2 (28, 24). Error correction handles the data in units of 8-bit 1 symbol.

The ECC block has Pointer handling function, and can generate a C1 pointer in C1 correction, and a C2 pointer in the C2 correction. The C1 and C2 pointers output a flag about the ECC-handled data to mark it as error data. This Flag information signal is input into the interpolator, and used for handling the error data. Also, the Error correcting results can be monitored using the FLAG1, FLAG2, FLAG3, FLAG4, FLAG5 pins

MODE	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	REMARK
C1 No error	0	0	0	0	0	C1 correction start
C1 1 error	0	0	0	0	1	-
C1 2 error	0	0	0	1	0	-
C1 Irretrirvable error	0	1	1	1	1	C1 pointer set
C2 No error	1	0	0	0	0	C2 correction start
C2 1 error	1	0	0	0	1	-
C2 2 error	1	0	0	1	0	-
C2 3 error	1	0	0	1	1	-
C2 4 error	1	0	1	0	0	-
C2 Irretrievable error 1	1	1	1	1	0	C1 pointer copy
C2 Irretrievable error 2	1	1	1	1	1	C2 pointer set

INTERPOLATOR / MUTE

Interpolator

If a burst error occurs on the disc, sometimes data cannot be corrected even if you carry out the ECC process. The Interpolator block uses the ECCs C2 pointer to interpolate the data.

The audio data is input into the Data bus in the following order: for each L/R-ch: 8-bit C2 point, lower data 8 bits, and upper data 8 bits.

If C2PO pin is high, and one error has occurred, the average value interpolation is carried out, and if three consecutive errors occurred, the previous value hold interpolation is carried out.

For one period of LRCH, if LRCH is low, R-ch data is output, and if LRCH is high, L-ch data is output. Please refer to Figure-9 for the Interpolator blocks timing diagram.

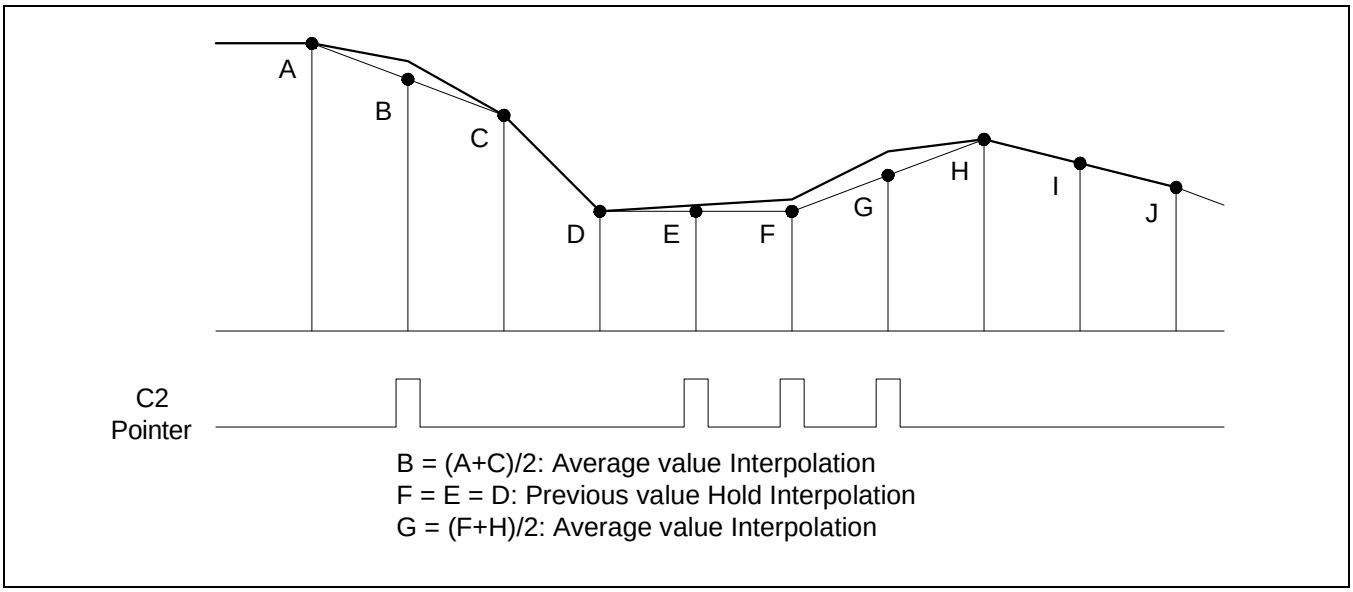


Figure 6. Interpolation Method

Mute/Attenuation

The audio data can be muted or weakened by the ATTM signal of the MUTE pin and CNTL-S register.

- Zero Cross Mute
  The audio data is muted when the CNTL-Z registers ZCMT is high, mute is high, and the upper 6 bits of audio data are all high.
- Muting
  The audio data is in Muting is the CNTL-Z registers ZCMT is L and the Mute pin is high.
- Attenuation
  Audio signal is weakened by the CNTL-Z registers ATTM and Mute signal.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	– ∞ dB
1	0	–12 dB
1	1	–12 dB

CLV SERVO

CNTL-C, E, G1, G2, and G3 registers are selected to control the CLV (Constant Linear Velocity) servo using the data input from MICOM. Also, the design is such that the servo control is stable when setting the speed. When setting the speed, the /(Pw≥64) signal can be detected from the /ISTAT pin only if the CNTL-D register is first set before the CNTL-C register is selected.

Forward

This mode rotates the spindle motor in the forward direction. The related output pin status are as follows: .

SMDP	SMSD	SMEF	SMON
H	Hi-Z	L	H

Reverse

This mode rotates the spindle motor in the reverse direction. The related output pin status are as follows:.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	H

Speed-mode

The spindle motor is controlled roughly by speed mode when track jumping or EFM phase is unlocked.

If a period of VCO is "T", the pulse width of frame sync is 22T. In case that the signal detected from EFM signal exceeds 22T by noise on the disc and etc., it must be removed, if not, the right frame sync can't be detected. In this case, the pulse width of EFM signal is detected by peak hold clock and bottom hold clock. (Peak hold clock is XTFR/2 or XTFR/4, and bottom hold clock is XTFR/16 or XTFR/32.)

The detected value is used for synchronized frame signal. If the frame signal is less than 21T, the SMDP terminal outputs "L", eaqul to 22T, outputs "Hi-Z", and more than 23T, ouputs "H".

If the gain signal of CNTL-W register is "L", the output of SMDP terminal is reduced up to –12dB, if it is "H", there is no reduction.

Output condition: SMSD="Hi-Z", SMEF="L", SMON="H".

Hspeed-Mode

The rough servo mode, which moves 20,000 tracks in high speed acts between the inside and outside of the CD.

The mirror domain of track which hasn't pit is duplicated with 20KHz signal to EFM. In this case, servo action is unstable because the peak value of mirror signal which is longer than orignal frame sync signal which is detected. In Hspeed mode, by using the 8.4672/256MHz signal against peak hold and XTFR/16 or XTFR/32 signal against bottom hold, the mirror component is removed, and Hspeed servo action to be stable.

he output condition is as following.

SMDP	SMSD	SMEF	SMON
–	Hi-Z	L	H

Phase-Mode

The phase mode is the mode to control the EFM phase. Phase difference between PBFR/4 and XTFR/4 is detected when NCLV of CNTL-Z register is "L",and phase difference between Read Base Counter/4 and Write Base Counter/4 detected when NCLV is "H", and the difference is outputted to SMDP(Fig.14).

If the cycle of VCO/2 signal is put as "T" and it is put as "/WP" during a "H" period of PBFR, it outputs "H" to SMSD terminal from the falling edge of PBFR to the (/WP-278T) x 32, and then, outputs "L" to the falling edge of the next PBFR. (Figure 7)

XPHSP-Mode

The XPHSP mode is the mode used in normal operation.

The LKFS signal made from frame sync block is to sampling which period is PBFR/ 16. If the sampling is "H", the Phase mode is performed, and if the sampling is eight of "L" continously, Speed-mode is performed automatically. The selection of peak hold period in Speed-mode and selection of bottom hold period and gain in Speed/ Hspeed-mode is determined by CNTL-W register.

VPHSP-Mode

The VPHSP mode is the mode used for rough servo control. It uses VCO instead of X-tal in the EFM pattern test. When the range of VCO center changes, VCO is easily locked because the rotation of a spindle motor changes in the same direction.

Stop-Mode

This mode stops the spindle motor.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	L

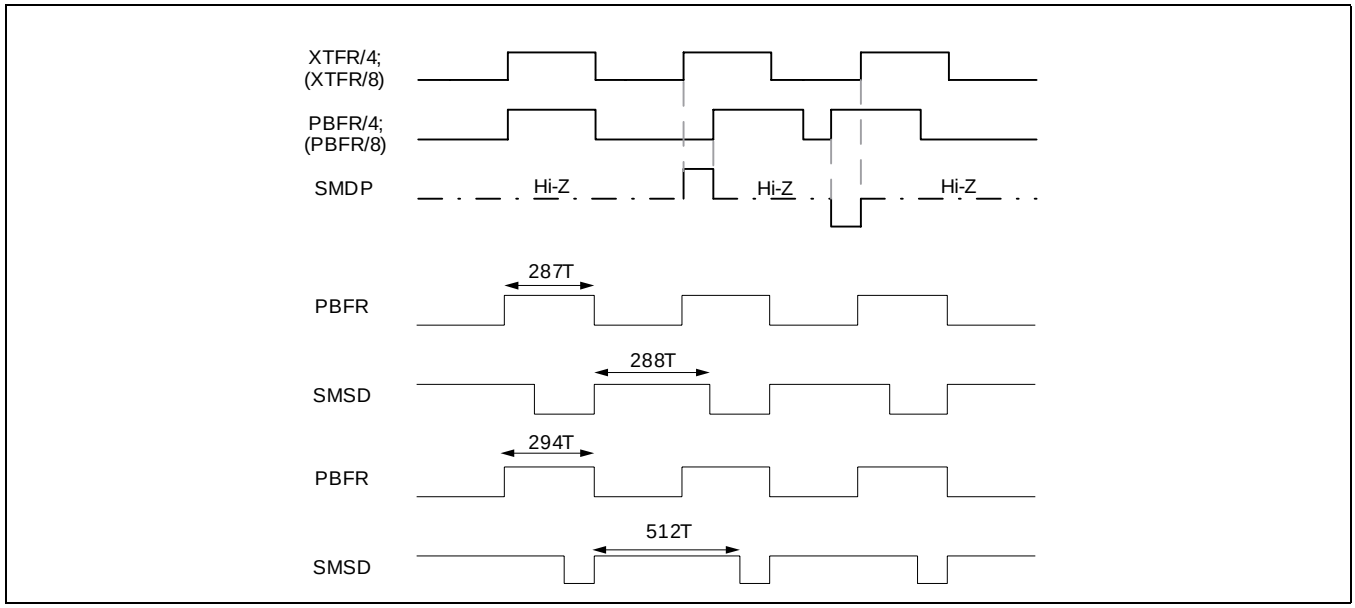


Figure 7. SMSD, SMDP Output Timing Diagram

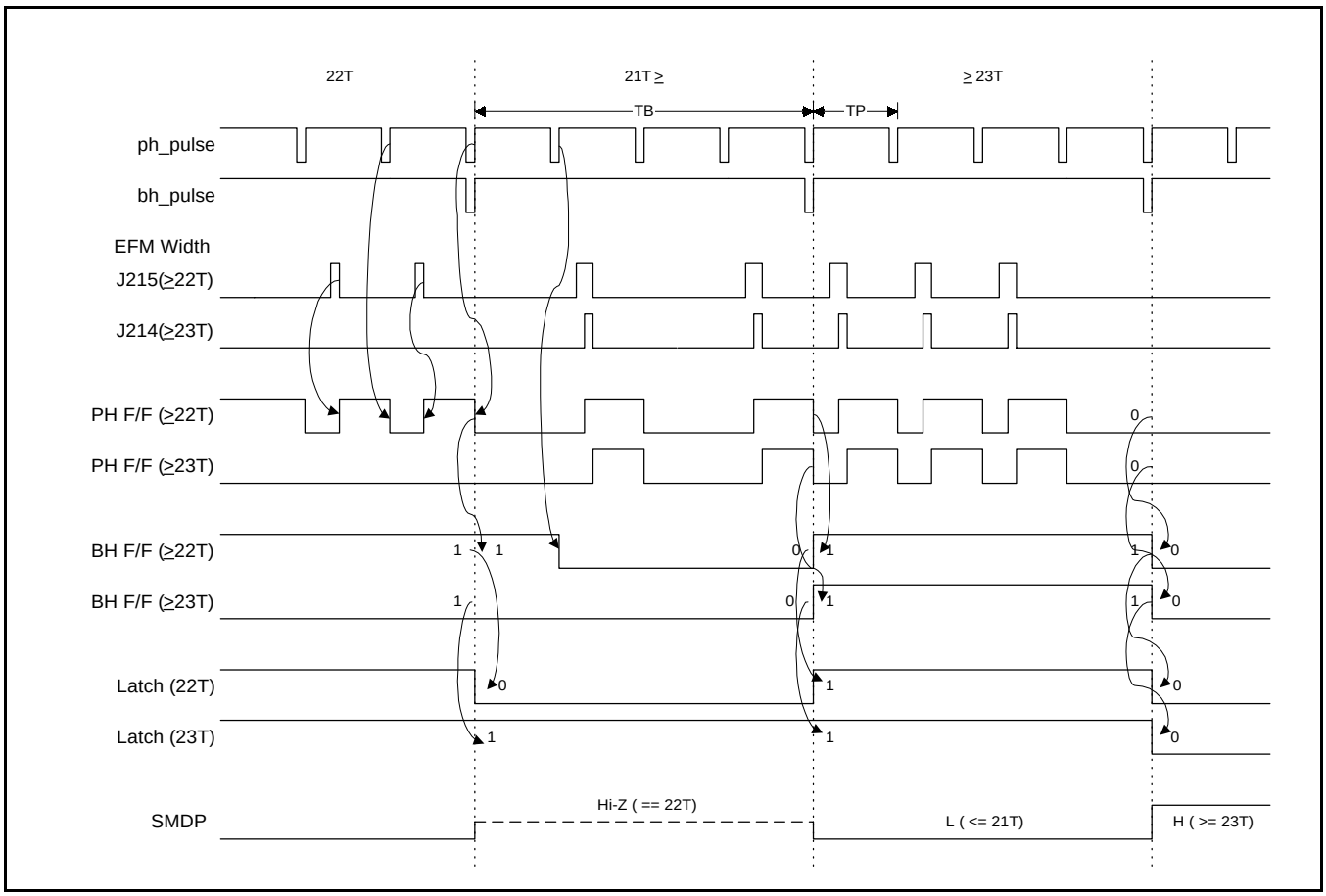


Figure 8. SMDP Output When The Gain is High in Speed-mode

DIGITAL FILTER

The S5L9284E has a built-in FIR (Finite Impulse Response) digital filter.
This digital filter consists of 8fs over sampling filter.

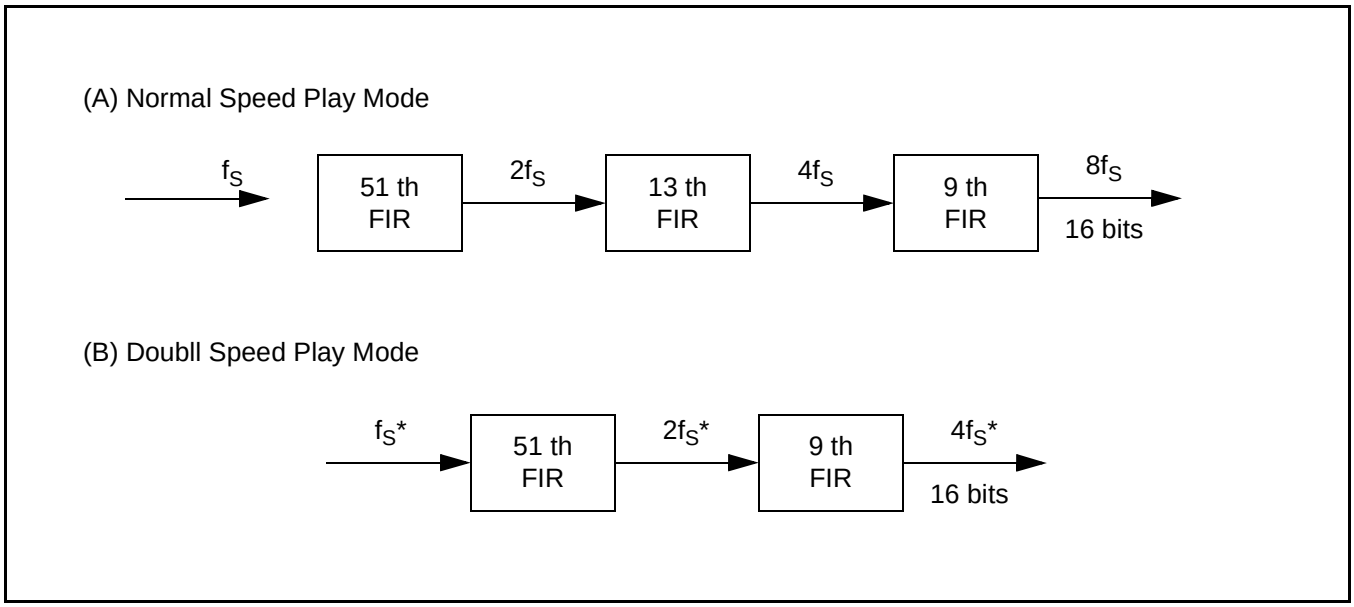


Figure 9. Digital Filter Block Diagram

FILTER CHARACTERISTIC

Ripple in passband : within ± 0.5dB

Attenuation in stopband: below -42dB

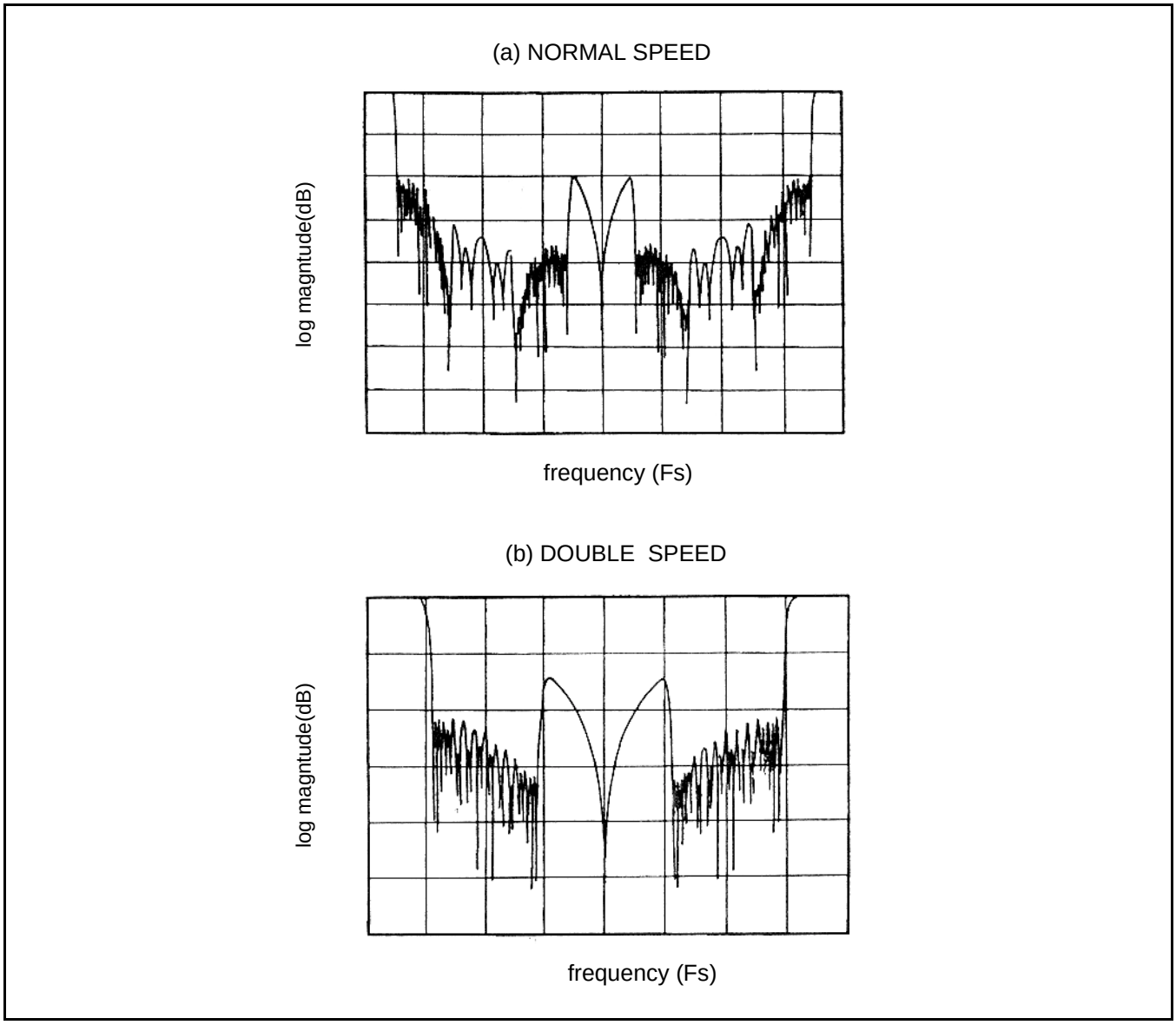


Figure 10. Filter Characteristic Curve

DIGITAL AUDIO OUT

This block serially outputs 2-channel and 16-bit data with the digital audio interface format as reference.

Digital audio interface format for CD

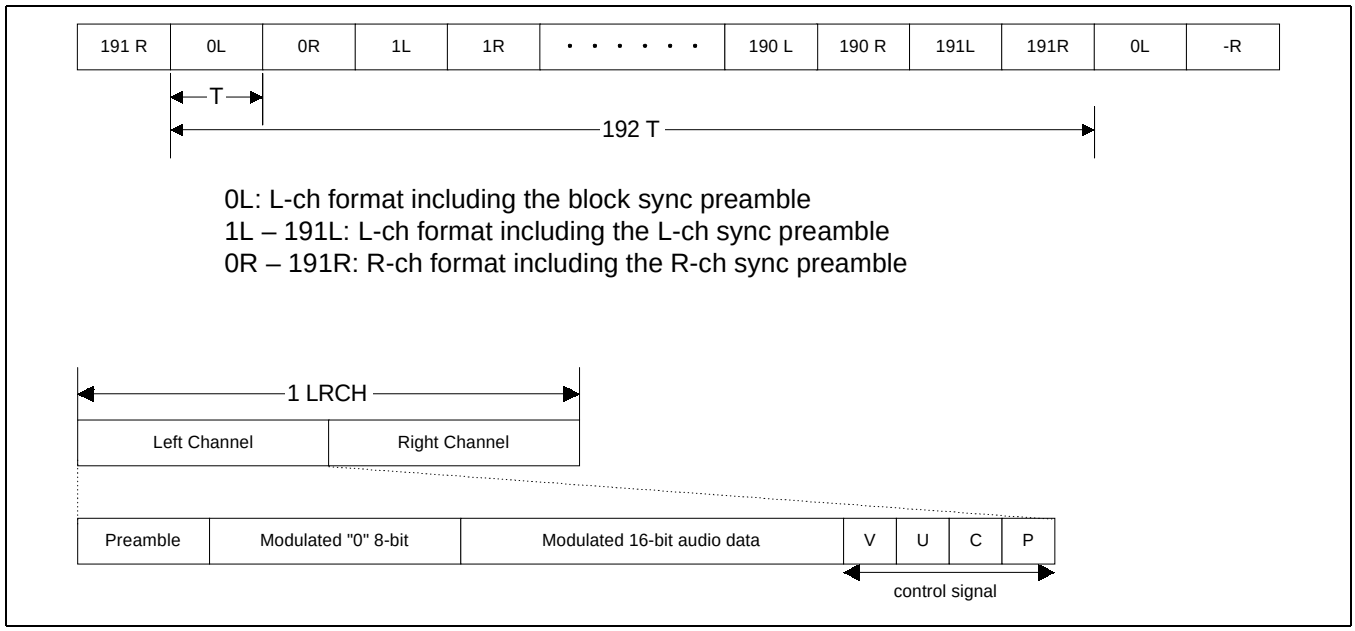


Figure 11. Digital Audio Out Format

Preamble

The Preamble is used to distinguish the datas block and L/R ch data

.

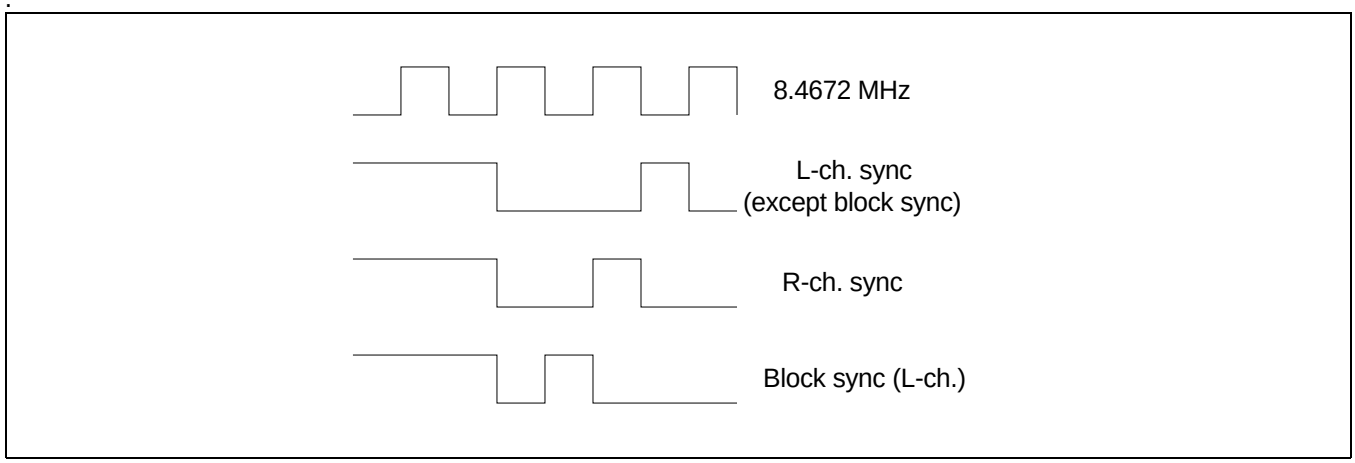


Figure 12. Preamble Signal

Control Signal

(1) Validity bit: shows the presence of error in 16-bit audio data: “H”=error, “L”=valid data

(2) User definable bit: subcode data out

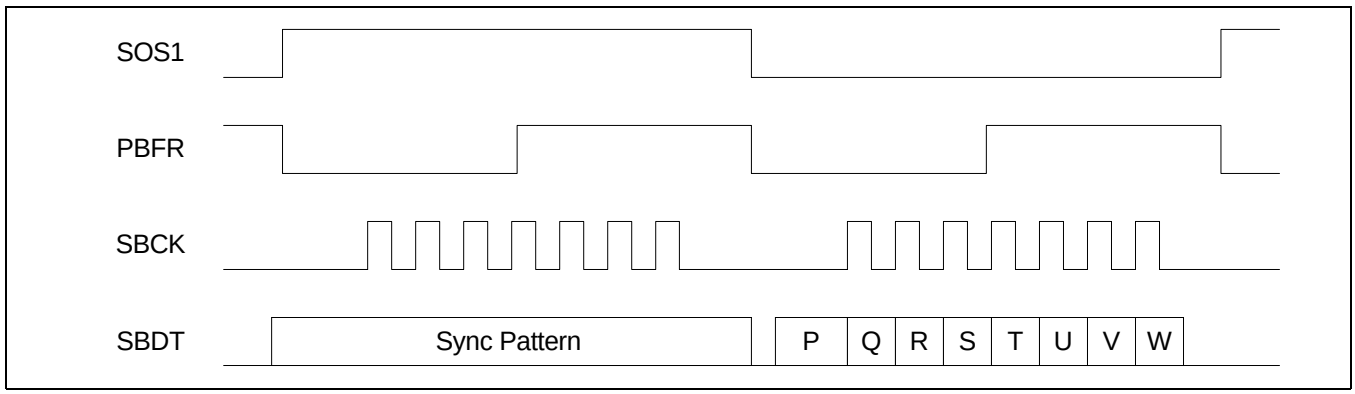


Figure 13. Digital Audio Data Out Timing Diagram

(3) Channel status bit: subcode-Qs upper 4-bit data output, shows number of channels, pre-emphasis, copy, CDP-category, etc.

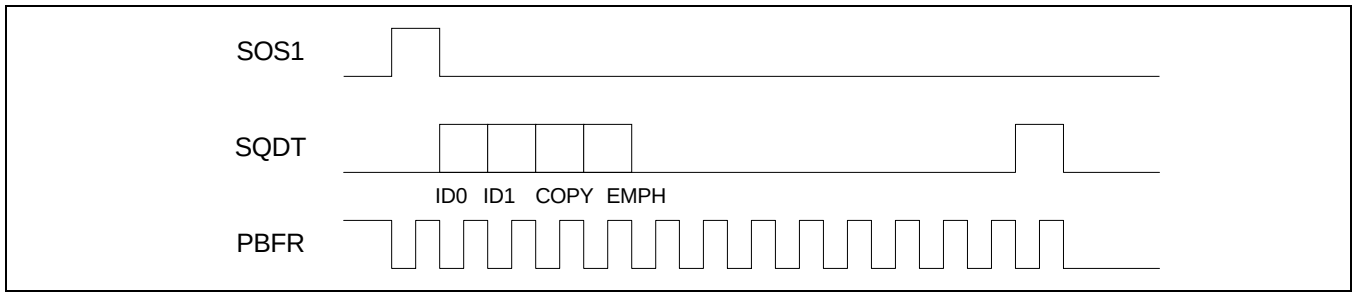


Figure 14. Channel Status Data Out Timing Diagram

(4) Parity Bit: makes even parity

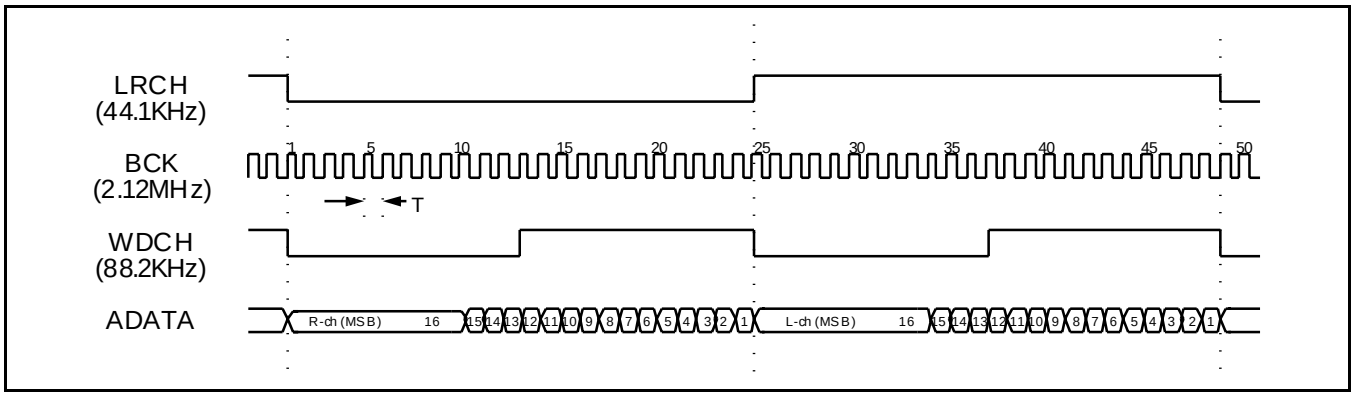


Figure 15. Digital Audio Data Out Timing Diagram 48bits/slot

DIGITAL PLL

This device contains Digital PLL in order to obtain the stable channel clock for demodulating EFM signal. The block diagram of Digital PLL is as follows.

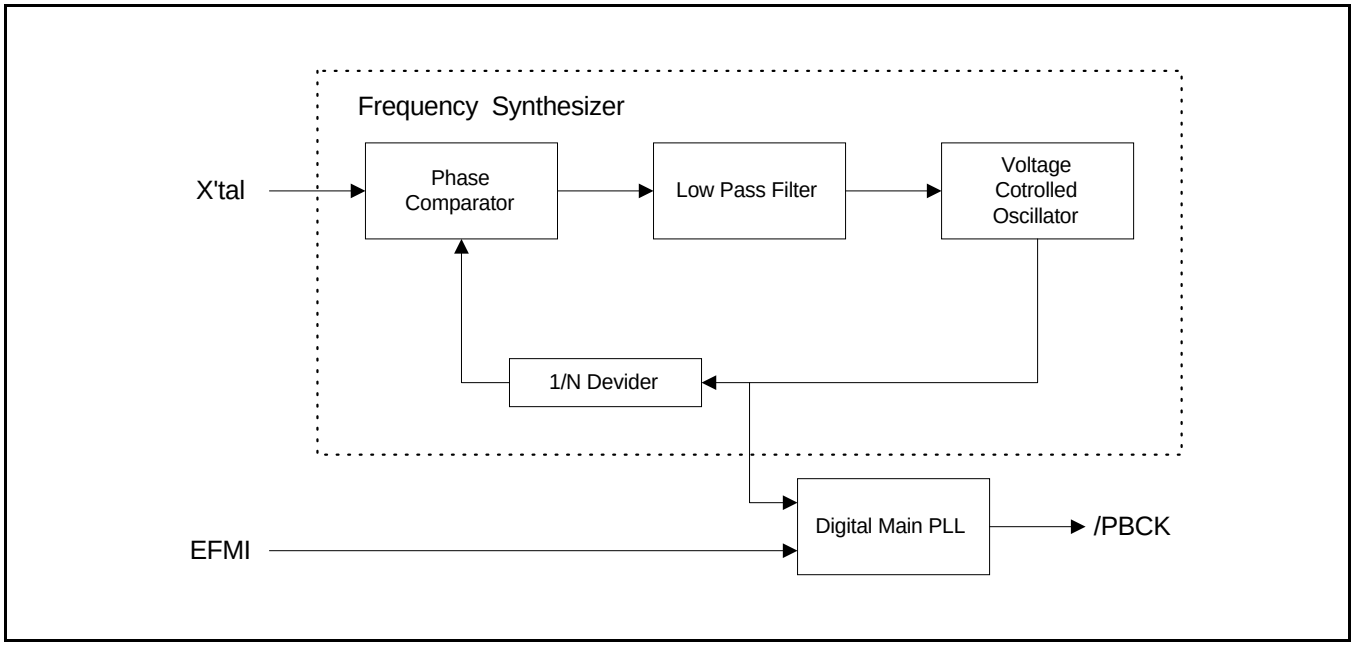


Figure 16. Digital PLL Circuit Diagram

D/A CONVERTER (DIGITAL TO ANALOG CONVERTER)

The S5L9284E has a built-in 16-bit D/A converter. Digital audio data is a 2's complement serial format (MSB sirst),

Vref Terminal

Vref, the reference voltage across a resister-ladder, is usually recommended with VrefH1=5V, VrefL1=0V. One way of avoiding an amplitude mismatching between the Vref and OP AMP input connected to the output of D/A converter is to reduce the analog output amplitude with VrefH2=5V and VrefL2=0V (At this time about 100µF capacitor should be connected from VreH1 and VrefL1 to GND). By the effect of built-in RH and RL with this choice, the maximum analog output amplitude result in a narrow range of about 1.5 ~ 3.5V for 0dB playback.

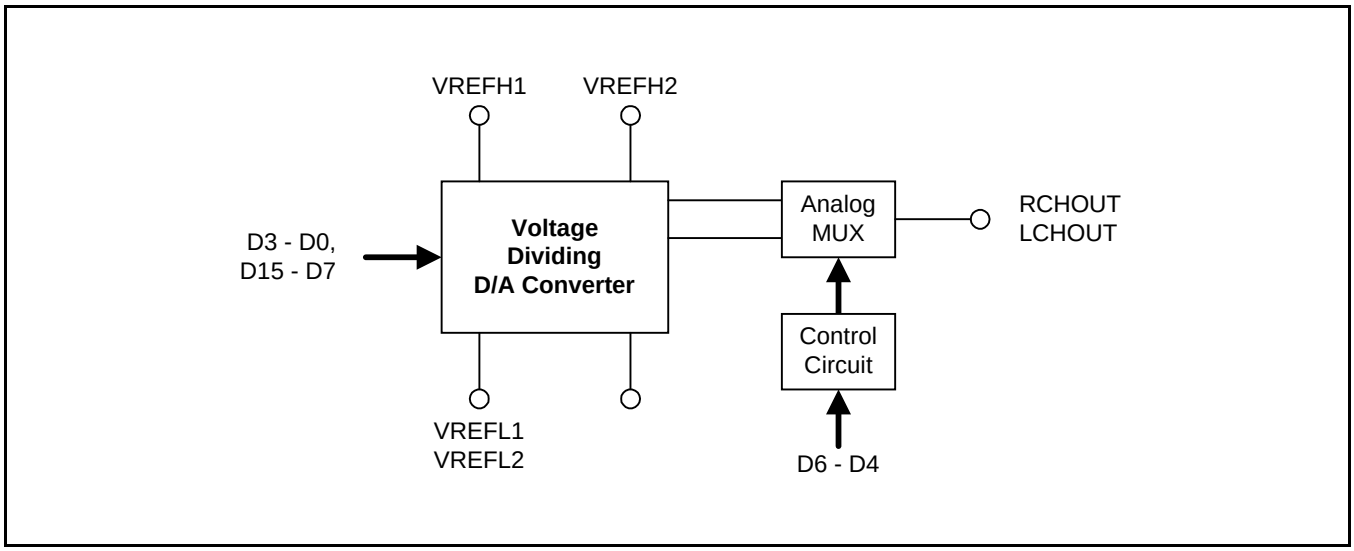


Figure 17. Vref Relation Circuit

D/A Converter Electrical Characteristic

The D/A Converter electrical characteristic built in S5L9826F01 is as follows.

(V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C)

Characteristics	Symbol	Test Conditon	MIN	TYP	MAX	Unit
Total Harmonic Distortion	THD	Data=1kHz, 0dB	–	–	0.08	%
Signal to Noise Ratio	S/N	V_{DD}=4.5V Data=1kHz, 0dB	–	92	–	dB
Cross-Talk	CT	Data=1kHz, 0dB	–	–85	–	dB

DIGITAL DE-EMPHASIS

The Emphasis/De-Emphasis circuit is used for improving S/N ration by decreasing high frequency noise in case of the frequency characteristic of signal not being changed.

The digital de-emphasis circuit, which can de-emphasise the signal emphasised on disc, is built-in S5L9826F01, and the frequency characteristic is as follows.

Frequency Characteristic of De-emphasis Circuit

Frequency	Characteristic
1KHz	-0.51dB
5KHz	-4.5dB
10KHz	-7.59dB
20KHz	-9.5dB

ESP INTERFACE BLOCK

INTRODUCTION

Because the location of normal table CD Player used in family is fixed, it is possible to play music stabilitable when the degree of damage on disc is in limit range.

But in now, it is general that user can hear music when moving by Walkman-CD Player. In this case, if user has been shocked suddenly, it often happens that music playing is unstable.

On this, the ESP interface block is added to S5L9826F01 for realizing the function of Anti-shock.
The application circuit of using NPC anti-shock memory controller IC SM5859AF and S5L9826F01 is as follows.

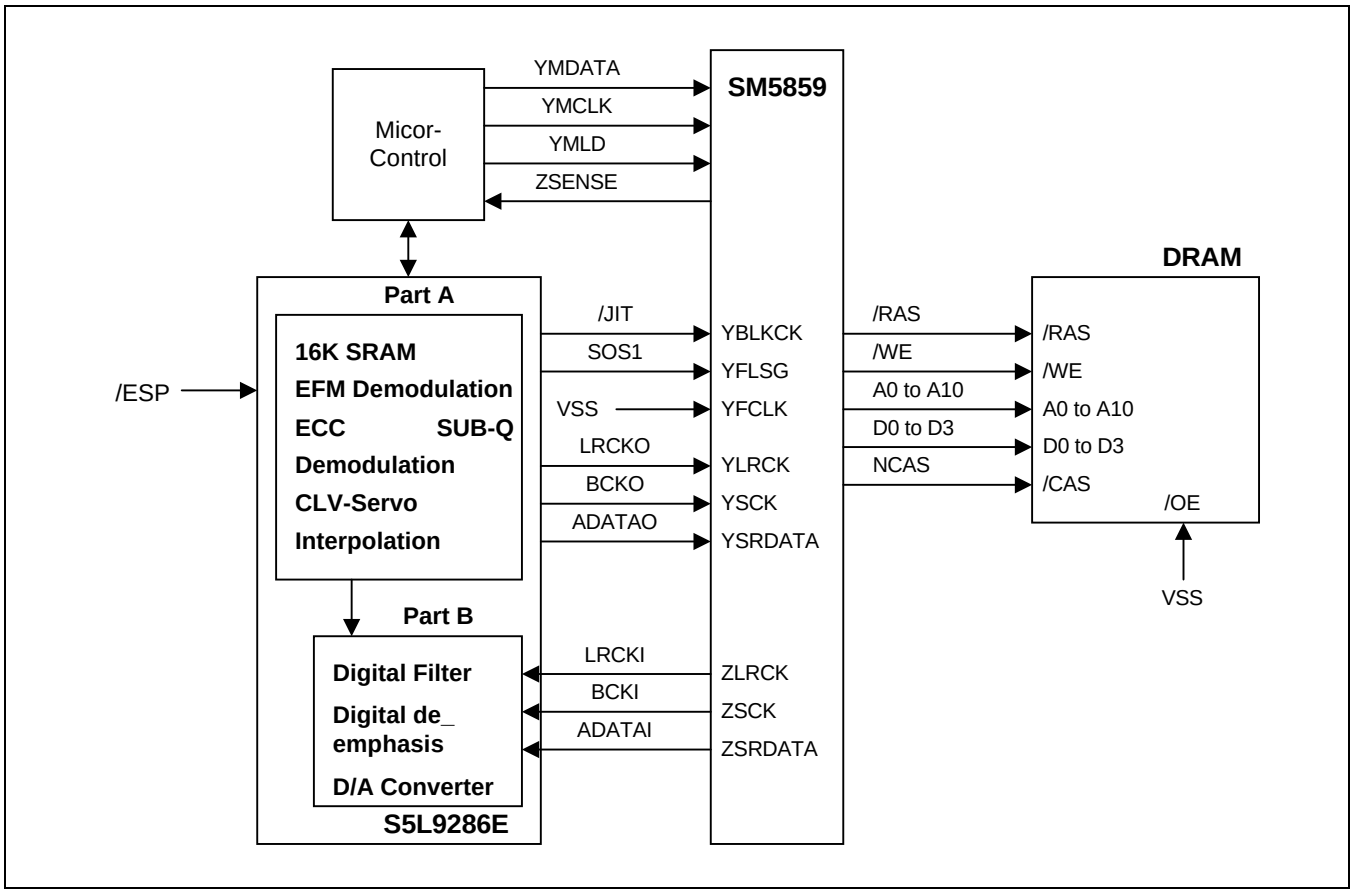


Figure 18. ESP Interface Application

The operation of S5L9826F01 is different when normal operation and forming anti- shock function with external ESP IC. From Figure19, the operation of part B composed by Digital Filter, Digital de-emphasis and 16-bit D/A Converter in S5L9826F01 and part A except part B is separated. When anti-shock function is used in case of /ESP Pin being "L", part A block operates in double speed and part B block operates in normal speed.

That is, after EFM Demodulation, Error Correction and Interpolation block operation in double speed, audio data is inputted to ESP IC which is the anti-shock memory controller. Audio data received by ESP IC is saved in external memory and then inputted to S5L9284E. In part B of S5L9826F01, the data is dealed with in normal speed and then outputted .

The anti-shock function is not used in case of /ESP terminal being "H".

The interface timing diagram of ESP IC is as follows.

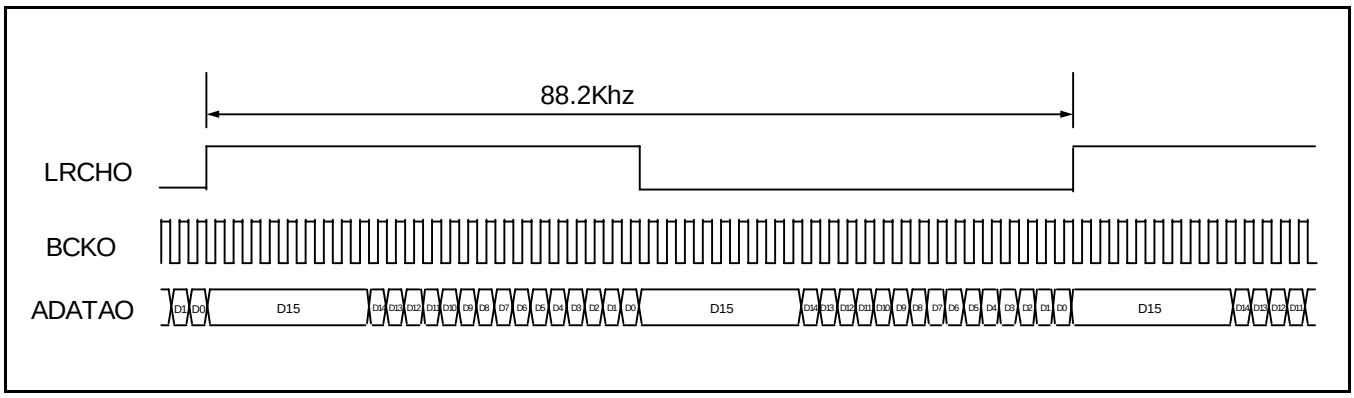


Figure 19. Timing Chart of Signal Output to ESP IC

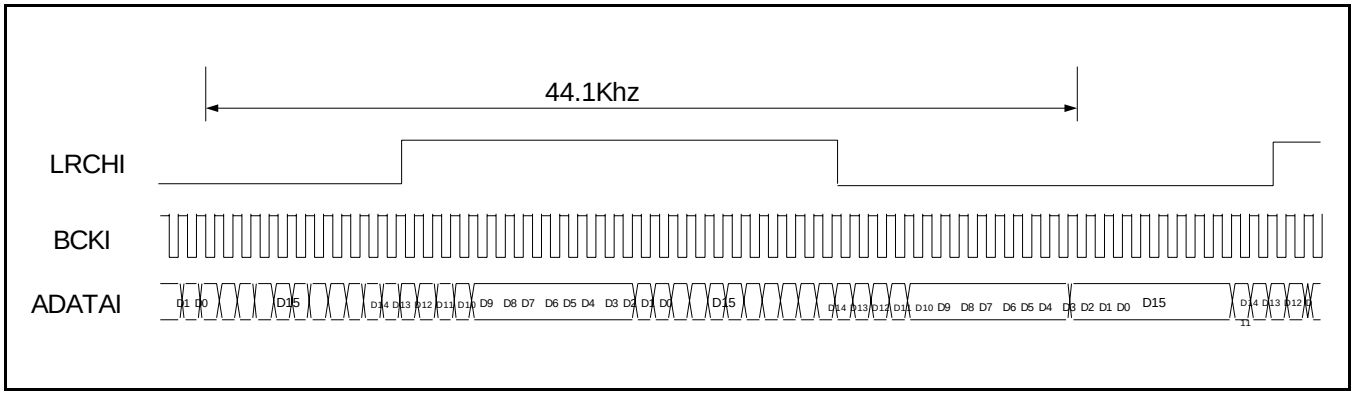


Figure 20. Timing Chart of Signal ESP IC Outpu to DSP

APPLICATION INFORMATION

MICOM REGISTER

The S5L9826F01 uses the exactly same MICOM command as S5L9282E (DSP+DAC) except one address addition.

ADRESS: $88

DATA: D1(DEEM)

H: When Internal Digital De-emphasis circuit is used.
L: When External Analog De-emphasis circuit is used.

D1 bit is cleared 'L' by Reset.
During fast search, for example forward or backward, MICOM must order attenuation to DSP IC.
If MICOM dosen't order attenuation to DSP, the DSP IC may cause malfunction of Erasuer correction during fast search.

ESP PART

If ESP IC is not used, you must connect follow pins to GND.

- LRCHI
- ADATAI
- BCKI

PACKAGE DIMENSION