Precision Supply-Voltage Monitor and Reset Controller With a Watchdog Timer and 4k-bit Microwire Memory

FEATURES

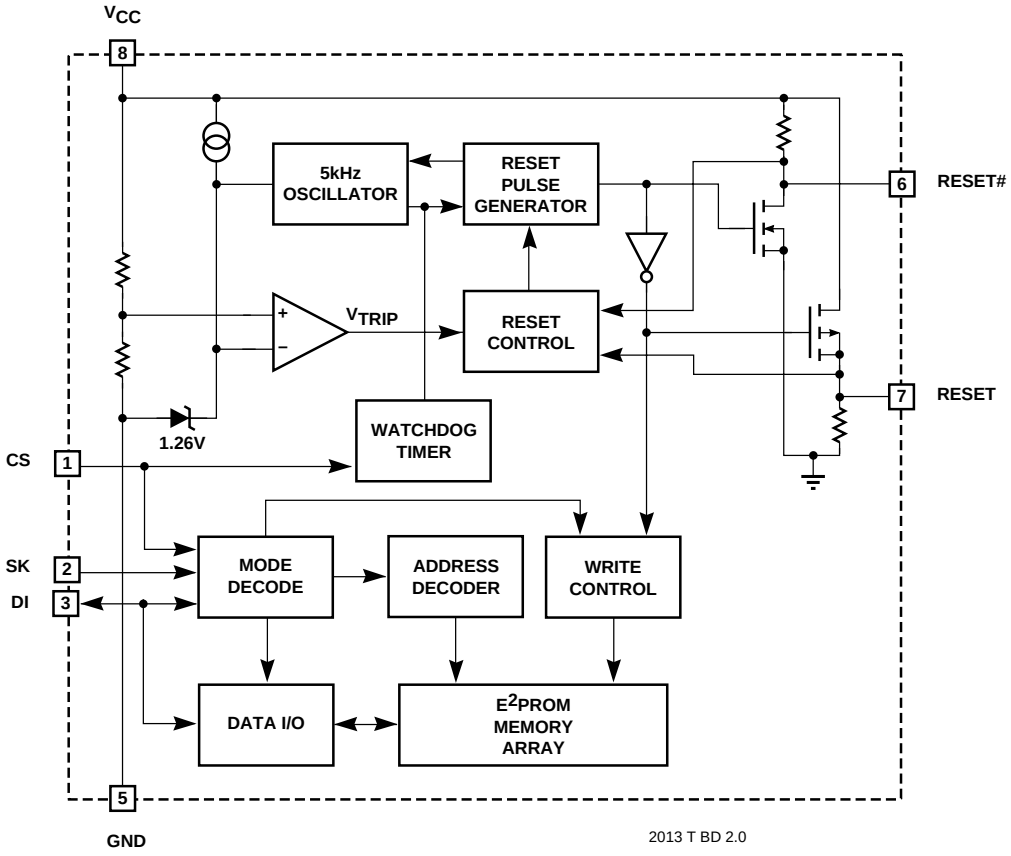
- **Precision Monitor & RESET Controller**
  - **— RESET and RESET# Outputs**
  - **— Guaranteed RESET Assertion to V_{CC} = 1V**
  - **— 200ms Reset Pulse Width**
  - **— Internal 1.26V Reference with ±1% Accuracy**
  - **— ZERO External Components Required**
- **Watchdog Timer**
  - **— Nominal 1.6 Second Time-out Period**
  - **— Reset by Any Transition of CS**
- **Memory**
  - **— 4K-bit Microwire Memory**
  - **— S93WD662**
    - **– Internally Ties ORG Low**
    - **– 100% Compatible With all 8-bit Implementations**
    - **– Sixteen Byte Page Write Capability**
  - **— S93WD663**
    - **– Internally Ties ORG High**
    - **– 100% Compatible With all 16-bit Implementations**
    - **– Eight Word Page Write Capability**

OVERVIEW

The S93WD662 and S93WD663 are precision power supervisory circuits providing both active high and active low reset outputs. Both devices incorporate a watchdog timer with a nominal time-out value of 1.6 seconds.

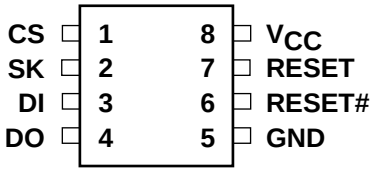
Both devices have 4k-bits of E^2PROM memory that is accessible via the industry standard microwire bus. The S93WD662 is configured with an internal ORG pin tied low providing a 8-bit byte organization and the S93WD663 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93WD662 and S93WD663 have page write capability. The devices are designed for a minimum 100,000 program/erase cycles and have data retention in excess of 100 years.

BLOCK DIAGRAM



PIN CONFIGURATION

8-Pin SOIC



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PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.7 to 6.0V Power Supply
GND	Ground
RESET/RESET#	RESET I/O

DEVICE OPERATION

APPLICATIONS

The S93WD662/WD663 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable.

RESET CONTROLLER DESCRIPTION

The S93WD662/WD663 provides a precision reset controller that ensures correct system operation during brownout and power-up/-down conditions. It is configured with two open drain reset outputs: pin 7 is an active high output and pin 6 is an active low output.

During power-up, the reset outputs remain active until V_{CC} reaches the V_{TRIP} threshold. The outputs will continue to be driven for approximately 200ms after reaching V_{TRIP}. The reset outputs will be valid so long as V_{CC} is $\geq$ 1.0V. During power-down, the reset outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The reset pins are I/Os; therefore, the S93WD662/WD663 can act as a stabilization circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset time-out after detecting a low to high transition and the RESET# input will initiate a reset time-out after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a debounce/reset extender circuit.

It should be noted the reset outputs are open drain. When used as outputs driving a circuit they need to be either tied high (RESET#) or tied to ground (RESET) through the use of pull-up or pull-down resistors. Refer to the applications aid section for help in determining the value of resistor to be used. Internally these pins are weakly pulled up (RESET#) and pulled down (RESET). If the signals are not being used the pins may be left unconnected.

WATCHDOG TIMER DESCRIPTION

The S93WD662/WD663 has a watchdog timer with a nominal time-out period of 1.6 seconds. Whenever the watchdog times out, it will generate a reset output to both pins 6 and 7. The watchdog timer is reset by any transition on CS.

The watchdog timer will be held in a reset state during power-on while V_{CC} is less than V_{TRIP}. Once V_{CC} exceeds V_{TRIP} the watchdog will continue to be held in a reset state for the t_{PURST} period. After t_{PURST} it will be released and the timer will begin operation. If either reset input is asserted the watchdog timer will be reset and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

GENERAL OPERATION

The S93WD662/WD663 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The S93WD663 is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The S93WD662 is organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. See the Applications Aid section for detailed use of the ready busy status.

The format for all instructions is: one start bit; two op code bits and either eight (x16) or nine (x8) address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93WD662/WD663 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93WD662/WD663 can be

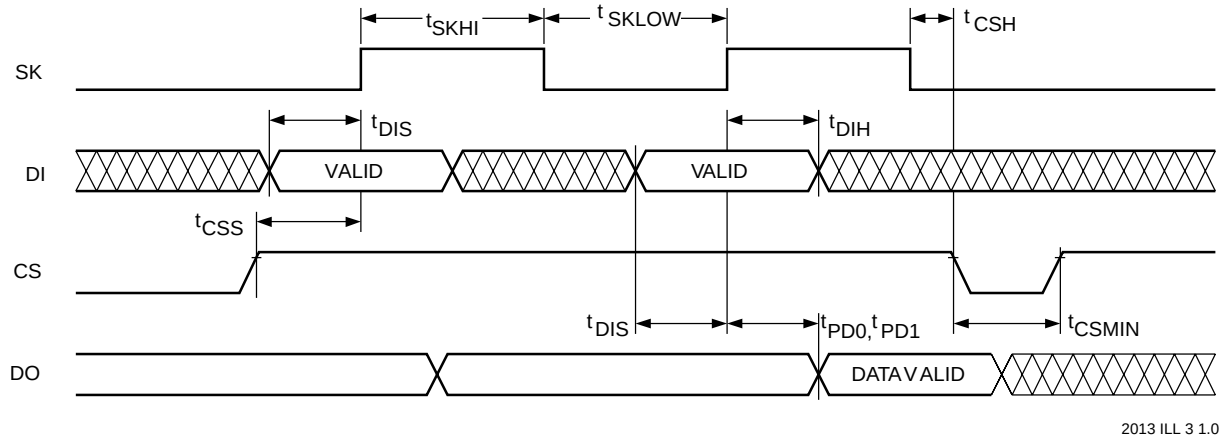

Figure 1. Sychronous Data Timing

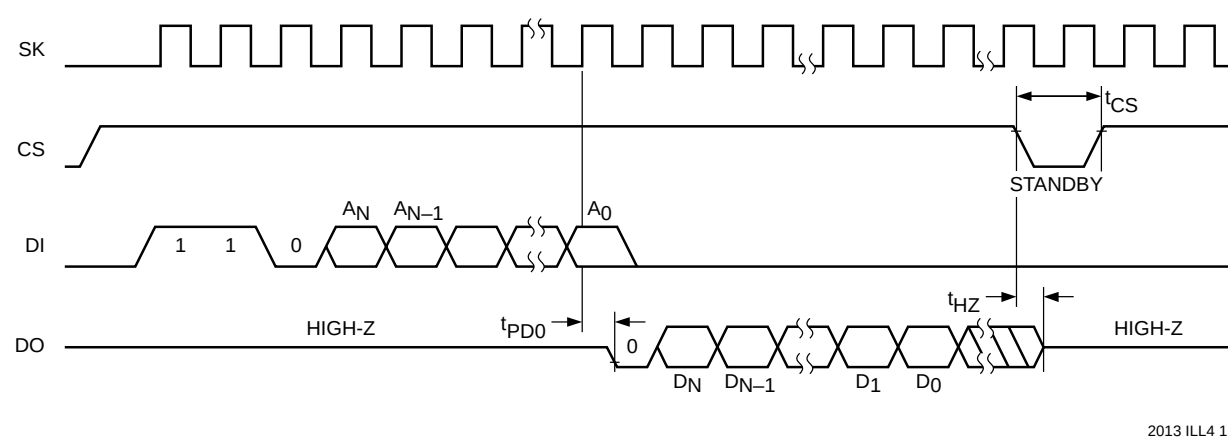

Figure 2. Read Instruction Timing

determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The S93WD662/WD663 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93WD662/WD663 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Page Write

93WD662 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 9-bit byte address immediately followed by the first byte of data to be written. The host can then continue clocking in 8-bit bytes of data with each byte to be written to the next higher address. Internally the address pointer is incremented after receiving each group of eight clocks; however, once the address counter reaches x xxxx 1111 it will roll over to x xxxx 0000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

93WD663 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 8-bit byte address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word to be written to the next higher address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxxx x111 it will roll over to xxxx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S93WD662/WD663 will output data from the next higher address location. The S93WD662/WD663 will continue incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. . CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.

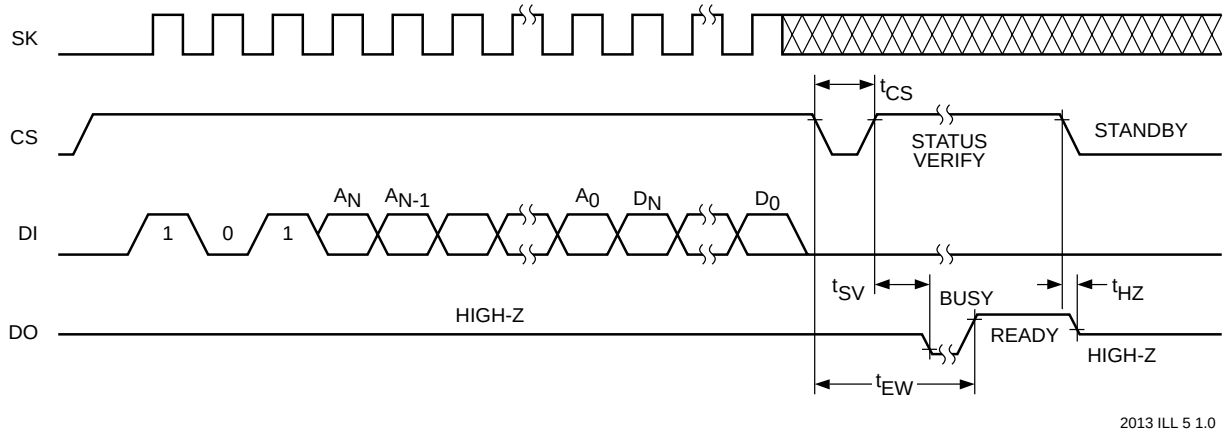

Figure 3. Write Instruction Timing

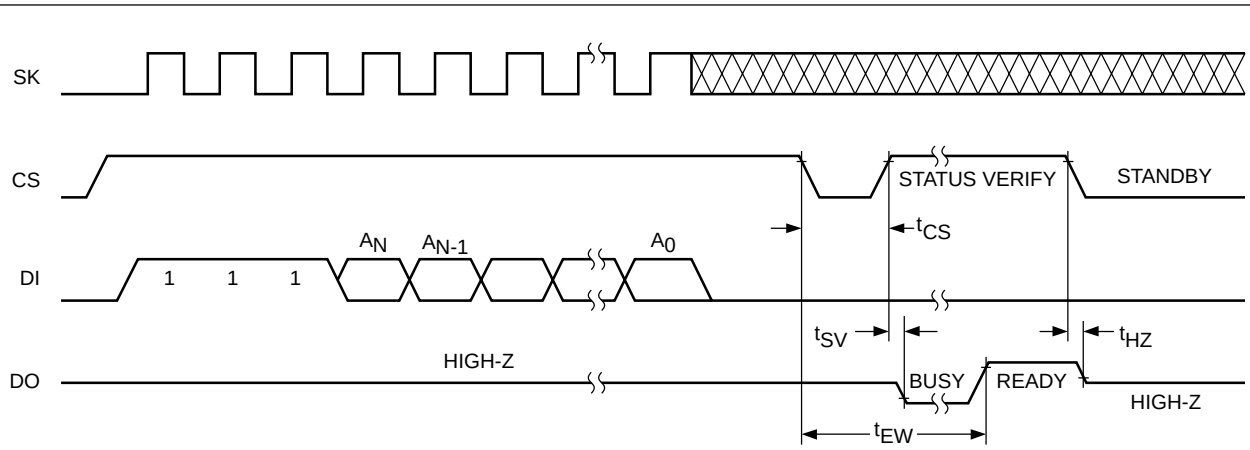

Figure 4. Erase Instruction Timing

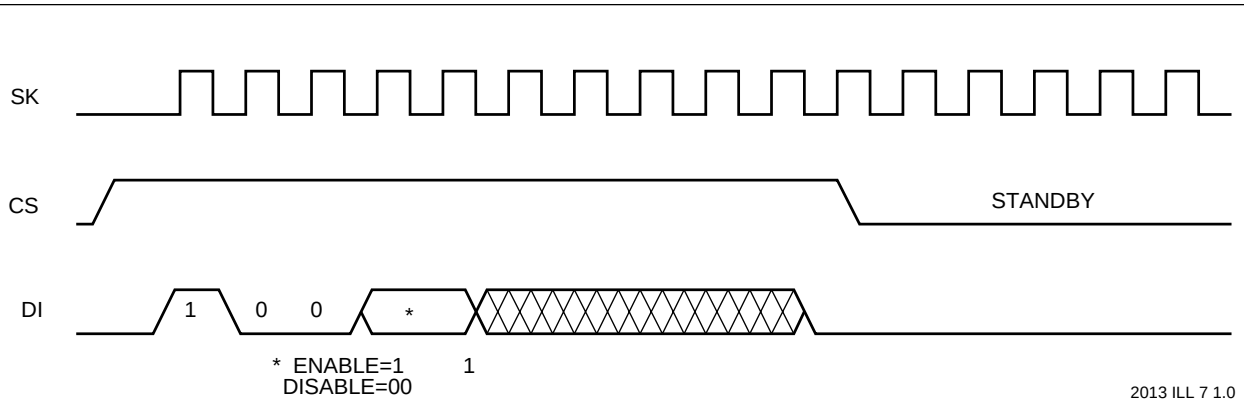

Figure 5. EWEN/EWDS Instruction Timing

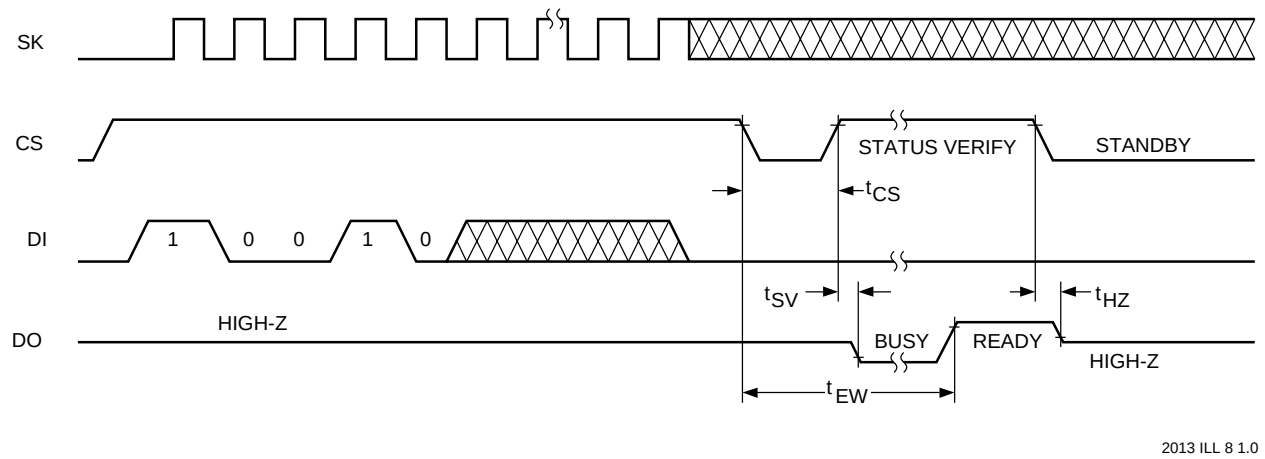

Figure 6. ERAL Instruction Timing

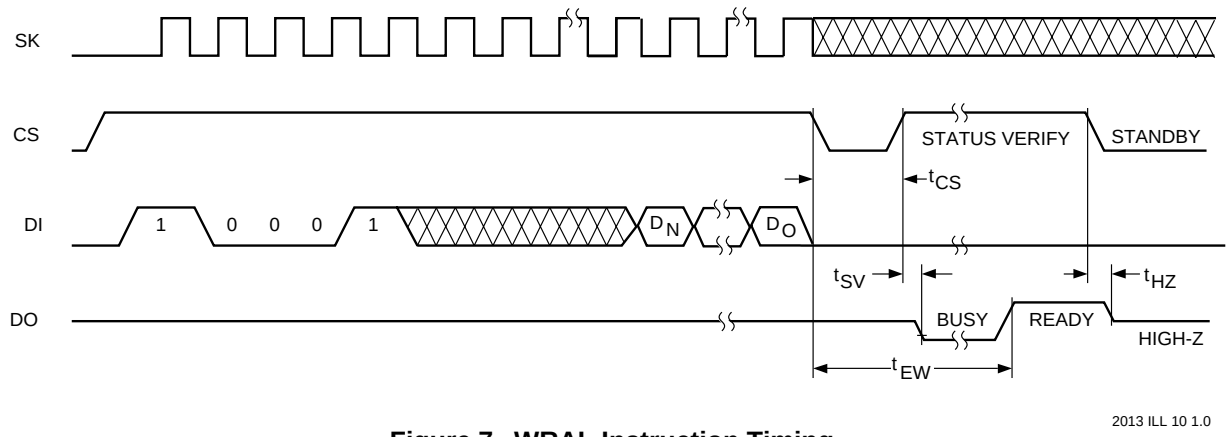

Figure 7. WRAL Instruction Timing

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8–A0	A7–A0			Read Address AN–A0
ERASE	1	11	A8–A0	A7–A0			Clear Address AN–A0
WRITE	1	01	A8–A0	A7–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	00	11xxx xxxx	11xxx xxx			Write Enable
EWDS	1	00	00xxx xxxx	00xxx xxx			Write Disable
ERAL	1	00	10xxx xxxx	10xxx xxx			Clear All Addresses
WRAL	1	00	01xxx xxxx	01xxx xxx	D7–D0	D15–D0	Write All Addresses

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V
V_{CC} with Respect to Ground ..... –2.0V to +7.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current(2) ..... 100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units
N_{END}(3)	Endurance	100,000		Cycles/Byte
T_{DR}(3)	Data Retention	100		Years
V_{ZAP}(3)	ESD Susceptibility	2000		Volts
I_{LTH}(3)(4)	Latch-Up	100		mA

D.C. OPERATING CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f_{SK} = 1MHz V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{SB}	Power Supply Current (Standby)			50	µA	CS = 0V Reset Outputs Open
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (Including ORG pin)			10	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V_{CC}+1	V V	4.5V-V_{CC}<5.5V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	0 V_{CC}X0.7		V_{CC}X0.2 V_{CC}+1	V V	1.8V-V_{CC}<2.7V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	2.4		0.4	V V	4.5V-V_{CC}<5.5V I_{OL} = 2.1mA I_{OH} = -400µA
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	V_{CC}-0.2		0.2	V V	1.8V-V_{CC}<2.7V I_{OL} = 1mA I_{OH} = -100µA

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Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C_{OUT}(1)	OUTPUT CAPACITANCE (DO)	5	pF	V_{OUT}=OV
C_{IN}(1)	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V_{IN}=OV

Note: 2013 PGM T4 1.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

		Limits					
		V_{CC}=2.7V-4.5V		V_{CC}=4.5V-5.5V			Test
SYMBOL	PARAMETER	Min.	Max.	Min.	Max.	UNITS	Conditions
t_{CSS}	CS Setup Time	100		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		ns	
t_{DIS}	DI Setup Time	200		100		ns	
t_{DIH}	DI Hold Time	200		100		ns	
t_{PD1}	Output Delay to 1		0.5		0.25	µs	
t_{PD0}	Output Delay to 0		0.5		0.25	µs	
t_{HZ}(1)	Output Delay to High-Z		200		100	ns	
t_{EW}	Program/Erase Pulse Width		10		10	ms	
t_{CSMIN}	Minimum CS Low Time	0.5		0.25		µs	
t_{SKHI}	Minimum SK High Time	0.5		0.25		µs	
t_{SKLOW}	Minimum SK Low Time	0.5		0.25		µs	
t_{SV}	Output Delay to Status Valid		0.5		0.25	µs	
SK_{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

Note: 2013 PGM T6 1.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

		2.7		5 Volt-A		5 Volt-B		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{TRIP}	Reset Trip Point	2.55	2.7	4.25	4.5	4.50	4.75	V
t_{PURST}	Power-Up Reset Timeout	130	270	130	270	130	270	ms
t_{RPD}	V_{TRIP} to RESET Output Delay		5		5		5	µs
V_{RVALID}	RESET# Output Valid	1		1		1		V
t_{GLITCH}	Glitch Reject Pulse Width		30		30		30	ns
V_{OLRS}	RESET Output Low Voltage I_{OL}=1mA		0.4		0.4		0.4	V
V_{OHRS}	RESET# Output High I_{OH}	V_{CC}-.75		V_{CC}-.75		V_{CC}-.75		V

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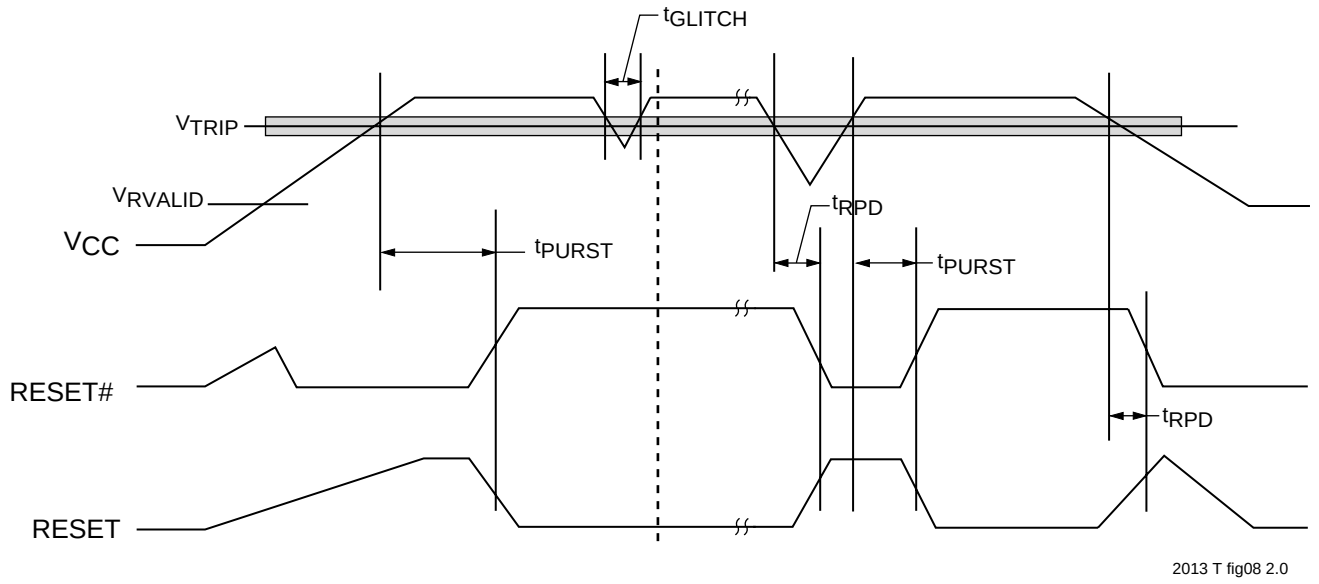
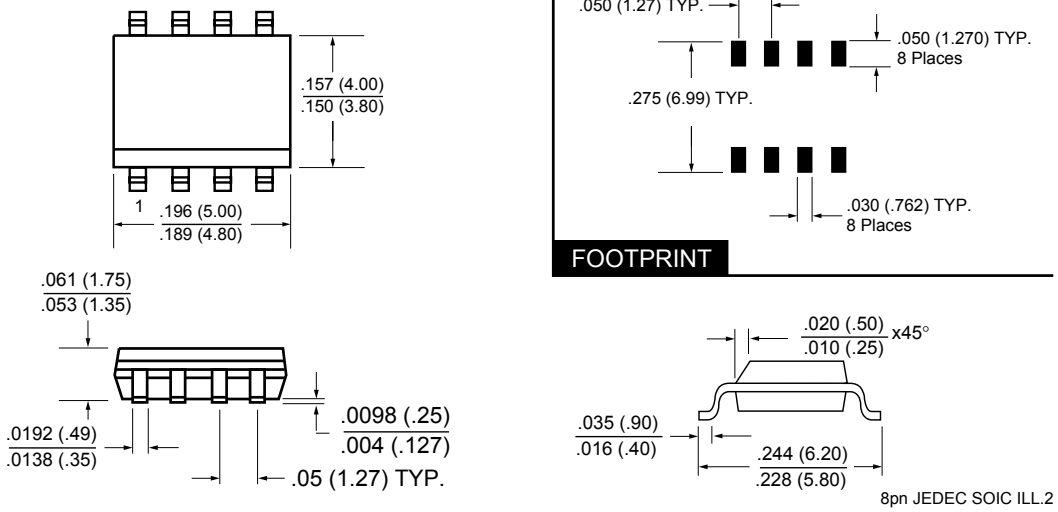


Figure 8. RESET Timing Diagram

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)

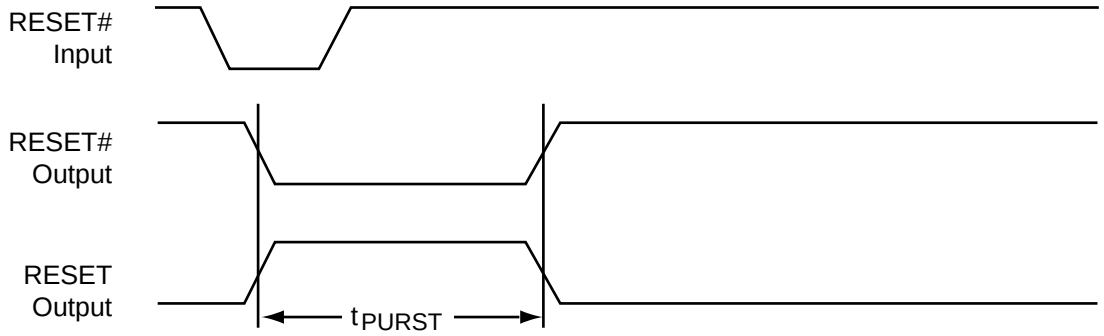


8pn JEDEC SOIC ILL.2

Applications Aid

Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S93WD662/WD663 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST}. The same reset output affect can be attained by using the active high reset input.



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When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET# Output Voltage	V_{OL}	V_{CC} = 1.0V, I_{OL}=100µA			0.3	V
		V_{CC} = 1.2V, I_{OL}=100µA			0.3	V
		V_{CC} = 3.0V, I_{OL}=500µA			0.3	V
		V_{CC} = 3.6V, I_{OL}=500µA			0.3	V
		V_{CC} = 4.5V, I_{OL}=750µA			0.3	V
RESET# Output Voltage	V_{OL}	V_{CC} = 1.0V, I_{OL}=100µA			0.4	V
		V_{CC} = 1.2V, I_{OL}=150µA			0.4	V
		V_{CC} = 3.0V, I_{OL}=750µA			0.4	V
		V_{CC} = 3.6V, I_{OL}=1mA			0.4	V
		V_{CC} = 4.5V, I_{OL}=1mA			0.4	V
RESET Output Voltage	V_{OH}	V_{CC} = 1.0V, I_{OH}=400µA	V_{CC}-0.75			V
		V_{CC} = 1.2V, I_{OH}=800µA	V_{CC}-0.75			V
		V_{CC} = 3.0V, I_{OH}=800µA	V_{CC}-0.5			V
		V_{CC} = 3.6V, I_{OH}=800µA	V_{CC}-0.5			V
		V_{CC} = 4.5V, I_{OH}=800µA	V_{CC}-0.5			V

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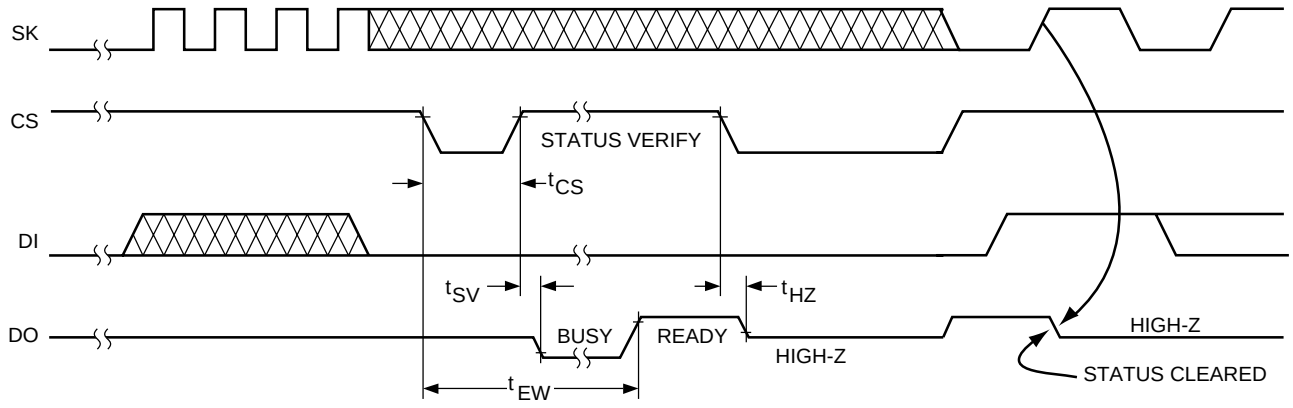
Ready/Busy Status

During the internal write operation the S93WD662/WD663 memory array is inaccessible. After starting the write operation (taking CS low) the host can implement a 10ms time-out routine or alternatively it can employ a polling routine that tests the state of the DO pin.

After starting the write, testing for the status is easily accomplished by taking CS high and testing the state of DO. If it is low the device is still busy with the internal write. If it is high the write operation has completed.

For the polling routine the host has the option of toggling CS for each test of DO, or it can place CS high and then intermittently test DO. SK is not required for any of these operations. Once the device is ready, it will continue to drive DO high whenever the S93WD662/WD663 is selected. The ready state of DO can be cleared by clocking in a start bit; this start bit can either be the beginning of a new command sequence or it can be a dummy start bit with CS returning low before the host issues a new command.



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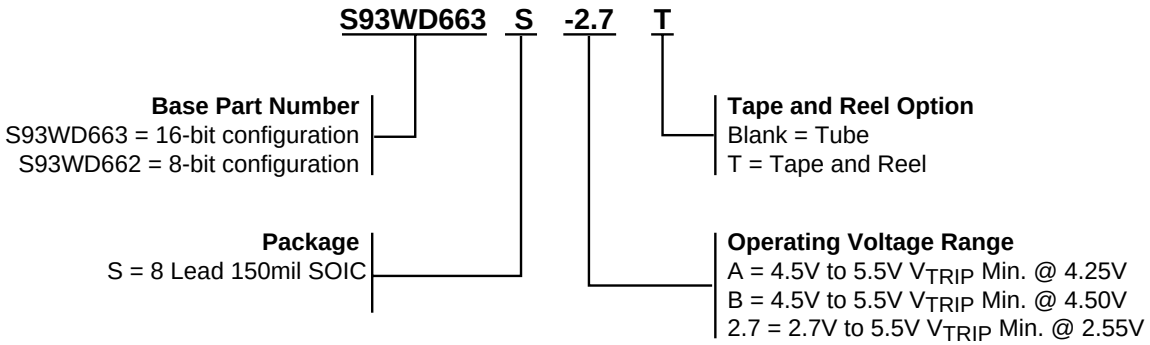
ORDERING INFORMATION



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