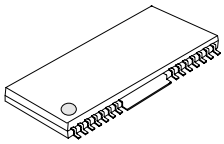
4-CH BTL DRIVER FOR CD PLAYER WITH 3.3V OUTPUT VOLTAGE

DESCRIPTION

The SA1469PH, an IC for CD players, has a 4-channel BTL driver, 3.3V regulator (attached PNP transistor required), standard operational amplifier, and internal reset output linked to an internal thermal shutdown circuit. The driver has gain adjustment input pins for each channel, allowing gain to be set to the desired value. Also, the internal level shift circuit helps reduce the number of attached components.



HSOP - 28-375-0.8

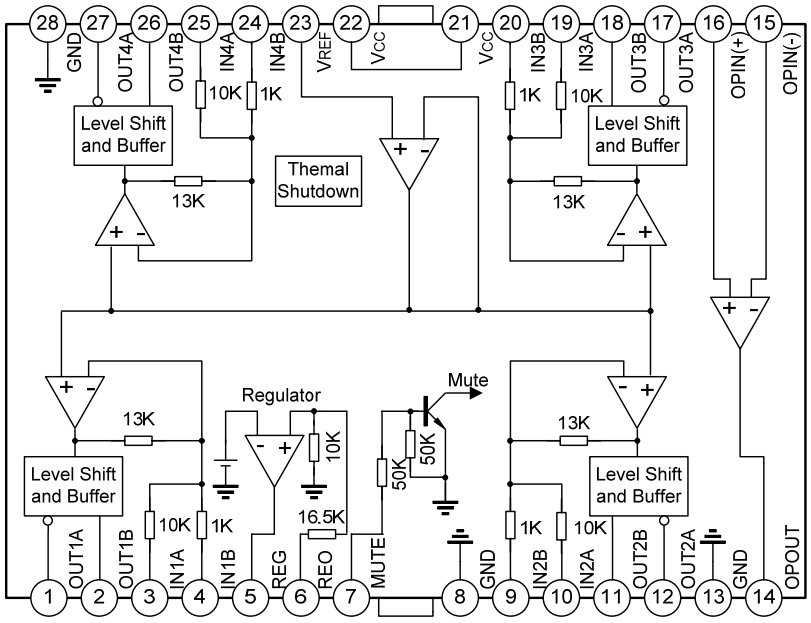
FEATURES

* 1-phase, full-wave, linear DC motor driver
* Gain is adjustable with an attached resistor.
* Internal standard operational amplifier.
* Internal 3.3V regulator. (required attached PNP transistor)
* Internal thermal shutdown circuit with hysteresis capabilities.

ORDERING INFORMATION

Device	Package
SA1469PH	HSOP-28-375-0.8

BLOCK DIAGRAM



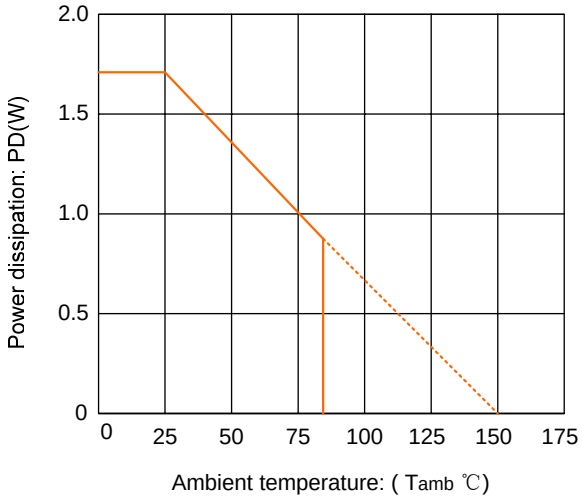
ABSOLUTE MAXIMUM RATING (T_{amb}=25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Power Dissipation	P_D	1.7(Note)	W
Operating Temperature	T_{opr}	-40~+85	°C
Storage Temperature	T_{stg}	-55~+150	°C
Maximum Output Current	I_{max}	1	A

Note: 1. When mounted on 76mm x 114mm x 1.57mm PCB (Phenolic resin material).

2. Power dissipation reduces 13.6mW / °C for using above T_{amb}=25 °C.

3. Do not exceed Pd and SOA (Safe Operating Area).



ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, V_{CC}=8.0V, unless otherwise specified)

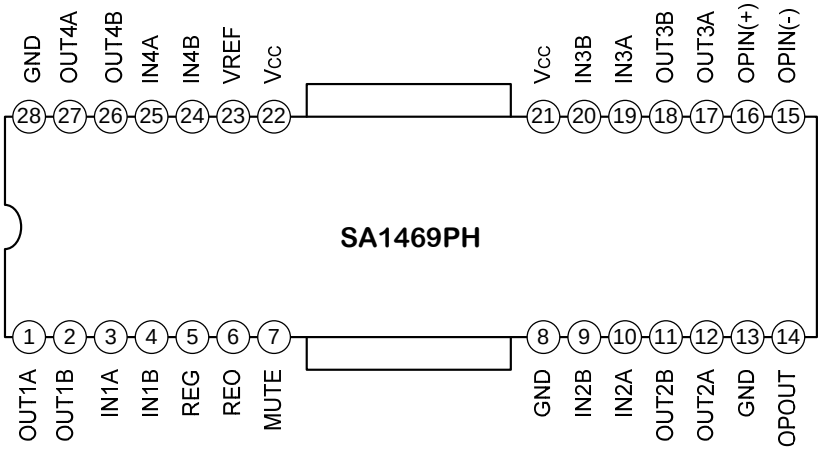
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
A REGULATOR PART						
Regulator Output Voltage	V_{REG}	I_L=100mA	3.13	3.3	3.47	V
Load Regulation	ΔV_{RL}	I_L=0mA to 200mA	-40.0	0	10.0	mV
Line Regulation	ΔV_{CC}	I_L=200mA, V_{CC}=6 to 9V	-10.0	0	20.0	mV
B DRIVER PART						
Quiescent Circuit Current	I_{CCQ}	V_I=0	5.5	9.5	13.5	mA
Input Offset Voltage	V_{OF}	-	-5.0	0	5.0	mV
Output Offset Voltage	V_{OO}	-	-30	0	30	mV
Maximum Sink Current	I_{SINK}	R_L=4Ω, V_{CC}	0.5	0.8	--	A
Maximum Source Current	I_{SOU}	R_L=4Ω, GND	0.5	0.8	--	A
Maximum Output Voltage	V_{OM}	V_I=2VRMS, 1kHz	2.5	3.0	--	V
Closed Loop Voltage Gain	A/F	V_I=0.1VRMS, 1kHz	7.0	8.0	9.0	Db
Ripple Rejection Ratio	R_R	V_I=-20dB, 120Hz	60.0	80.0	--	dB
Slew Rate	S_R	100Hz, squarewave	1.0	2.0	--	V/μs

(To be continued)

(Continued)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
C OP AMP						
Input Offset Voltage	V_{OF1}	-	-5.0	0	5.0	mV
Input Bias Current	I_{B1}	-	--	--	300	nA
High Level Output Voltage	V_{OH1}	-	6	-	-	V
Low Level Output Voltage	V_{OL1}	-	-	-	1.8	V
Output Sink Current	I_{SINK1}	R_L=50Ω, GND	10	40	-	mA
Output Source Current	$I_{SOURCE1}$	R_L=50Ω, V_{CC}	10	50	-	mA
Open Loop Voltage Gain	G_{VO1}	V_{IN}=-75dB, f=1kHz	65	78	-	dB
Ripple Rejection Ratio	R_{R1}	V_{IN}=-20dB, 120Hz	50	70	-	dB
Slew Rate	S_R	Square, V_{OUT}=2Vp-p, f=120kHz	0.5	1	-	V/μs
Common Mode Rejection Ratio	C_{MRR1}	V_{IN}=-20dB, 1kHz	70	84	-	dB

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OUT1A	O	Drive output
2	OUT1B	O	Drive output
3	IN1A	I	Drive input
4	IN1B	I	Drive input
5	REG		Regulator
6	REO	O	Regulator output
7	MUTE	I	Mute
8	GND	--	Ground

(To be continued)

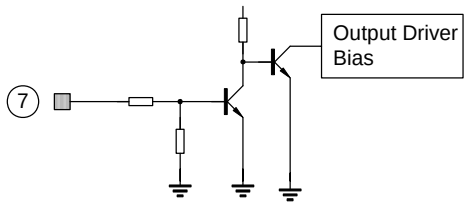
(Continued)

Pin No.	Symbol	I/O	Description
9	IN2B	I	Drive input
10	IN2A	I	Drive input
11	OUT2B	O	Drive output
12	OUT2A	O	Drive output
13	GND	--	Ground
14	OPOUT	O	Opamp output
15	OPIN (-)	I	Opamp input (-)
16	OPIN (+)	I	Opamp input (+)
17	OUT3A	O	Drive output
18	OUT3B	O	Drive output
19	IN3A	I	Drive input
20	IN3B	I	Drive input
21	Vcc	--	Supply voltage
22	Vcc	--	Supply voltage
23	VREF	I	2.5V bias voltage
24	IN4B	I	Drive input
25	IN4A	I	Drive input
26	OUT4B	O	Drive output
27	OUT4A	O	Drive output
28	GND	--	Ground

FUNCTIONAL DESCRIPTION

1. MUTE

Function	Mute	Operation conditions
Thermal shutdown	○	T≥175°C
External muting	○	V(mute)≤ 1.4V or open



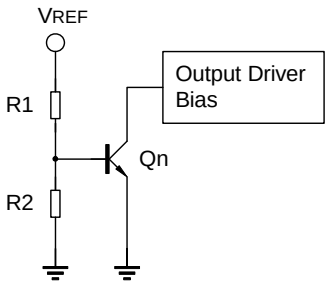
1) The circuit is muted during thermal shutdown and during the mute-on state.In each case, only the drivers are muted.

2) During mute, the output pins remain at the internal bias voltage, roughly (Vcc-Vf)/2.

3) When the mute pin # 7 is open or the voltage of the mute pin # 7 is below 0.5V, the mute circuit is activated so that the output circuit will be muted..

4) When the voltage of the mute pin is above 2V, the mute circuit is stopped and the output circuit is operated normally.
5) If the chip temperature rises above 175°C, then the TSD (Thermal Shutdown) circuit is activated and the output circuit is muted.

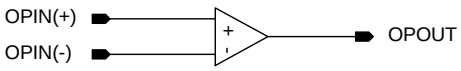
2. TSD (THERMAL SHUTDOWN)



1) The VREF is the output voltage of the band-gap-referenced biasing circuit and acts as the input voltage of the TSD circuit.
2) The base-emitter voltage of the TR, Qn is designed to turn-on at below voltage.
$V_{BE}=V_{REF} * R2/(R1+R2)=460mV$
3) When the chip temperature rises up to 175°C, then the turn-on voltage of the Qn would drop down to 460mV. (Hysteresis: 25°) and, the Qn would turn on so the output circuit will be muted.

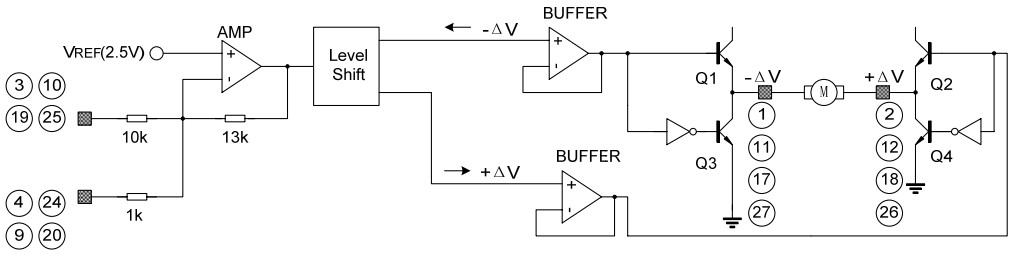
3. OP-AMP

OP-Amp is integrated in the IC for user convenuence.



Pins 14, 15 and 16 may be left open when the operational amplifier is not used.

4. DRIVER



1) The voltage, V_{REF}, is the reference voltage given by the BIAS voltage of the pin # 23.
2) The input signal through the pin # 3 is amplified by 13K/10K times and then fed to the level shift.
3) The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as +ΔV and -ΔV is fed into the driver buffer.
4) Driver buffer operates the power TR of the output stage according to the state of the input signal.
5) The output stage is the BTL driver and the motor is rotating in forward direction by operating TR Q1 and TR Q4. on the other hand, if TR Q2 and TR Q3 is operating, the motor is rotating in reverse direction.

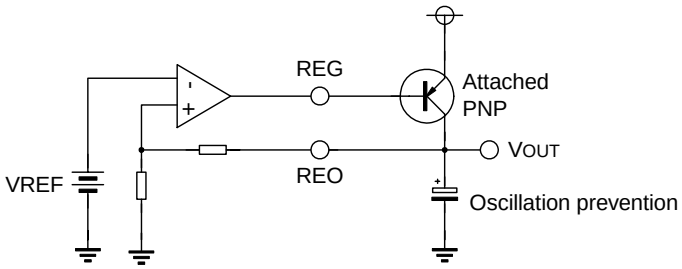
6) When the input voltage through the pin # 3 is below the VREF, then the direction of the motor in forward direction.
7) When the input voltage through the pin # 3 is above the VREF, then the direction of the motor in reverse direction.
8) If it is desired to change the gain, then the pin # 4 or # 24 can be used.

5. RADIATION FIN IS CONNECTING TO THE INTERNAL GND OF THE PACKAGE.

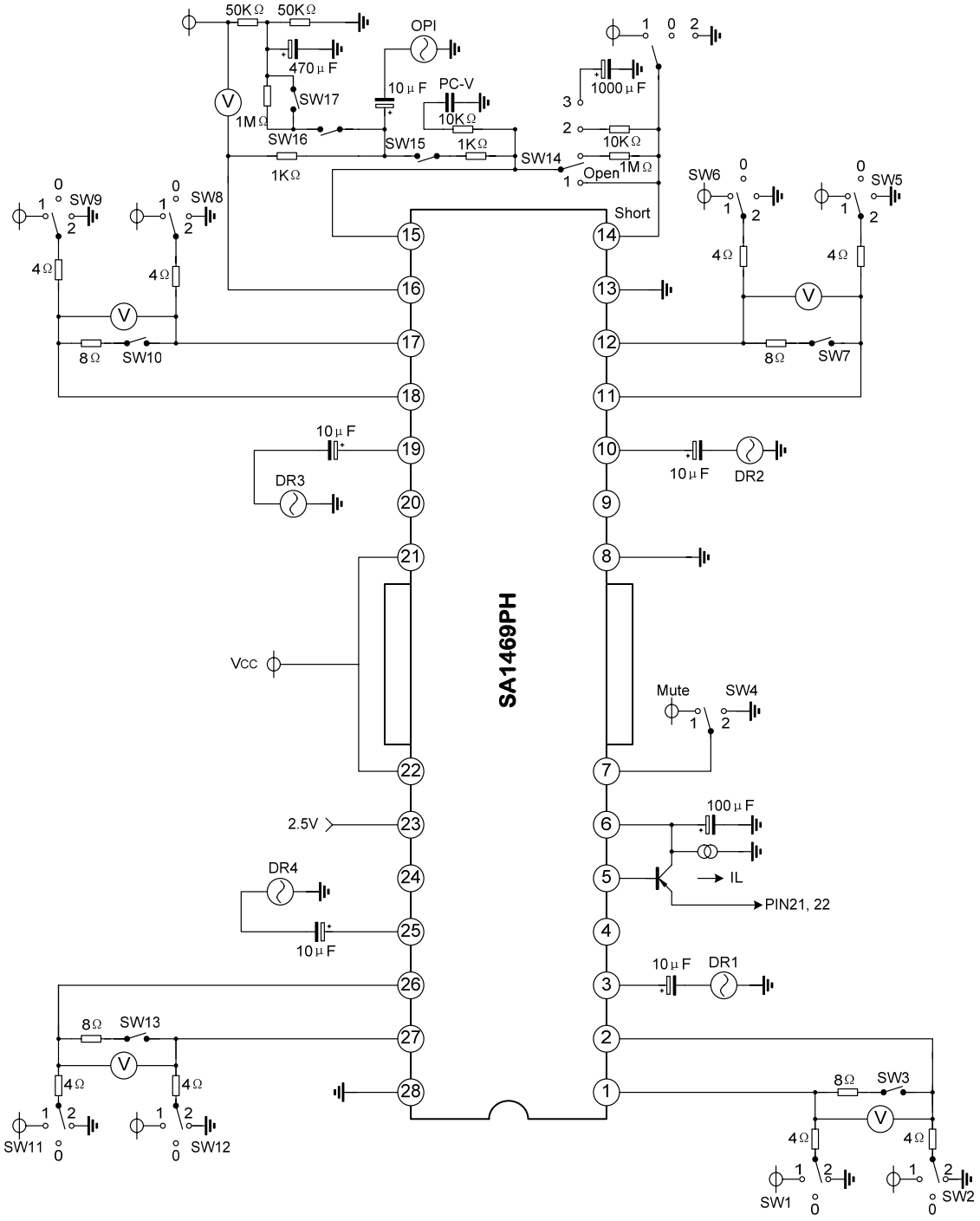
Connect the fin to the external GND.

6. REGULATOR

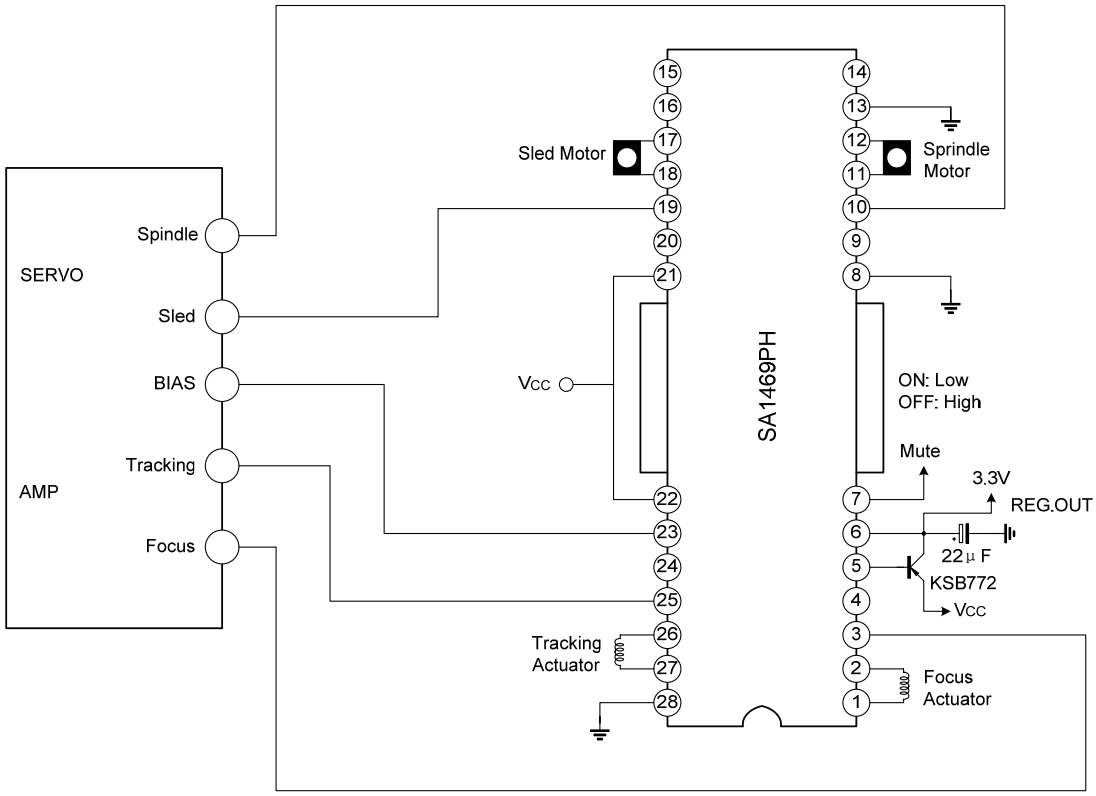
This is a typical series regulator that generates a reference voltage internally. A PNP low saturation type transistor must be connected.



TEST CIRCUIT



TYPICAL APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS CURVES

Fig.1 Driver I/O characteristics (variable load)

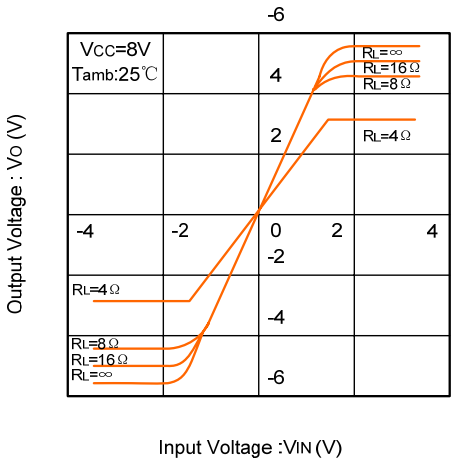


Fig.2 Driver I/O characteristics (variable power supply)

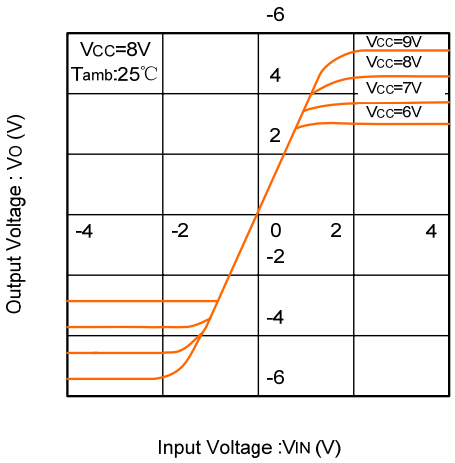


Fig. 3 Power supply voltage vs. output offset voltage

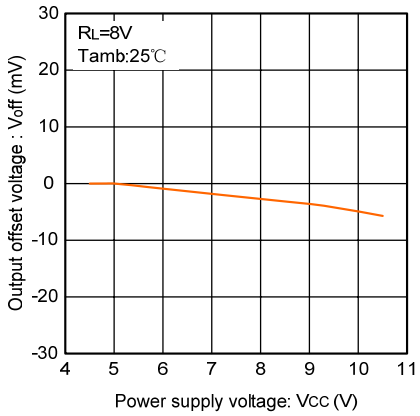


Fig. 4 Driver gain vs. temperature (RIN connected via gain adjustment pin)

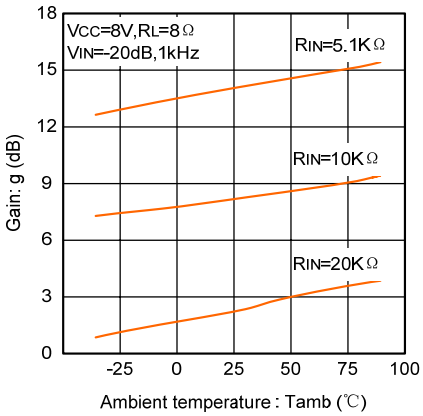


Fig. 5 Regulator voltage vs. temperature

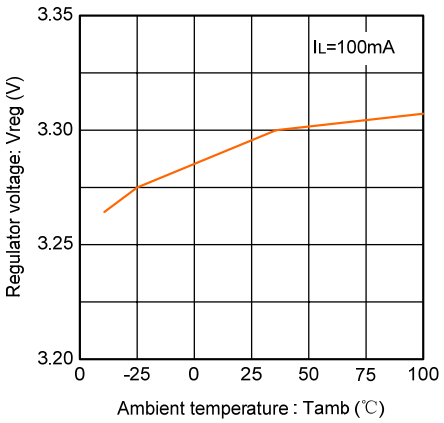


Fig. 6 Load current vs. regulator voltage

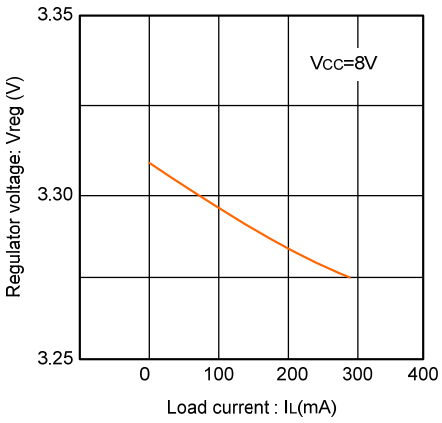
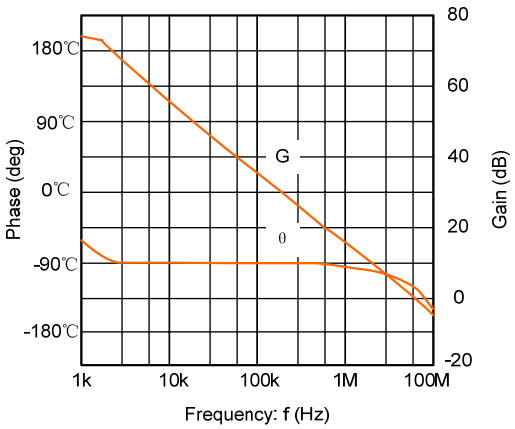
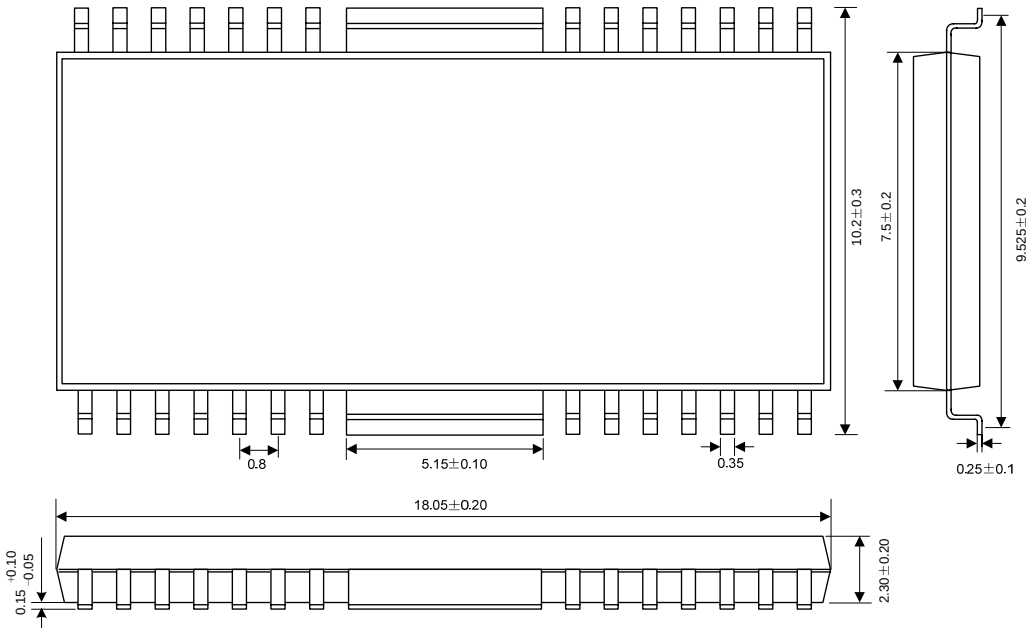


Fig. 7 Operational amplifier vs. open loop



PACKAGE OUTLINE

HSOP-28-375-0.8 UNIT: mm



ATTACH

Revision History

Data	REV	Description	Page
2003.05.26	1.0	Original	
2007.03.12	1.1	Modify the “Operating Temperature”	1
2007.08.13	1.2	Modify the “Block Diagram”, “Supply Voltage”, “Functional Description” and “Typical Application Circuit”	1,4,7
2007.10.25	1.3	Add the “Power dissipation curve”	2
2008.07.23	1.4	Modify the “Power dissipation curve”	