DATA SHEET

SA5217
Postamplifier with link status indicator

Product specification
Replaces datasheet NE/SA5217 of 1995 Apr 26
IC19 Data Handbook

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Philips
Semiconductors

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Postamplifier with link status indicator SA5217

DESCRIPTION

The SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The SA5217 can be DC coupled with the previous transimpedance stage using SA5210, SA5211 or SA5212A transimpedance amplifiers. The main difference between the SA5217 and the SA5214 is that the SA5217 does not make the output of A1 and input of A2 accessible; instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmitt trigger function by connecting two external capacitors. The result is that a much longer string of 1s and 0s, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input threshold and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, thereby insuring a low Bit Error Rate (BER). An auto-zero loop can be used to replace two input coupling capacitors with a single Auto Zero (AZ) capacitor. A signal absent flag indicates when signals are below threshold. The low signal condition forces the TTL output to the last logic state. User interaction with this "jamming" system is available. The SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 40mA from a standard 5V supply. The SA5217 is designed as a companion to the SA5211/5212A and SA5210 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The SA5210/5217, SA5211/5217 or SA5212A/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Synchronous Optical Networks (SONET) STS-1
- RF limiter
- Good for 2^{23} -1 pseudo random bit stream

PIN CONFIGURATION

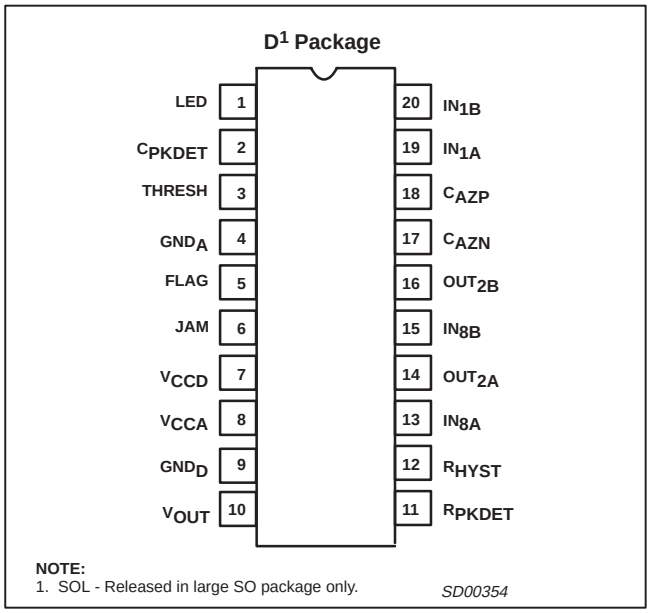


Figure 1. Pin Configuration

FEATURES

- Postamp for the SA5211/5212A. SA5210 preamplifier family
- Wideband operation: typical 75MHz (150MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5217D	SOT163-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	SA5214	UNIT
V_{CCA}	Power supply	+6	V
V_{CCD}	Power supply	+6	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation	1.4	W
V_{IJ}	Jam input voltage	-0.5 to 5.5	V

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM

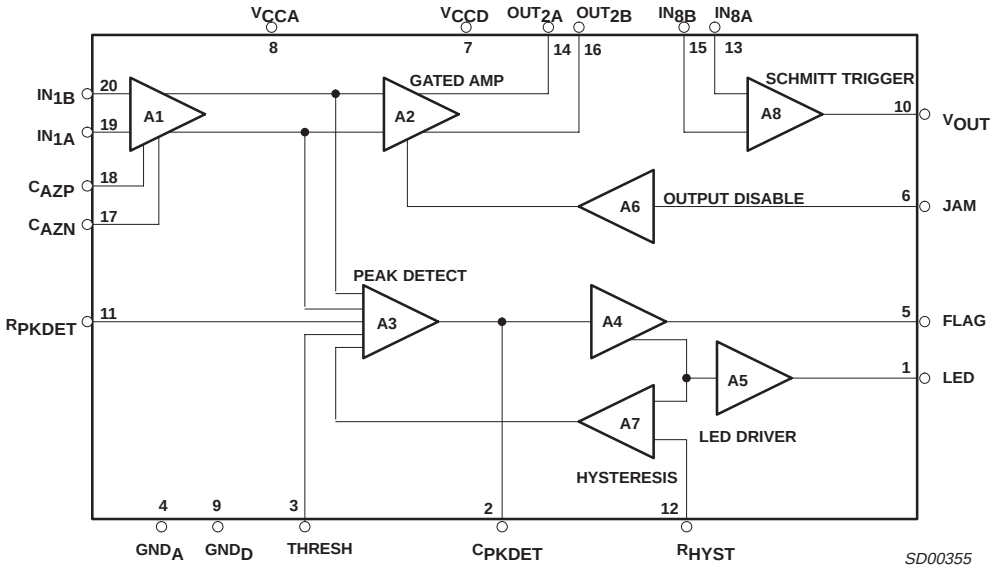


Figure 2. Block Diagram

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CCA}	Power supply	4.5 to 5.5	V
V_{CCD}	Power supply	4.5 to 5.5	V
T_A	Ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature range	-40 to +110	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at V_{CCA} = V_{CCD} = +5.0V unless otherwise specified. Typical data applies at V_{CCA} = V_{CCD} = +5.0V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{CCA}	Analog supply current			30	41.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.5	mA
V_{I1}	A1 input bias voltage (A,B inputs)		3.08	3.4	3.70	V
V_{O2}	A1 output bias voltage (A,B outputs)		3.10	3.8	4.50	V
V_{I8L}	A8 input bias voltage Low (A,B inputs)		3.40	3.55	3.68	V
V_{I8H}	A8 input bias voltage High (A,B inputs)		3.68	3.91	4.12	V
V_{OH}	High-level TTL output voltage	I_{OH}=-200µA	2.4	3.4		V
V_{OL}	Low-level TTL output voltage	I_{OL}=8mA		0.3	0.4	V
I_{OH}	High-level TTL output current	V_{OUT}=2.4V		-40	-24.4	mA
I_{OL}	Low-level TTL output current	V_{OUT}=0.4V	7.0	30		mA
I_{OS}	Short-circuit TTL output current	V_{OUT}=0.0V		-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72		V
V_{IHJ}	High-level jam input voltage		2.0			V
V_{ILJ}	Low-level jam input voltage				0.8	V
I_{IHJ}	High-level jam input current	V_{IJ}=2.7V			30	µA
I_{ILJ}	Low-level jam input current	V_{IJ}=0.4V	-485	-240		µA
V_{OHF}	High-level flag output voltage	I_{OH}=-80µA	2.4	3.8		V
V_{OLF}	Low-level flag output voltage	I_{OL}=3.2mA		0.33	0.4	V
I_{OHF}	High-level flag output current	V_{OUT}=2.4V		-18	-5	mA
I_{OLF}	Low-level flag output current	V_{OUT}=0.4V	3.25	10		mA
I_{SCF}	Short-circuit flag output current	V_{OUT}=0.0V	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	V_{LED}=3.0V	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at V_{CCA} = V_{CCD} = +5.0V unless otherwise specified. Typical data applies at V_{CCA} = V_{CCD} = +5.0V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single-ended)	Test CIrcuit		6		mV_{P-P}
	Minimum Functional A1 input signal (differential)			3		
	Minimum input sensitivity for output BER ≤ 10^{-9} (single-ended)	PRBS = 2^{23}–1		9		mV_{P-P}
	Minimum input sensitivity for output BER ≤ 10^{-9} (differential)			4.5		
R_{IN1}	Input resistance (differential at IN_1)	PRBS = 2^{23}–1		1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2		pF
R_{IN8}	Input resistance (differential at IN_2)			2000		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2		pF
R_{OUT2}	Output resistance (differential at OUT_2)			25		Ω
C_{OUT2}	Output capacitance (differential at OUT_2)			2		pF
V_{HYS}	Hysteresis voltage range (single-ended)	Test circuit, T_A = 25°C R_{RHYST}=5k R_{THRESH}=33k		10		mV_{P-P}
	Hysteresis voltage range (differential)			5		
V_{THR}	Threshold voltage (single-ended)	(FLAG Low) Test circuit, @ 50MHz		19		mV_{P-P}
	Threshold voltage (differential)	R_{RHYST}=4k R_{THRESH}=33k		9.5		
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L}10^2$		TBD		%

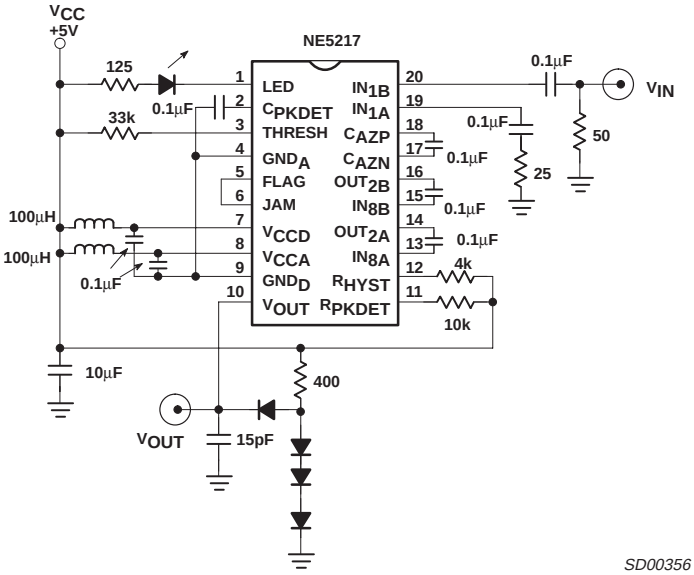


Figure 3. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

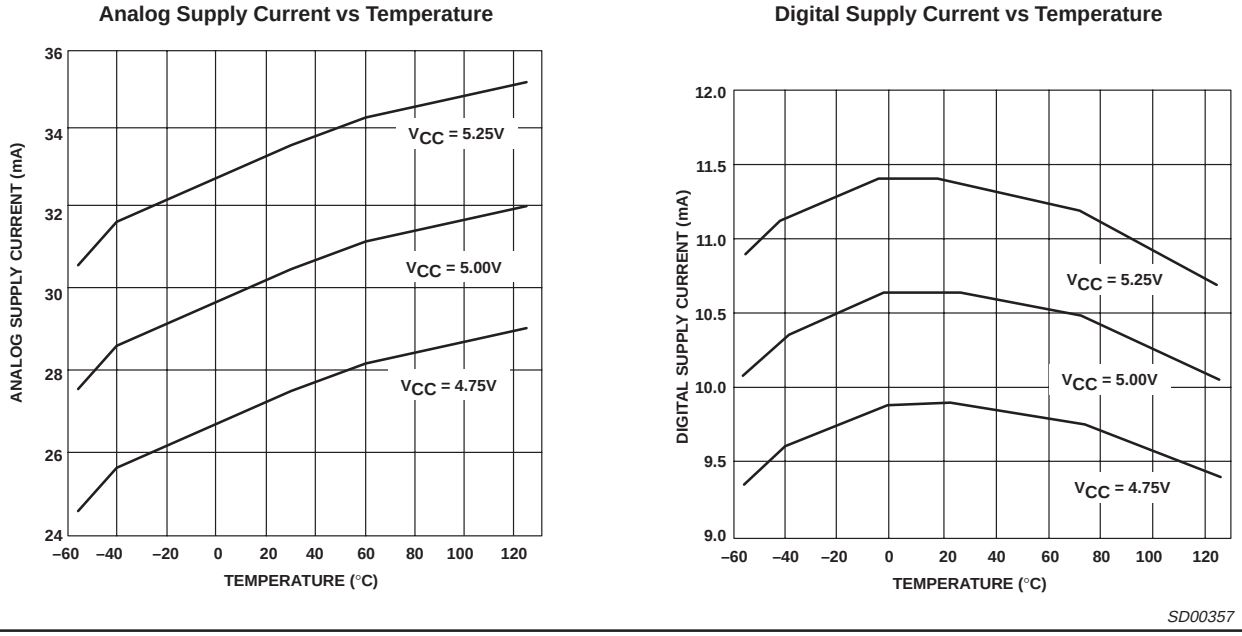


Figure 4. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

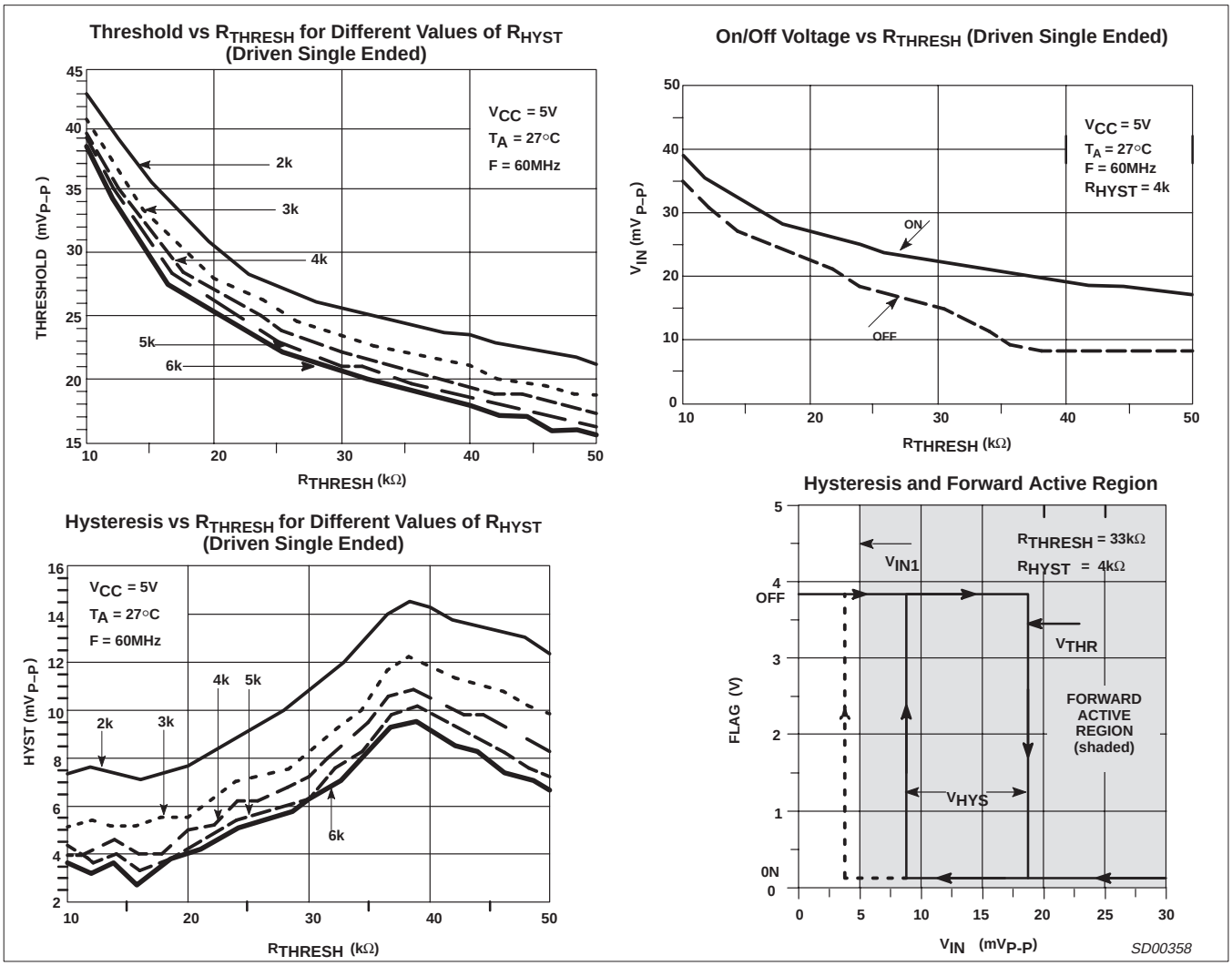


Figure 5. Typical Performance Characteristics (cont)

THEORY OF OPERATION AND APPLICATION

The SA5217 postamplifier is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

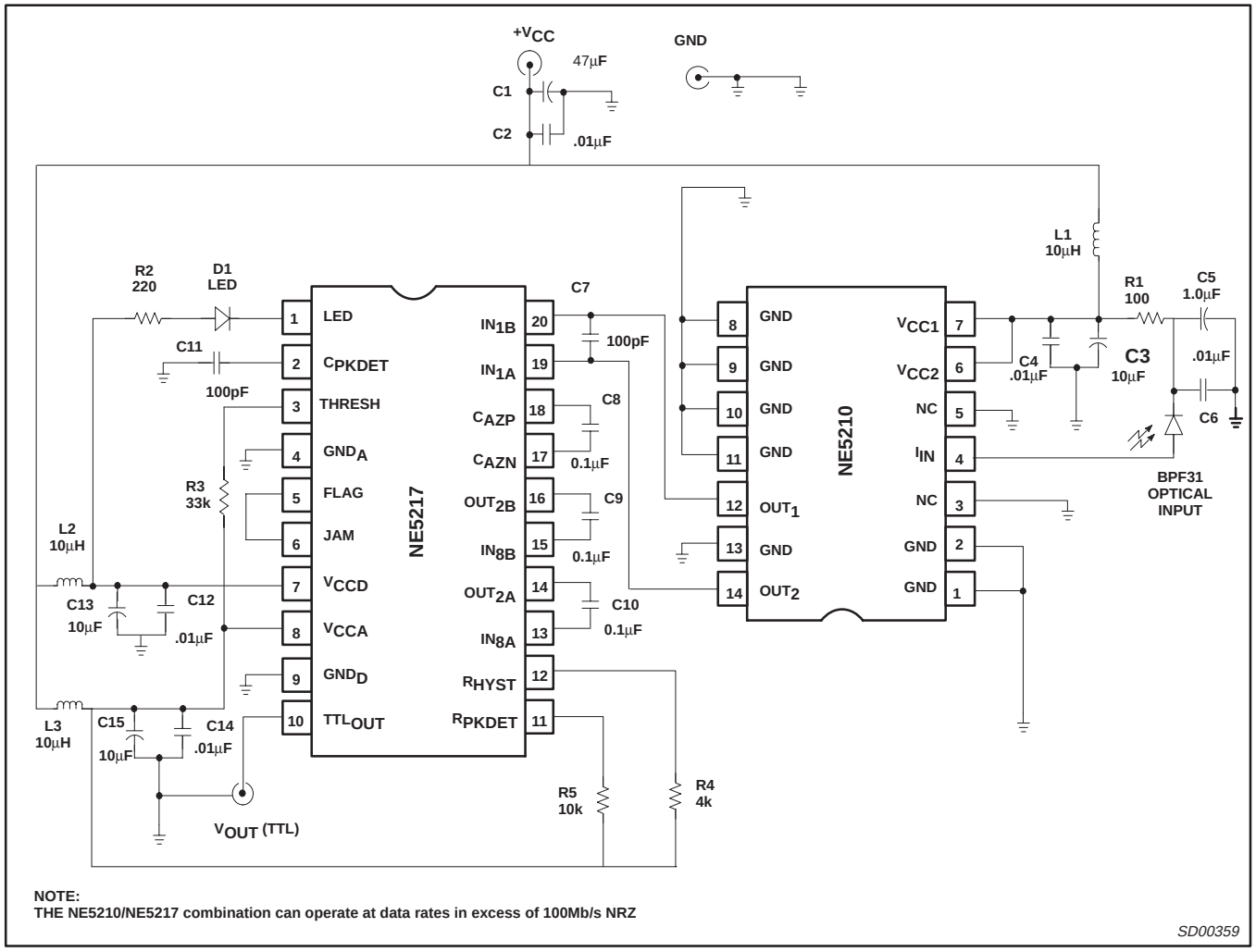
The SA5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL High on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the On state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back tot he "JAM" input; forcing the "JAM" input to TTL High will latch the TTL Data Out at the last logical state.

Threshold voltage and hysteresis voltage range are adjustable with resistors R_{THRESH} and R_{HYST}. The typical values given in the data sheet will result in performance shown in the graph "Hysteresis and Forward Active Region". A minority of parts may be sensitive enough that FLAG High (Off) occurs below the minimum functional input signal level, V_{IN1}. This condition is shown by the dotted line in the graph. Such parts may require adjustment of R_{THRESH} if it is important to guarantee that an output signal is present for the full hysteresis range. If this is not important, R_{THRESH} may be adjusted to give a FLAG Low for lower level input signals.

An auto-zero loop allows the SA5217 to be directly connected to a transimpedance amplifier such as the SA5210, SA5211, or SA5212A without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the SA5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination.

A typical application of the SA5217 postamplifier is depicted in Figure 6. The system uses the SA5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. this typical application is optimized for a 50Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.



NOTE:
THE NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

SD00359

Figure 6. A 50Mb/s Fiber Optic Receiver

For more information on this application, please refer to Application Brief AB1432.

Die Sales Disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

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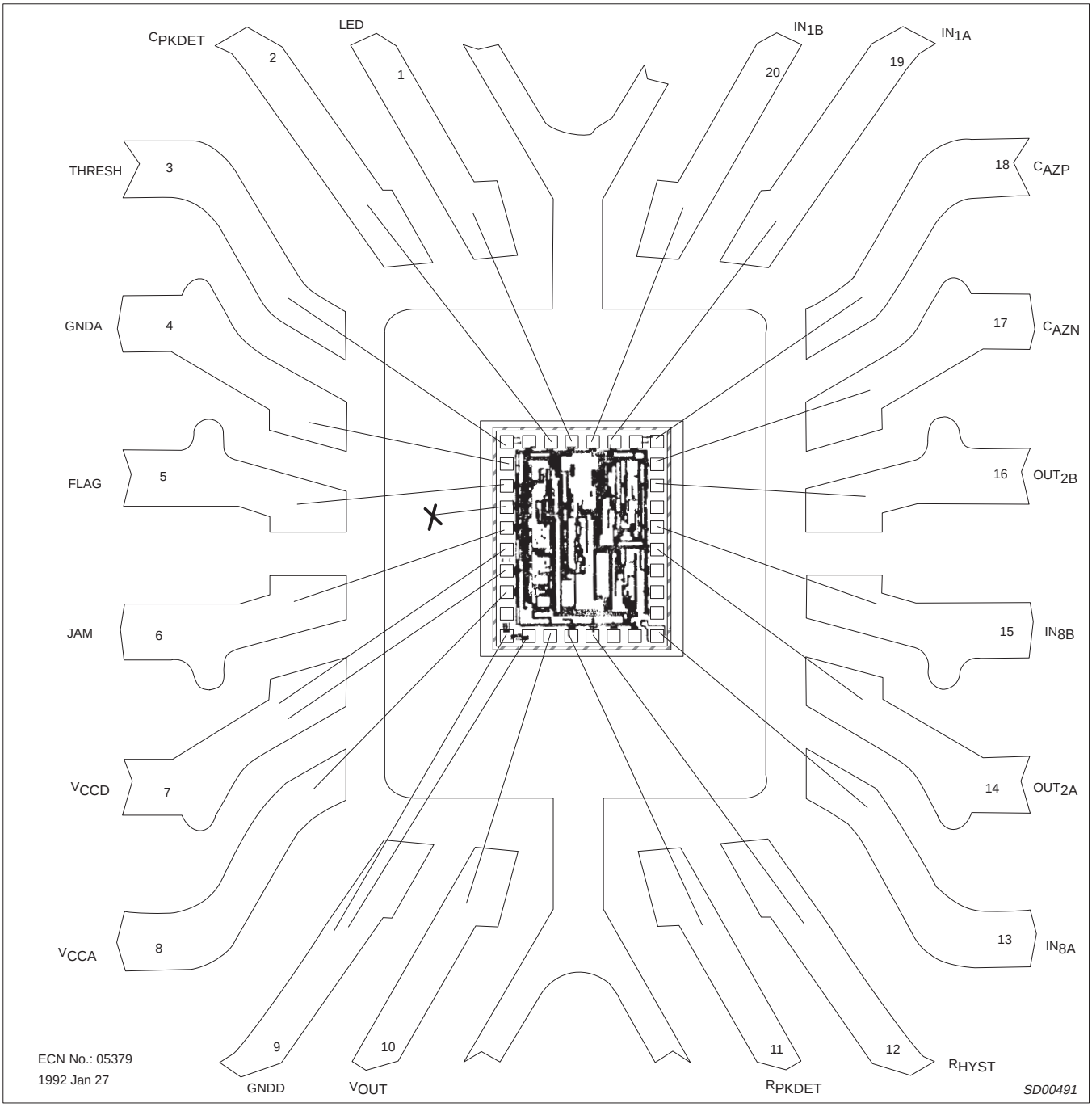
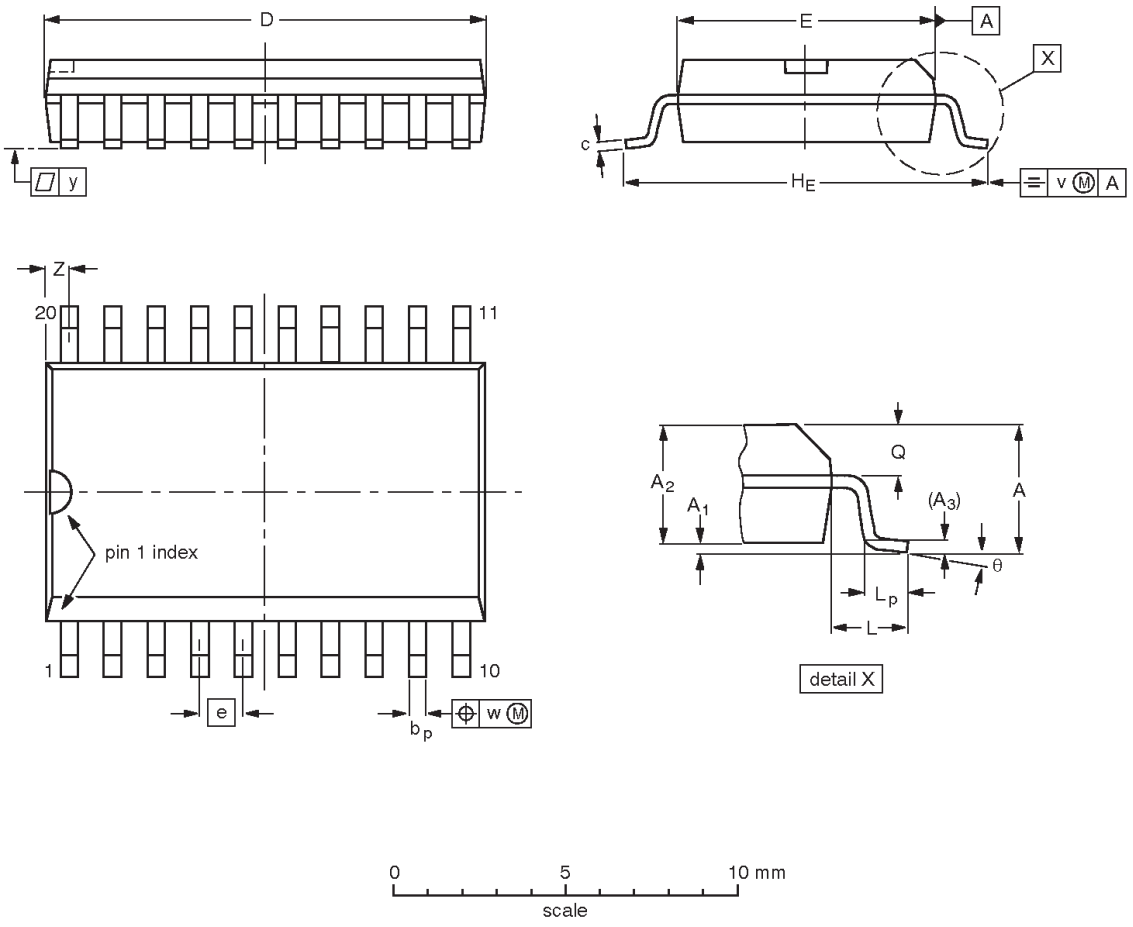


Figure 7. SA5217 Bonding Diagram

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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