SA58632

2 × 2.2 W BTL audio amplifier

Rev. 01 — 27 June 2006 Product data sheet

1. General description

The SA58632 is a two-channel audio amplifier in an HVQFN20 package. It provides power output of 2.2 W per channel with an 8 Ω load at 9 V supply. The internal circuit is comprised of two BTL (Bridge-Tied Load) amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The SA58632 is housed in a 20-pin HVQFN package, which has an exposed die attach paddle enabling reduced thermal resistance and increased power dissipation.

2. Features

- Low junction-to-ambient thermal resistance using exposed die attach paddle
- Gain can be fixed with external resistors from 6 dB to 30 dB
- Standby mode controlled by CMOS-compatible levels
- Low standby current < 10 μA
- No switch-on/switch-off plops
- High power supply ripple rejection: 50 dB minimum
- ElectroStatic Discharge (ESD) protection
- Output short circuit to ground protection
- Thermal shutdown protection

3. Applications

- Professional and amateur mobile radio
- Portable consumer products: toys and games
- Personal computer remote speakers

PHILIPS

4. Quick reference data

Table 1. Quick reference data

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		2.2	9	18	V
I_q	quiescent current	R_L = ∞ Ω	[1]	-	15	22	mA
I_{stb}	standby current	V_{MODE} = V_{CC}		-	-	10	µA
P_o	output power	THD+N = 10 %		1.2	1.5	-	W
		THD+N = 0.5 %		0.9	1.1	-	W
		THD+N = 10 %; V_{CC} = 9 V		-	2.2	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 0.5 W		-	0.15	0.3	%
PSRR	power supply rejection ratio		[2]	50	-	-	dB
			[3]	40	-	-	dB

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.

[2] Supply voltage ripple rejection is measured at the output with a source impedance of R_s = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

[3] Supply voltage ripple rejection is measured at the output, with a source impedance of R_s = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SA58632BS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 6 × 5 × 0.85 mm	SOT910-1

6. Block diagram

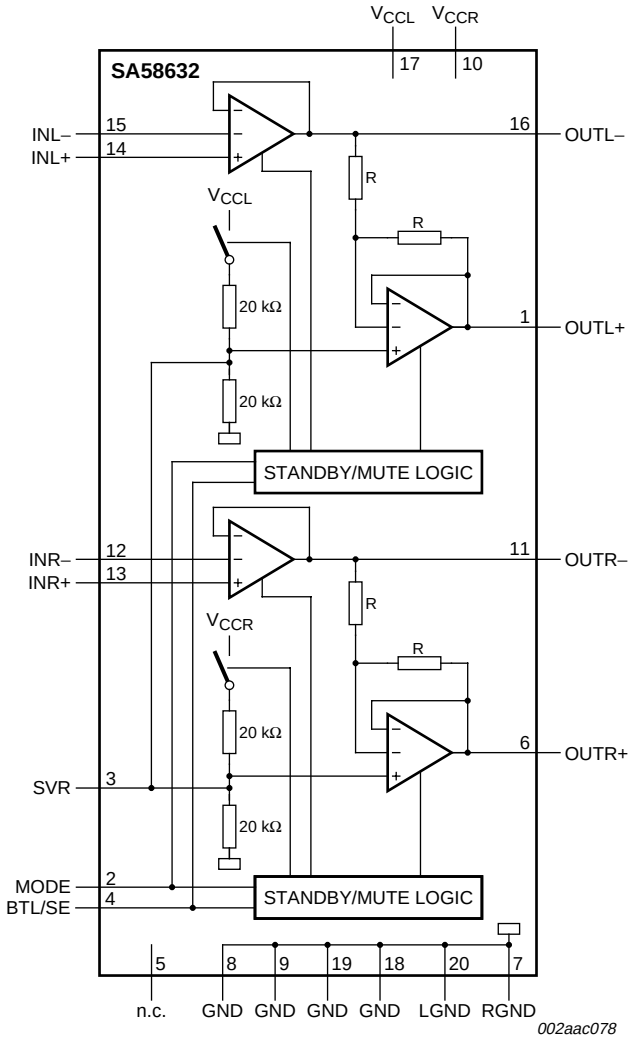


Fig 1. Block diagram of SA58632

7. Pinning information

7.1 Pinning

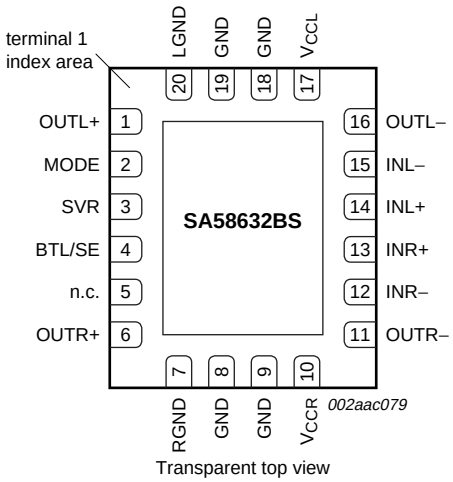


Fig 2. Pin configuration for HVQFN20

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
OUTL+	1	positive loudspeaker terminal, left channel
MODE	2	operating mode select (standby, mute, operating)
SVR	3	half supply voltage, decoupling ripple rejection
BTL/SE	4	BTL loudspeaker or SE headphone operation
n.c.	5	not connected
OUTR+	6	positive loudspeaker terminal, right channel
RGND	7	ground, right channel
GND	8, 9, 18, 19	ground[1]
V_{CCR}	10	supply voltage; right channel
OUTR–	11	negative loudspeaker terminal, right channel
INR–	12	negative input, right channel
INR+	13	positive input, right channel
INL+	14	positive input, left channel
INL–	15	negative input, left channel
OUTL–	16	negative output terminal, left channel
V_{CCL}	17	supply voltage, left channel
LGND	20	ground, left channel

[1] Pins 8, 9, 18 and 19 are connected to the lead frame and also to the substrate. They may be kept floating. When connected to the ground plane, the PCB can be used as heatsink.

8. Functional description

The SA58632 is a two-channel BTL audio amplifier capable of delivering 2 × 1.5 W output power to an 8 Ω load at THD+N = 10 % using a 6 V power supply. It is also capable of delivering 2 × 2.2 W output power to an 8 Ω load at THD+N = 10 % using a 9 V power supply. Using the MODE pin, the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range of 6 dB to 30 dB by external feedback resistors.

8.1 Power amplifier

The power amplifier is a Bridge-Tied Load (BTL) amplifier with a complementary PNP-NPN output stage. The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of an NPN power transistor. The total voltage loss is < 1 V. With a supply voltage of 6 V and an 8 Ω loudspeaker, an output power of 1.5 W can be delivered to the load, and with a 9 V supply voltage and an 8 Ω loudspeaker an output power of 2.2 W can be delivered.

8.2 Mode select pin (MODE)

The device is in Standby mode (with a very low current consumption) if the voltage at the MODE pin is greater than V_{CC} – 0.5 V, or if this pin is floating. At a MODE voltage in the range between 1.5 V and V_{CC} – 1.5 V the amplifier is in a mute condition. The mute condition is useful to suppress plop noise at the output, caused by charging of the input capacitor. The device is in Active mode if the MODE pin is grounded or less than 0.5 V (see Figure 6).

8.3 BTL/SE output configuration

To invoke the BTL configuration (see Figure 3), the BTL/SE pin is taken to logic HIGH or not connected. The output differentially drives the speakers, so there is no need for coupling capacitors. The headphone can be connected to the amplifier negative outputs using a coupling capacitor for each channel. The headphone common ground is connected to the amplifier ground.

To invoke the Single-Ended (SE) configuration (see Figure 15), the BTL/SE pin is taken to logic LOW or connected to ground. The positive outputs are muted with a DC level of $0.5V_{CC}$. Using a coupling capacitor for each channel, speakers can be connected to the amplifier negative outputs. The speaker common ground is connected to the amplifier ground. Headphones can be connected to the negative outputs without using output coupling capacitors. The headphone common ground pin is connected to one of the amplifier positive output pins.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	operating	–0.3	+18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	1	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
$V_{P(sc)}$	short-circuit supply voltage		-	10	V
P_{tot}	total power dissipation	HVQFN20	-	2.2	W

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		80	K/W
		64.5 mm^2 (10 square inch) heat spreader	[1]	22	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			3	K/W

[1] Thermal resistance is 22 K/W with DAP soldered to 64.5 mm^2 (10 square inch), 1 ounce copper heat spreader.

11. Static characteristics

Table 6. Static characteristics

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		2.2	9	18	V
I_q	quiescent current	R_L = ∞ Ω	[1]	-	15	22	mA
I_{stb}	standby current	V_{MODE} = V_{CC}		-	-	10	µA
V_O	output voltage		[2]	-	2.2	-	V
$\Delta V_{O(offset)}$	differential output voltage offset			-	-	50	mV
I_{IB}	input bias current	pins INL+, INR+		-	-	500	nA
		pins INL–, INR–		-	-	500	nA
V_{MODE}	voltage on pin MODE	operating		0	-	0.5	V
		mute		1.5	-	V_{CC} – 1.5	V
		standby		V_{CC} – 0.5	-	V_{CC}	V
I_{MODE}	current on pin MODE	0 V < V_{MODE} < V_{CC}		-	-	20	µA
$V_{I(SE)}$	input voltage on pin BTL/SE	single-ended (SE)		0	-	0.6	V
$V_{I(BTL)}$	input voltage on pin BTL/SE	BTL		2	-	V_{CC}	V
$I_{I(SE)}$	input current on pin BTL/SE	$V_{I(SE)}$ = 0 V; pin connected to ground in SE mode		-	-	100	µA

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.

[2] The DC output voltage with respect to ground is approximately $0.5 \times V_{CC}$.

12. Dynamic characteristics

Table 7. Dynamic characteristics

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD+N = 10 %		1.2	1.5	-	W
		THD+N = 0.5 %		0.9	1.1	-	W
		THD+N = 10 %; V_{CC} = 9 V; application demo board		-	2.2	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 0.5 W		-	0.15	0.3	%
$G_{v(cl)}$	closed-loop voltage gain		[1]	6	-	30	dB
ΔZ_i	differential input impedance			-	100	-	kΩ
$V_{n(o)}$	noise output voltage		[2]	-	-	100	μV
PSRR	power supply rejection ratio		[3]	50	-	-	dB
			[4]	40	-	-	dB
$V_{O(mute)}$	mute output voltage	mute condition	[5]	-	-	200	μV
α_{cs}	channel separation			40	-	-	dB

[1] Gain of the amplifier is 2 × (R2 / R1) in test circuit of Figure 3.

[2] The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of R_s = 0 Ω at the input.

[3] Supply voltage ripple rejection is measured at the output with a source impedance of R_s = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

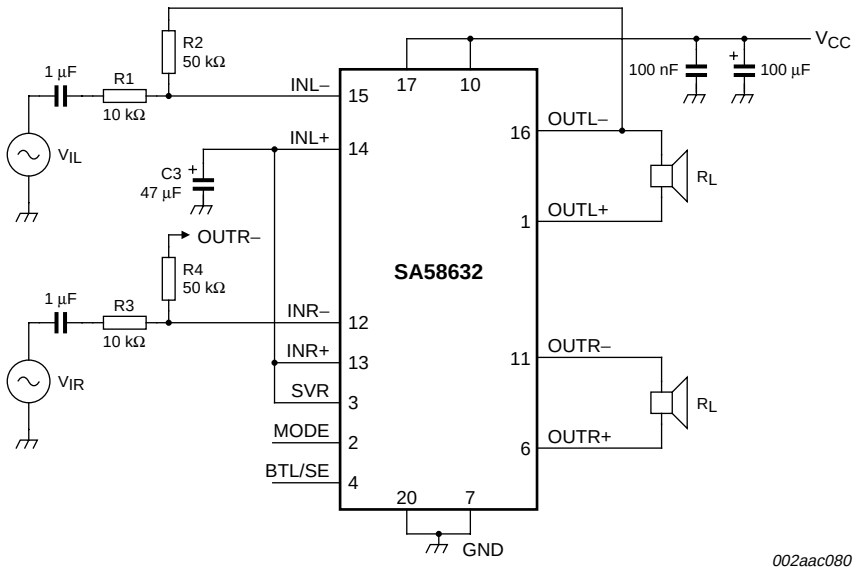
[4] Supply voltage ripple rejection is measured at the output, with a source impedance of R_s = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

[5] Output voltage in mute position is measured with an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, which includes noise.

13. Application information

13.1 BTL application

T_{amb} = 25 °C, V_{CC} = 9 V, f = 1 kHz, R_L = 8 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz. The BTL diagram is shown in Figure 3.



$$\text{Gain left} = 2 \times \frac{R2}{R1}$$

$$\text{Gain right} = 2 \times \frac{R4}{R3}$$

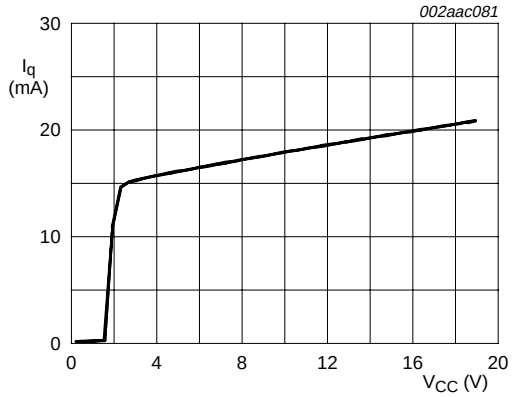
Pins 8, 9, 18 and 19 connected to ground.

Fig 3. Application diagram of SA58632 BTL differential output configuration

14. Test information

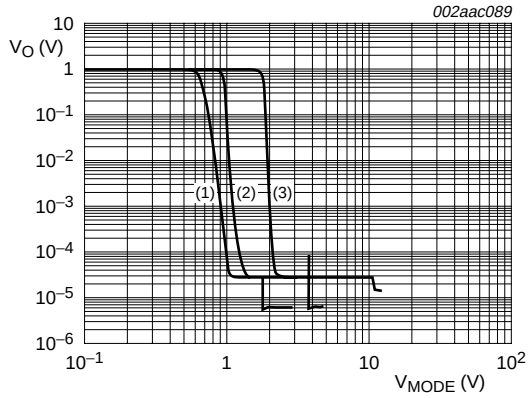
14.1 Static characterization

The quiescent current has been measured without any load impedance (Figure 4). Figure 6 shows three areas: operating, mute and standby. It shows that the DC switching levels of the mute and standby respectively depends on the supply voltage level.



$R_L = \infty\ \Omega$

Fig 4. I_q versus V_{CC}



Band-pass = 22 Hz to 22 kHz.

(1) V_{CC} = 3 V.

(2) V_{CC} = 5 V.

(3) V_{CC} = 12 V.

Fig 5. V_O versus V_{MODE}

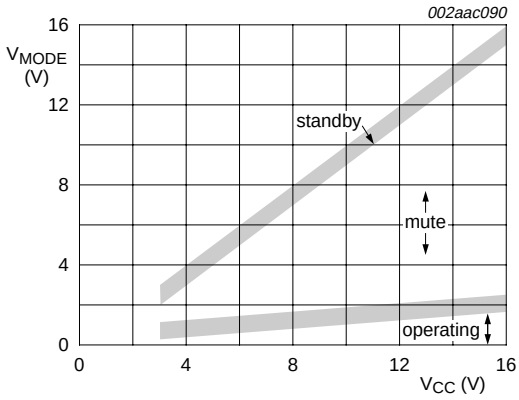
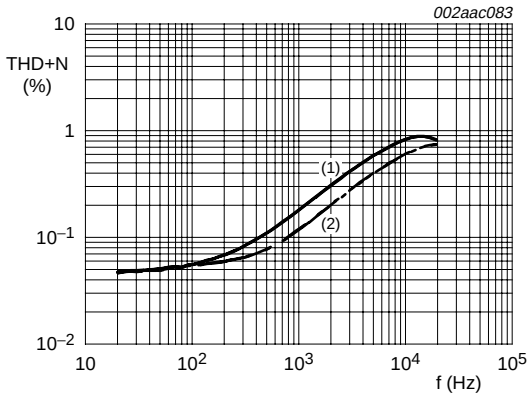


Fig 6. V_{MODE} versus V_{CC}

14.2 BTL dynamic characterization

The total harmonic distortion-plus-noise (THD+N) as a function of frequency (Figure 7) was measured with a low-pass filter of 80 kHz. The value of capacitor C2 influences the behavior of PSRR at low frequencies; increasing the value of C2 increases the performance of PSRR.

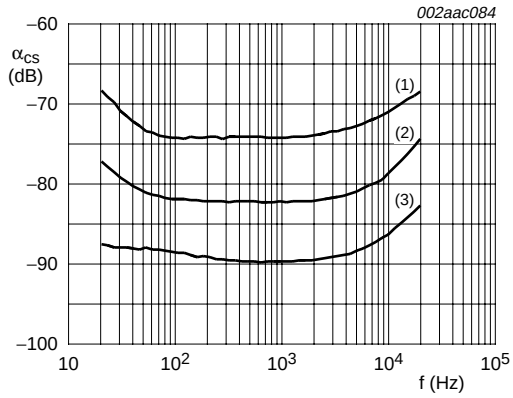


P_o = 0.5 W; G_v = 20 dB.

(1) V_{CC} = 6 V; R_L = 8 Ω.

(2) V_{CC} = 7.5 V; R_L = 16 Ω.

Fig 7. THD+N versus frequency



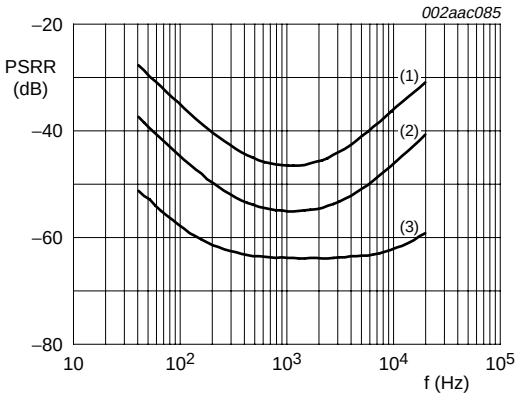
V_{CC} = 6 V; V_O = 2 V; R_L = 8 Ω.

(1) G_v = 30 dB.

(2) G_v = 20 dB.

(3) G_v = 6 dB.

Fig 8. Channel separation versus frequency



V_{CC} = 6 V; R_s = 0 Ω; V_{ripple} = 100 mV.

(1) G_v = 30 dB.

(2) G_v = 20 dB.

(3) G_v = 6 dB.

Fig 9. PSRR versus frequency

14.3 Thermal behavior

The measured thermal performance of the HVQFN20 package is highly dependent on the configuration and size of the heat spreader on the application demo board. Data may not be comparable between different semiconductors manufacturers because the application demo boards and test methods are not standardized. Also, the thermal performance of packages for a specific application may be different than presented here, because of the configuration of the copper heat spreader of the application boards may be significantly different.

Philips Semiconductors uses FR-4 type application boards with 1 ounce copper traces with solder coating.

The demo board (see Figure 23) has a 1 ounce copper heat spreader that runs under the IC and provides a mounting pad to solder to the die attach paddle of the HVQFN20 package. The heat spreader is symmetrical and provides a heat spreader on both top and bottom of the PCB. The heat spreader on top and bottom side of the demo board is connected through 2 mm diameter plated through holes. Directly under the DAP (Die Attach Paddle), the top and bottom side of the PCB are connected by four vias. The total top and bottom heat spreader area is 64.5 mm^2 (10 in^2).

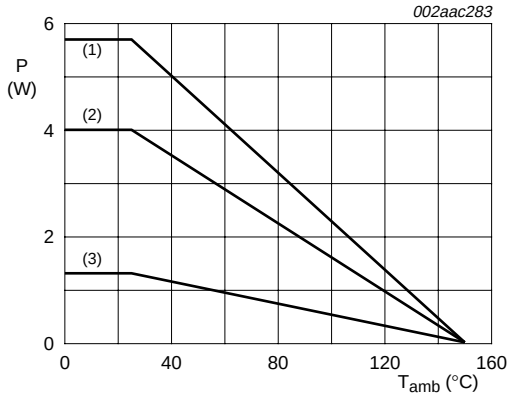
The junction to ambient thermal resistance, $R_{th(j-a)}$ = 22 K/W for the HVQFN20 package when the exposed die attach paddle is soldered to 5 square inch area of 1 ounce copper heat spreader on the demo PCB. The maximum sine wave power dissipation for T_{amb} = 25 °C is:

$$\frac{150 - 25}{22} = 5.7 \text{ W}$$

Thus, for T_{amb} = 60 °C the maximum total power dissipation is:

$$\frac{150 - 60}{22} = 4.1 \text{ W}$$

The power dissipation versus ambient temperature curve (Figure 10) shows the power derating profiles with ambient temperature for three sizes of heat spreaders. For a more modest heat spreader using 5 square inch area on the top or bottom side of the PCB, the $R_{th(j-a)}$ is 31 K/W. When the package is not soldered to a heat spreader, the $R_{th(j-a)}$ increases to 60 K/W.



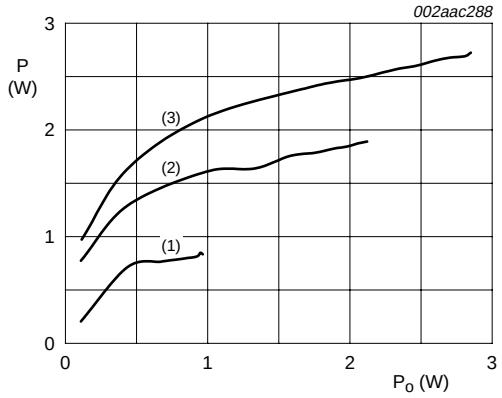
(1) 64.5 mm^2 heat spreader top and bottom (1 ounce copper).

(2) 32.3 mm^2 heat spreader top or bottom (1 ounce copper).

(3) No heat spreader.

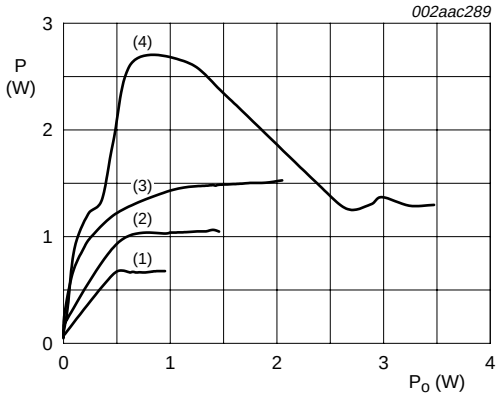
Fig 10. Power dissipation versus ambient temperature

The characteristics curves (Figure 11a and Figure 11b, Figure 12, Figure 13a and Figure 13b, and Figure 14) show the room temperature performance for SA58632 using the demo PCB shown in Figure 23. For example, Figure 11 “Power dissipation versus output power” (a and b) show the performance as a function of load resistance and supply voltage. Worst case power dissipation is shown in Figure 12. Figure 13a shows that the part delivers typically 2.8 W per channel for THD+N = 10 % using 8 Ω load at 9 V supply, while Figure 13b shows that the part delivers 3.3 W per channel at 12 V supply and 16 Ω load, THD+N = 10 %.



(1) V_{CC} = 6 V.
(2) V_{CC} = 7.5 V.
(3) V_{CC} = 9 V.

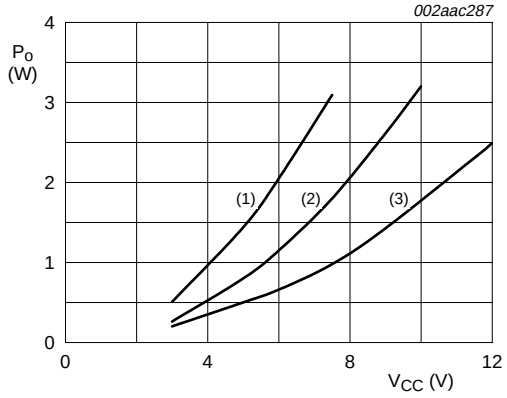
a. R_L = 8 Ω; f = 1 kHz; G_v = 20 dB



(1) V_{CC} = 6 V.
(2) V_{CC} = 7.5 V.
(3) V_{CC} = 9 V.
(4) V_{CC} = 12 V.

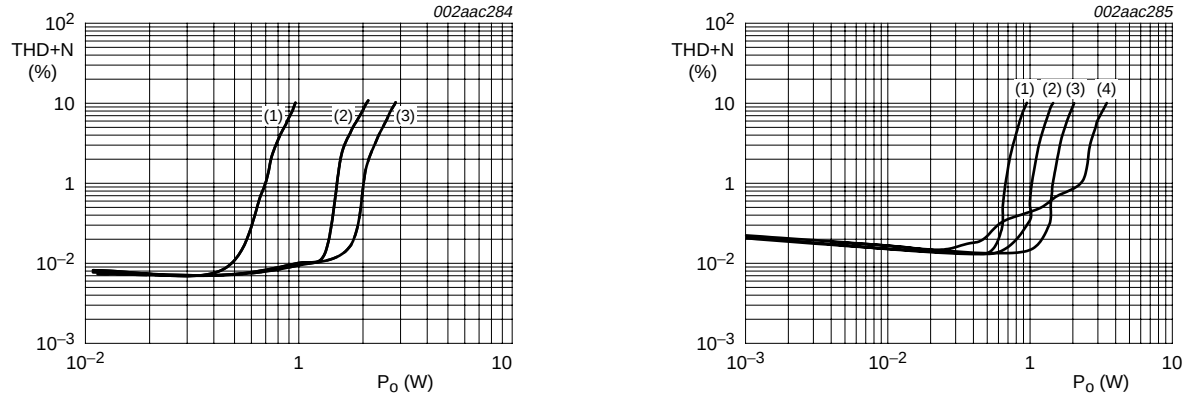
b. R_L = 16 Ω; f = 1 kHz; G_v = 20 dB

Fig 11. Power dissipation versus output power



(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig 12. Worst case power dissipation versus V_{CC}



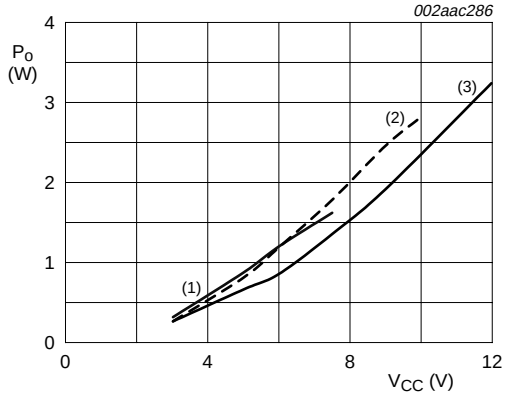
(1) V_{CC} = 6 V.
(2) V_{CC} = 7.5 V.
(3) V_{CC} = 9 V.

a. R_L = 8 Ω; f = 1 kHz; G_v = 20 dB

(1) V_{CC} = 6 V.
(2) V_{CC} = 7.5 V.
(3) V_{CC} = 9 V.
(4) V_{CC} = 12 V.

b. R_L = 16 Ω; f = 1 kHz; G_v = 20 dB

Fig 13. THD+N versus output power



THD+N = 10 %; f = 1 kHz; G_v = 20 dB.

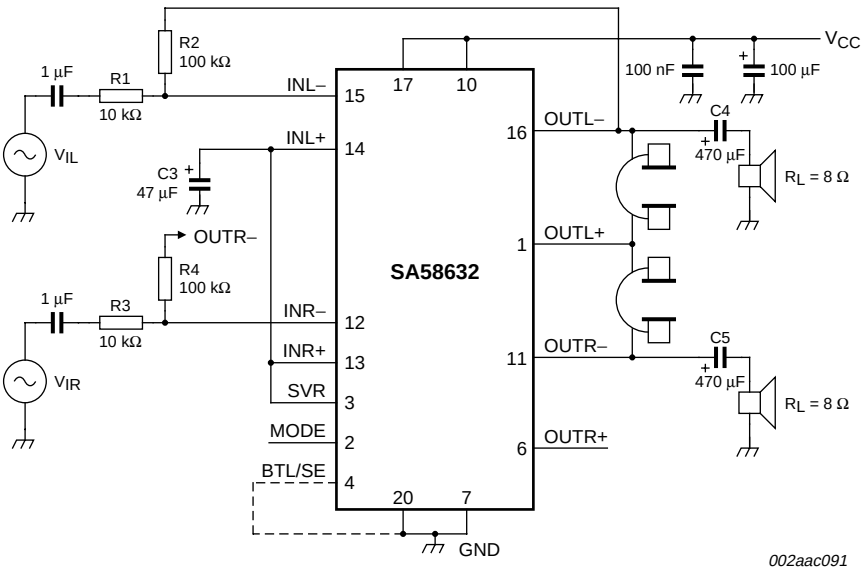
(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig 14. Output power versus V_{CC}

14.4 Single-ended application

T_{amb} = 25 °C; V_{CC} = 7.5 V; f = 1 kHz; R_L = 8 Ω; G_v = 20 dB; audio band-pass 20 Hz to 20 kHz.

The single-ended application diagram is shown in Figure 15.



$$\text{Gain left} = \frac{R2}{R1}$$

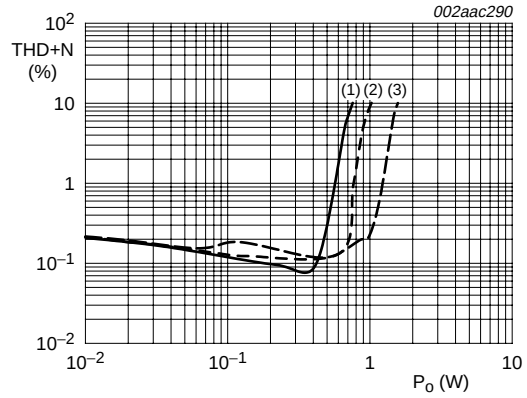
$$\text{Gain right} = \frac{R4}{R3}$$

Pins 8, 9, 18 and 19 connected to ground.

Fig 15. SE application circuit configuration

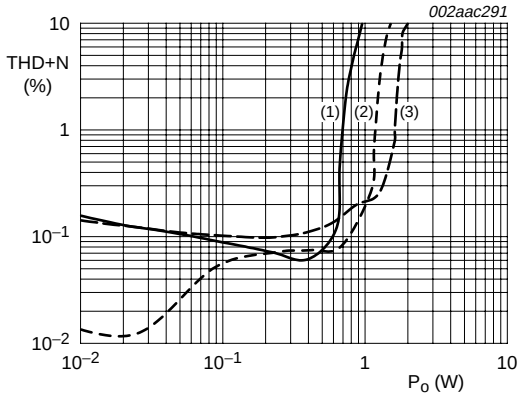
If the BTL/SE pin is to ground, the positive outputs (OUTL+, OUTR+) will be in mute condition with a DC level of 0.5V_{CC}. When a headphone is used (R_L > 25 Ω) the SE headphone application can be used without coupling capacitors by placing the load between negative output and one of the positive outputs (for example, pin 1) as the common pin.

Increasing the value of the tantalum or electrolytic capacitor C3 will result in a better channel separation. Because the positive output is not designed for high output current (2 × I_O) at the load impedance (< 16 Ω), the SE application with output capacitors connected to ground is advised. The capacitor value of C4/C5 in combination with the load impedance determines the low frequency behavior. The total harmonic distortion-plus-noise as a function of frequency was measured with a low-pass filter of 80 kHz. The value of the capacitor C3 influences the behavior of the PSRR at low frequencies; increasing the value of C3 increases the performance of PSRR.



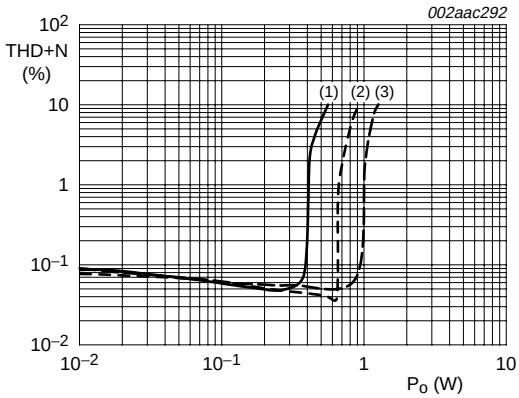
(1) V_{CC} = 7.5 V.
(2) V_{CC} = 9 V.
(3) V_{CC} = 12 V.

a. R_L = 4 Ω; f = 1 kHz; G_v = 10 dB



(1) V_{CC} = 9 V.
(2) V_{CC} = 12 V.
(3) V_{CC} = 15 V.

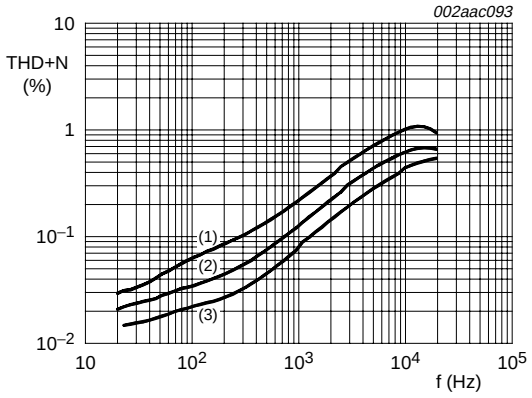
b. R_L = 8 Ω; f = 1 kHz; G_v = 10 dB



(1) V_{CC} = 9 V.
(2) V_{CC} = 12 V.
(3) V_{CC} = 15 V.

c. R_L = 16 Ω; f = 1 kHz; G_v = 10 dB

Fig 16. THD+N versus output power



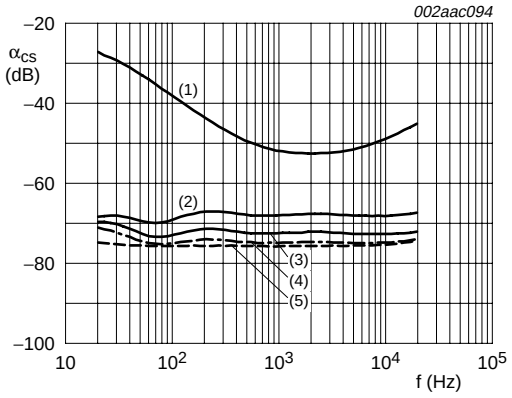
P_o = 0.5 W; G_v = 20 dB.

(1) V_{CC} = 7.5 V; R_L = 4 Ω.

(2) V_{CC} = 9 V; R_L = 8 Ω.

(3) V_{CC} = 12 V; R_L = 16 Ω.

Fig 17. THD+N versus frequency



V_o = 1 V; G_v = 20 dB.

(1) V_{CC} = 5 V; R_L = 32 Ω, to buffer.

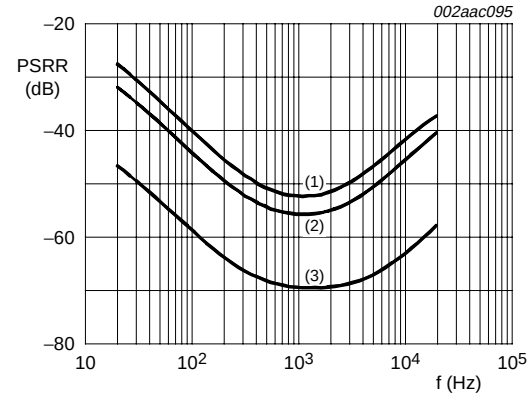
(2) V_{CC} = 7.5 V; R_L = 4 Ω.

(3) V_{CC} = 9 V; R_L = 8 Ω.

(4) V_{CC} = 12 V; R_L = 16 Ω.

(5) V_{CC} = 5 V; R_L = 32 Ω.

Fig 18. Channel separation versus frequency



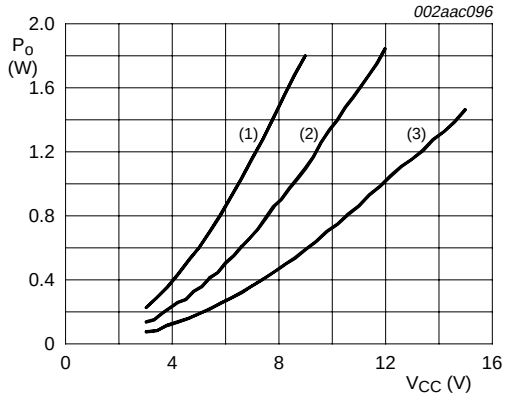
R_s = 0 Ω; V_{ripple} = 100 mV.

(1) G_v = 24 dB.

(2) G_v = 20 dB.

(3) G_v = 0 dB.

Fig 19. PSRR versus frequency



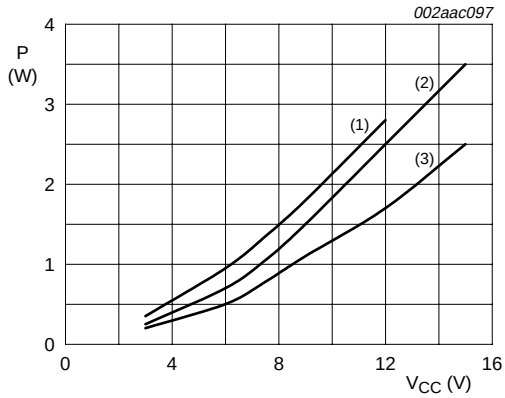
THD+N = 10 %.

(1) R_L = 4 Ω.

(2) R_L = 8 Ω.

(3) R_L = 16 Ω.

Fig 20. P_o versus V_{CC}



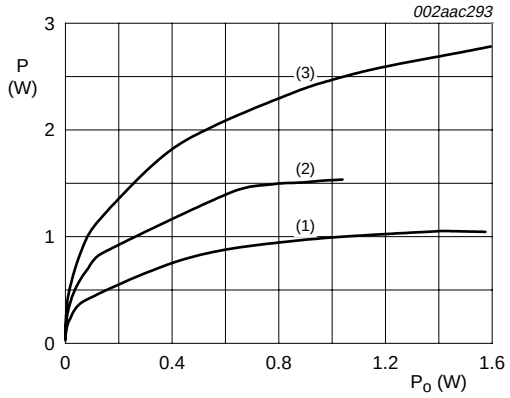
THD+N = 10 %.

(1) R_L = 4 Ω.

(2) R_L = 8 Ω.

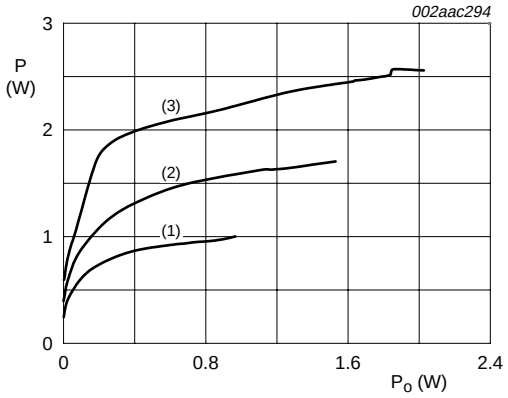
(3) R_L = 16 Ω.

Fig 21. Worst case power dissipation versus V_{CC}



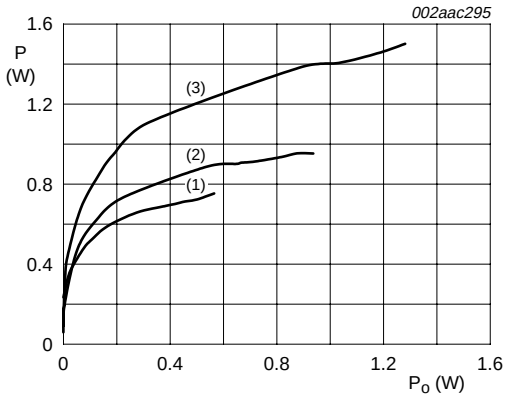
(1) V_{CC} = 7.5 V.
(2) V_{CC} = 9 V.
(3) V_{CC} = 12 V.

a. R_L = 4 Ω; f = 1 kHz; G_v = 10 dB



(1) V_{CC} = 9 V.
(2) V_{CC} = 12 V.
(3) V_{CC} = 15 V.

b. R_L = 8 Ω; f = 1 kHz; G_v = 10 dB



(1) V_{CC} = 9 V.
(2) V_{CC} = 12 V.
(3) V_{CC} = 15 V.

c. R_L = 16 Ω; f = 1 kHz; G_v = 10 dB

Fig 22. Power dissipation versus output power

14.5 General remarks

The frequency characteristics can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity of HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor (56 kΩ); this creates a low-pass filter.

14.6 SA58632BS PCB demo

The application demo board may be used for evaluation in either BTL or SE configuration as shown in the schematics in Figure 3 and Figure 15. The demo PCB is laid out for a 64.5 mm^2 (10 in^2) heat spreader (total of top and bottom heat spreader area).

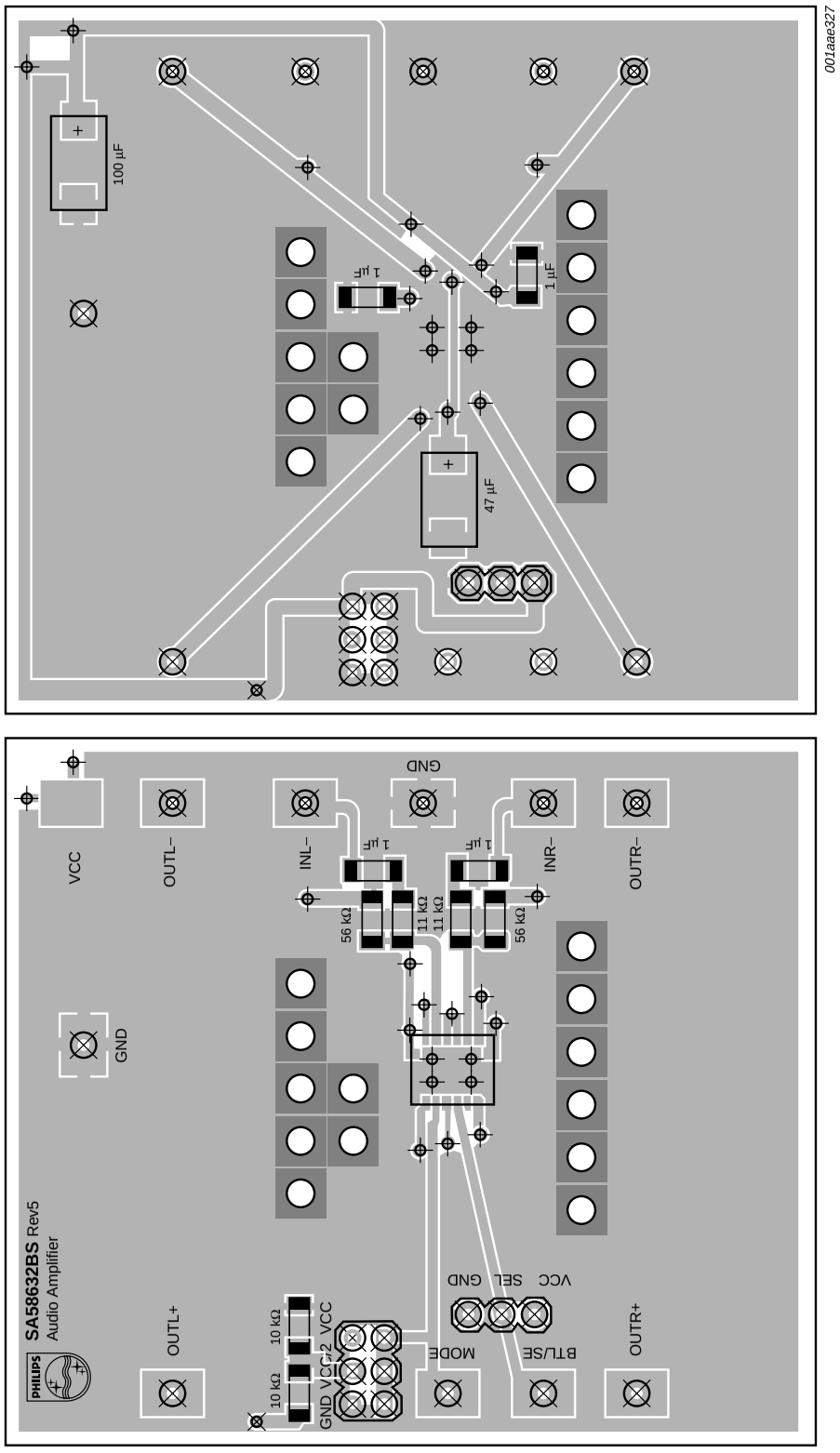
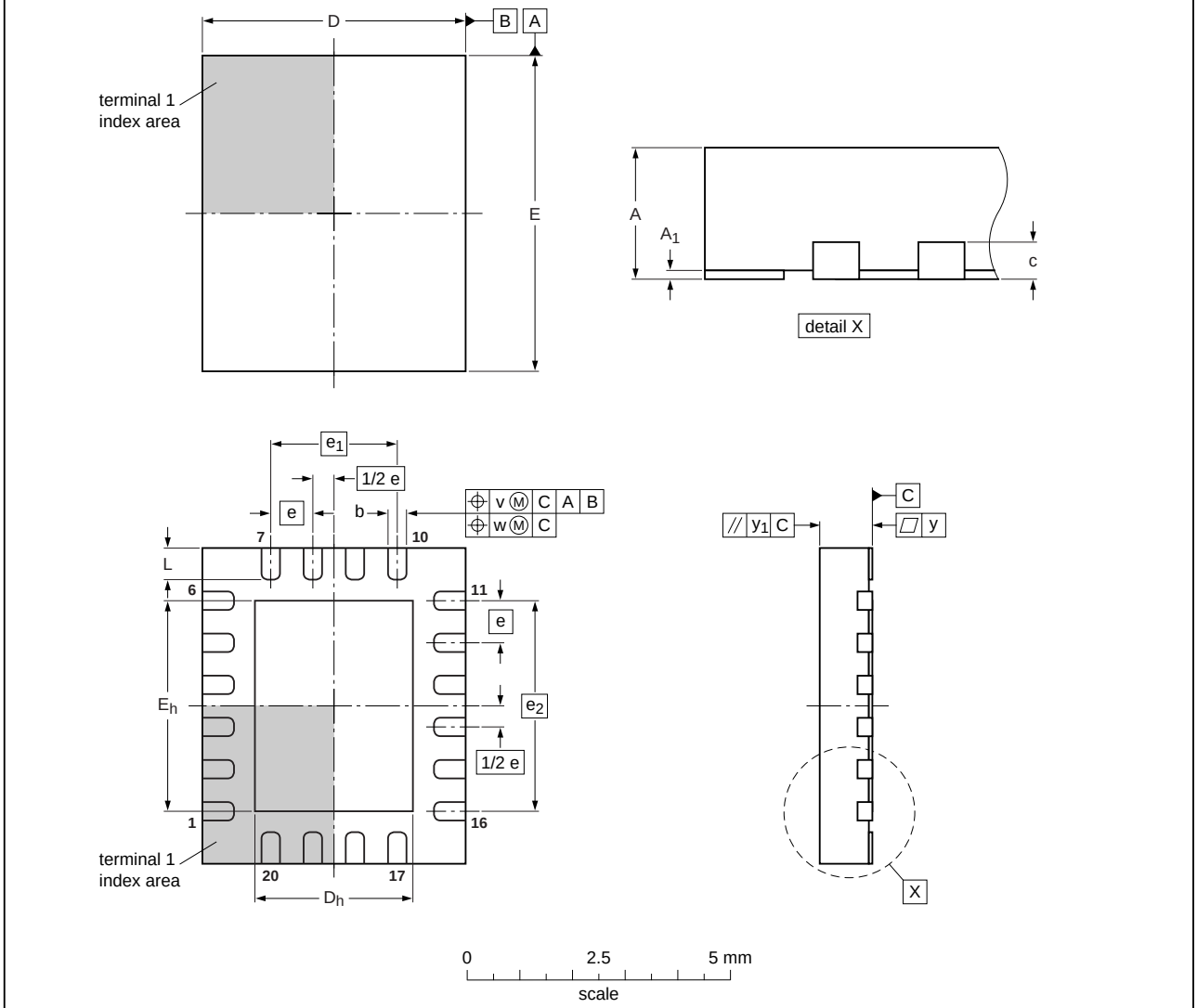


Fig 23. SA58632BS PCB demo

15. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 6 x 5 x 0.85 mm **SOT910-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.4 0.3	0.2	5.1 4.9	3.15 2.85	6.1 5.9	4.15 3.85	0.8	2.4	4	0.65 0.40	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT910-1	- - -	MO-220	- - -			05-10-11

Fig 24. Package outline SOT910-1 (HVQFN20)

16. Soldering

16.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 8. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 9. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

16.5 Package related soldering information

Table 10. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
BTL	Bridge-Tied Load
CMOS	Complementary Metal Oxide Semiconductor
DAP	Die Attach Paddle
ESD	ElectroStatic Discharge
NPN	Negative-Positive-Negative
PCB	Printed-Circuit Board
PNP	Positive-Negative-Positive
RMS	Root Mean Squared
SE	Single-Ended
THD	Total Harmonic Distortion

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58632_1	20060627	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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