IS-54 IF receiver SA638

DESCRIPTION

The SA638 is an IF receiver chip which serves the dual mode functionality required by the IS–54 standards for North American cellular telephones. It provides for both the analog FM (AMPS mode) and DQPSK (TDMA digital mode) IF receive functions in a monolithic BiCMOS Integrated Circuit housed in a compact SSOP–24 plastic package.

APPLICATIONS

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FEATURES

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PIN CONFIGURATION

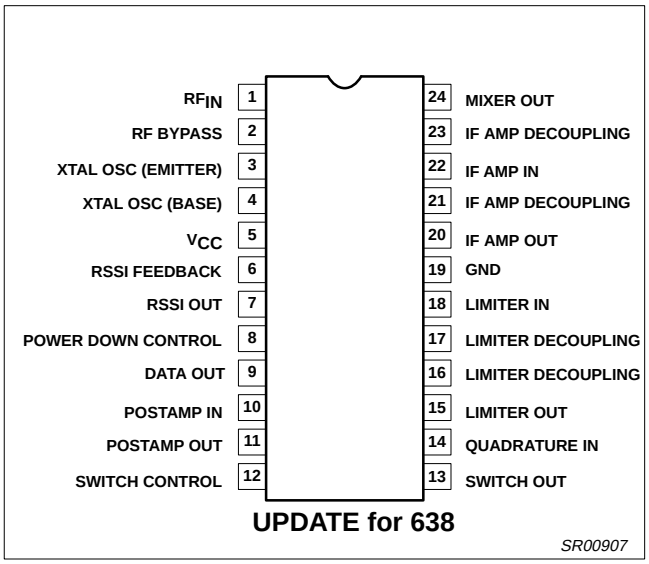

Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA638	SOT-355

BLOCK DIAGRAM

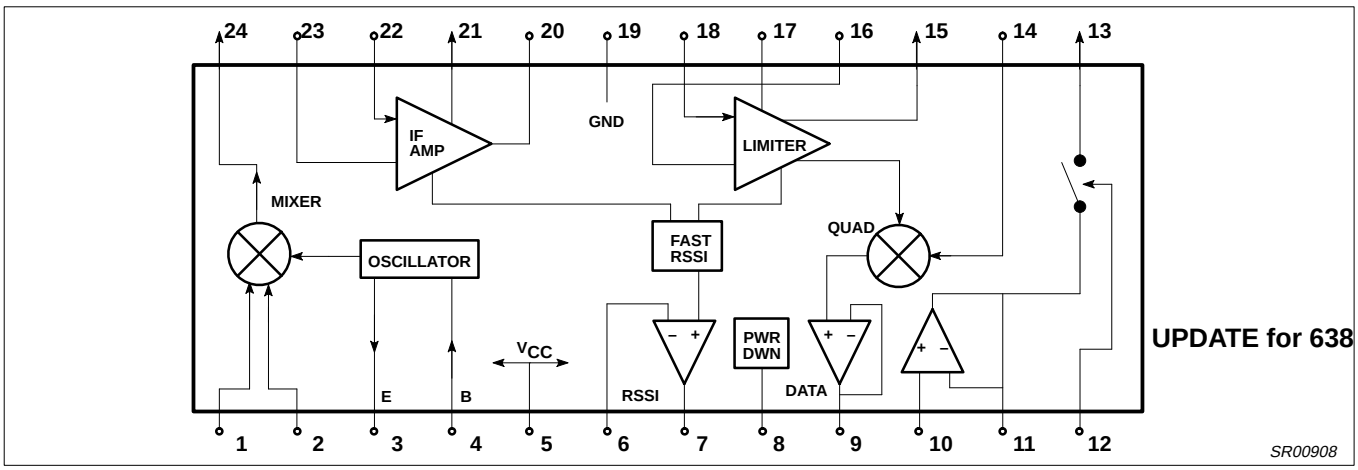

Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$RF_{IN(+)}$	**RF Input Plus:** Differential RF Plus input to mixer.
2	$RF_{IN(-)}$	**RF Input Minus:** Differential RF Minus input to mixer.
3	OSC_B	**LO Oscillator Transistor Base:** LO generator (Pins 3 and 4) with internal buffer to drive mixer differentially. Can also be driven externally.
4	OSC_E	**LO Oscillator Transistor Emitter:** Pins 3 and 4 are used to form an oscillator with external components (tank, varactor, etc.).
5	V_{CC1}	**Supply Voltage 1:** Voltage supply for mixer and main bias.
6	RSSI/AGC	**RSSI Out and AGC Input:** Dual use: RSSI output in AMPS mode (no internal opamp) and AGC input in QPSK mode if needed. If no AGC, input will auto AGC to pre-defined fixed level for IQ outputs, in which case this pin also serves as RSSI output.
7	PWRDWN	**Power-Down:** Chip power-down input (CMOS compatible).
8	OSC_{DEMOD}	**IF Oscillator Input (LO frequency x4):** Oscillator input x4 for I/Q demodulation is needed for internally generating quad LOs by division.
9	ModeSW	**Mode Switch:** Logic control signal to select between AMPS and QPSK modes of operation.
10	AUDIO/LPF	**Audio Out and LPF Corner Frequency Control:** Dual Use: Audio output in the AMPS mode and LPF corner frequency control in QPSK mode.
11	DEMOD1	**Demod Auxiliary Pin:** Used to implement FM demodulation in AMPS mode.
12	Q	**Baseband Q Ouptut:** Quadrature baseband output referenced to IQ_{REF}.
13	I	**Baseband I Output:** In-phase baseband output referenced to IQ_{REF}.
14	V_{CC2}	**Supply Voltage 2:** Voltage supply for IF amp and demodulator.
15	IQ_{REF}	**I/Q Reference Voltage:** Reference voltage for baseband I/Q outputs.
16	GND2	**Ground 2:** Ground common for IF amp and demodulator.
17	DEMOD2/Offsets	**Demod Auxiliary Pin and I/Q Offset Control:** Dual Use: In AMPS mode serves for FM demodulator; in QPSK mode serves as I/Q offset control.
18	IQ DEMOD	**Input to the Demodulator:** IF input to demodulator from AGC IF amp output.
19	GND1	**Ground 1:** Ground common for mixer and main bias.
20	$IFAMP_{OUT}$	**IF Amplifier Output:** IF amplifier output.
21	V_{CCMID}	**V_{CC} Midpoint Bypass:** The internally generated VCC midpoint bias needs to be externally bypassed with a suitable capacitor.
22	$IFAMP_{IN}$	**Input to IF Amplifier**: Input to IF Amplifier from mixer through external filter.
23	$IFAMP_{DC}$	**Reference Input to IF Amp:** External bypassing for low frequency feedback of IF amp to null DC offsets.
24	MIX_{OUT}	**Output from Mixer:** IF output from mixer to external BPF and IF amp.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage		V
V_{IN}	Voltage applied to any other pin		V
T_{STG}	Storage temperature range		°C
T_A	Operating ambient temperature range SA639		°C

NOTE: θ_{JA} Thermal impedance (DH package) 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA639			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain			10		mA
Mixer						
	Conversion power gain	Input matched externally to tbdΩ, Output is doubly terminated filter, 1.5kΩ impedance		15		dB
	Noise figure	Single side band		8.5		dB
IIP3	Input IP3			-10		dBm
	Input P-1, input compression point			-20		dBm
	Input impedance	1kΩ series with 2.5pF				
	IF output impedance			1.5		kΩ
	Input frequency range			150		MHz
	LO and 2xLO suppression at IF output			-30		dBc
	IF frequency				2	MHz
IF Amp, FM Demodulator, RSSI in FM Mode						
	IF amp gain			90		dB
	Input impedance			1.5		kΩ
	Output impedance			150		Ω
	RSSI dynamic range			90		dB
	RSSI linearity		-1.5		+1.5	dB
	Audio output impedance			300		Ω
	Audio output level			110		mV_{RMS}
	Audio SINAD for RF signal -50dBm			35		
	Noise figure			11		dB
	Output IP3			tbd		
IF Amp, AGC, RSSI and IQ Demodulator, QPSK Mode						
	Input impedance			1.5		kΩ
	Gain		10		95	dB
	Input IP3			tbd		
	RSSI dynamic range			90		dB
	RSSI linearity		-2.5		+2.5	dB
	LPF frequency control		40		80	kHz
	Channel matching: gain			1		dB
	phase			5		deg.
	I/Q output level	for a given tbd linearity; about IQ output reference level		250		mV_{PEAK}
	I/Q output reference level			tbd		

NOTE:
1.

CIRCUIT DESCRIPTION

The Mixer

The mixer section converts signals up to 150MHz to a 2nd IF of up to 2MHz (typically around 455KHz) with a power gain of 15dB, input IP3 of –10dBm and NF of 8.5dB. This section is comnlon to both modes of operation. An on–chip oscillator is provided (for use with an external tank, varactor, and synthesizer). The LO section has a buffer to drive the mixer differentially.

After external bandpass filtering, the signals enter the chip again into the IF amplifier section. One input of the IF amp is biased to V_{ccmid} (which is Vcc/2 generated internally and by–passed externally) and AC-coupled to the input signal externally while the other IF amp input is fed back from the amplifier output and AC by–passed to ground externally. This minimizes low frequency offsets since the amp is DC-coupled with very high gain.

(Note that, compared to our standard 6xx IF chips, we are freeing quite a few pins by using only 1 decoupling pin and by NOT splitting up the IF amp into 2 parts and going in and out for filtering in between.

In the AMPS mode the amplifier acts as a classic limiter with a fairly constant output voltage for a very large input voltage range. The RSSI (Received Signal Strength Indicator) is a temperature compensated high impedance output signal which acts as a voltage proportional to Logarithm of the input power and has a 90dB dynamic range. In the Digital mode the IF amp acts as a linear AGC (Automatic Gain Controlled) amplifier with maximum gain of 95dB and an AGC range of 85dB. The control for the AGC can be derived internally or supplied externally. If not supplied externally the internal AGC detector will regulate the gain to set the IQ baseband outputs to a pre–determined level (e.g., 250mV_{PEAK}). The RSSI output which is high impedance will then be available at Pin 6 after external filtering. On the other hand an external AGC input can force the voltage at this pin to regulate the gain externally based on external measurement of say the IQ baseband output voltages. In such a case the RSSI function is NOT provided by this pin. (This has been done mainly to conserve pins. Depending on customer feedback we can provide for separate RSSI output and AGC input pins if necessary.)

The IQ Demodulator Section

The IQ Demodulator section takes the signal after external filtering fronl the chip's IF anlp output. The I/Q LO is supplied to the chip externally as a x4 of the required correct LO signal such that the internal divider can generate quadrature LO signals of the correct frequency. After conversion to baseband the signals are filtered for suppressing LO and its by–products. (We have to decide if this filter will also provide for accurate baseband filtering. For example TI's ARCTIC baseband processor chip provides for such filtering in which case we do not have to provide for it.) After buffering, the single ended baseband IQ outputs are available for processing externally. The signals are referenced to a fixed DC level generated internally and available througn Pin 15. We can save a pin if the V_{ccmid} (Pin 21) can be used for this purpose. Single-ended outputs as described above are used rather than differential outputs in order to save pins.

The FM Demodulator section

The FM Demodulator section will incorporate a new technique wnich will not require a quad tank. However, a backup technique of the quad discriminator will be available if the new riskier approach fails. Because of this, two pins have been allocated for the FM demodulator in addition to the audio output (similar to our existing FM–IF products).

In this pinout there is provision for 2 V_{CC} pins and 2 ground pins in addition to a $V_{CC}/2$ bypass pin. This seems necessary in light of the hign gain values involved in the IF amp block.

There are at least three pins which have dual functionality: RSSI/AGC; Audio/LPF; Demod2/ IQ Offsets. We have to carefully look at this to see if this is feasible. If not, the pinout has to be changed appropriately.

Fallback Positions:

1. We have a fallback for the FM demodulator, the classic FM discriminator.
2. If the "one IF amp will work for both modes'' approach fails, we can provide 2 separate IF amp paths and switch between them for the different modes. The penalty is increased chip area.
3. The proposed solution for the lF amp is to have all its gain in one section with no external filtering in between. This is aggressive since our existing chips have 2 IF sections with separate DC feedback for each section and external filtering in between. If the proposed 1 section solution fails, going back to our old technique will require more pins than we perhaps have!

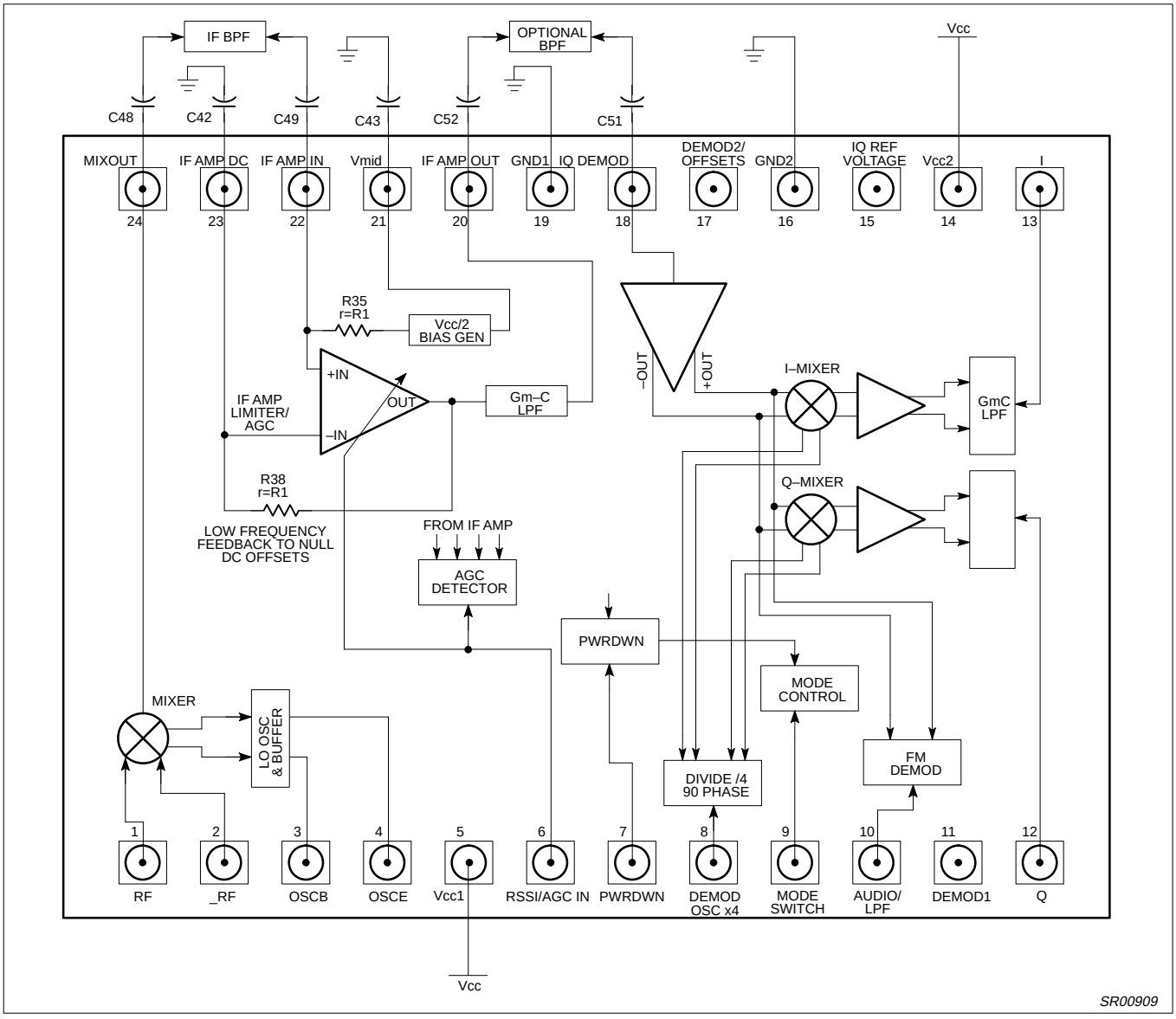

Figure 3. SA638 IS-54 Dual-Mode IF Chip