DATA SHEET

SA900
I/Q transmit modulator

Preliminary specification

IC17 Data Handbook

1997 Sept 16

Philips
Semiconductors

PHILIPS

I/Q transmit modulator SA900

DO NOT DISTRIBUTE WITHOUT ECN DATED AFTER Sept 16, 1997

DESCRIPTION

The SA900 is a monolithic high performance, multi-function transmit modulator for use in cellular radio applications, fabricated in QUBiC BiCMOS technology. The SA900 features both analog (AMPS) mode and complex, I/Q digital (NADC IS–136) mode quadrature modulation functions, a PLL synthesizer with VCO, crystal oscillator, programmable prescalers and Gilbert cell multiplier phase detector with programmable charge pump output. The DUALTX output can be used in DUAL mode cellular phone applications with the AMPS and NADC modulation being applied to the I/Q baseband inputs. The DUALTX output also provides 6-bit power control with 40dB of gain control in 0.63dB steps. In addition, buffered crystal oscillator programmable prescaler outputs are provided to support system clock reference needs. Programming of the SA900 functions are realized by a high speed 3-wire serial interface. The SA900 can be programmed into a sleep mode (low current mode providing crystal oscillator and Master Clock functions), a standby mode (providing crystal oscillator, Master Clock, System Clock 1 and Transmit LO buffer functions), and the AMPS mode and the DUAL mode configurations.

FEATURES

- V_{CC} = 4.0V
- Tx output frequency = 900MHz
- Direct modulation of RF
- DUAL mode, on-chip PA control
- I/Q modulator
- Single sideband quadrature LO generation with no external adjustments required
- On-chip crystal oscillator with 3 buffered outputs
- AMPS/TACS compatible
- On-chip VCO

PIN CONFIGURATION

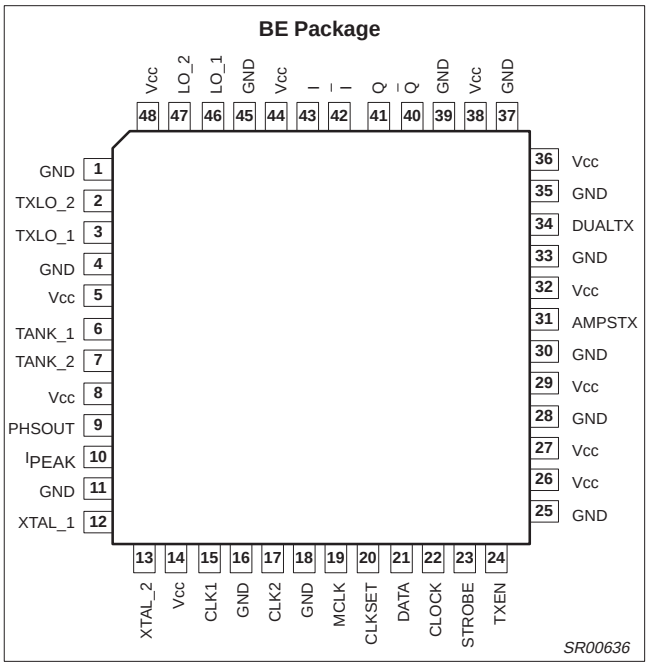


Figure 1. Pin Configuration

- Selective power-down
  - Low power AMPS/TACS mode
  - Low power dual mode NADC
- 48-Pin TQFP package

APPLICATIONS

- North American Digital Cellular (TDMA IS-136)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Plastic Low Profile Quad Flat Package (LQFP)	-40 to +85°C	SA900BE	SOT313-2

BLOCK DIAGRAM

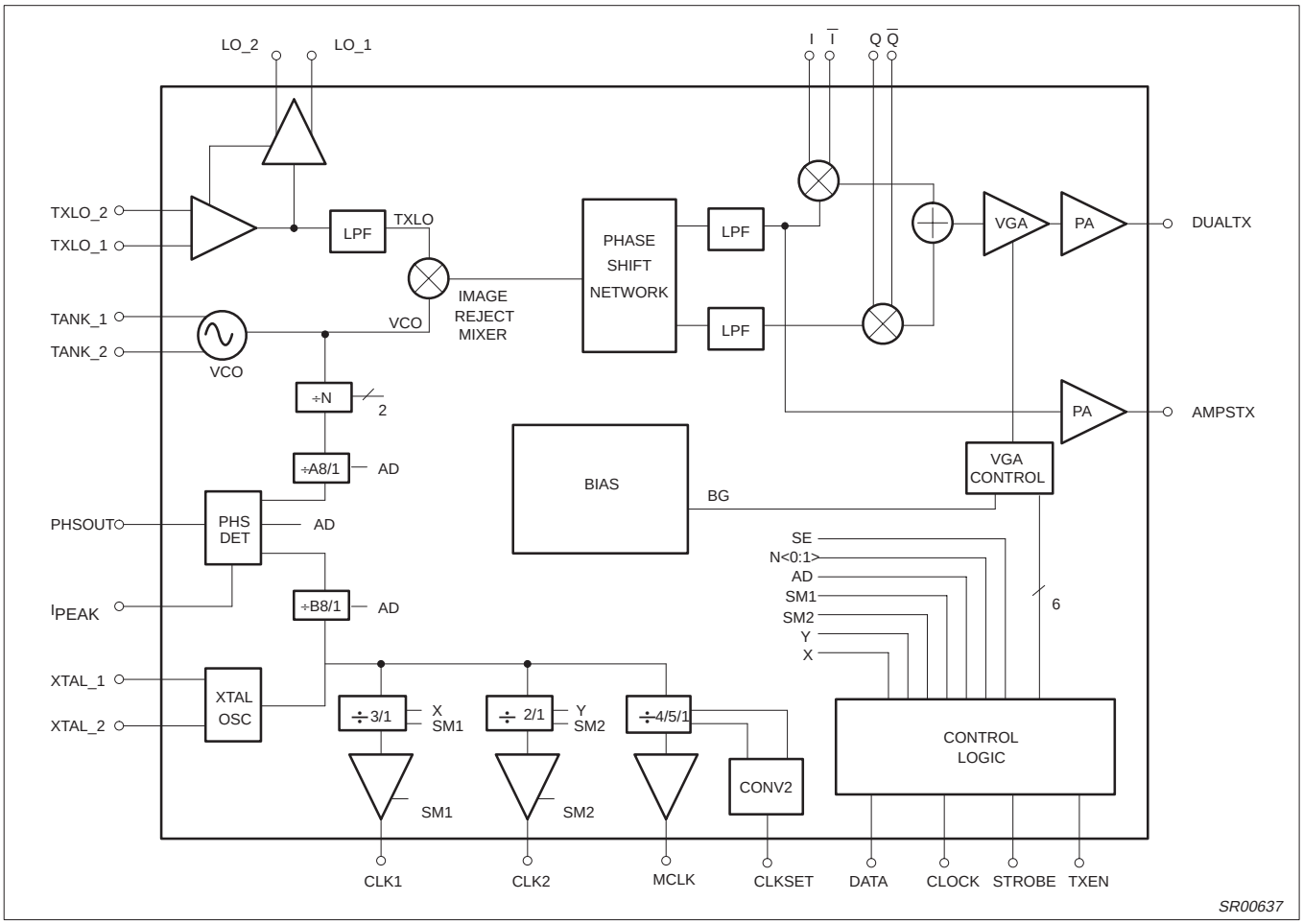


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin	Description
I	Non-inverting I Mod Signal
$\overline{I}$	Inverting I Mod Signal
TXLO_1/2	Second LO Input (differential/single-ended input)
DUALTX	RF output (850MHz) digital (DUAL) mode, complex modulated output
Q	Non-inverting Q Mod Signal
$\overline{Q}$	Inverting Q Mod Signal
CLK1	Buffered oscillator output (XO ÷3/÷1)
MCLK	Buffered oscillator output (XO ÷4/÷5/÷1)
CLK2	Buffered oscillator output (XO ÷2/÷1)
AMPSTX	RF output (850MHz) AMPS mode
V_{CC}	$+5V_{DC}$ power supply
GND	Ground
Data	Serial data input
Clock	Serial clock input
Strobe	Data strobe input
TXEN	AMPS and Dual Mode transmit enable
CLKSET	Program control pin for MCLK prescaler
XTAL1	Crystal oscillator base input
XTAL2	Crystal oscillator emitter output
PHSOUT	Phase comparator charge pump output
TANK_1	VCO differential tank
TANK_2	VCO differential tank
LO_1/2	Buffered differential TXLO output
I_{PEAK}	Phase comparator current programming

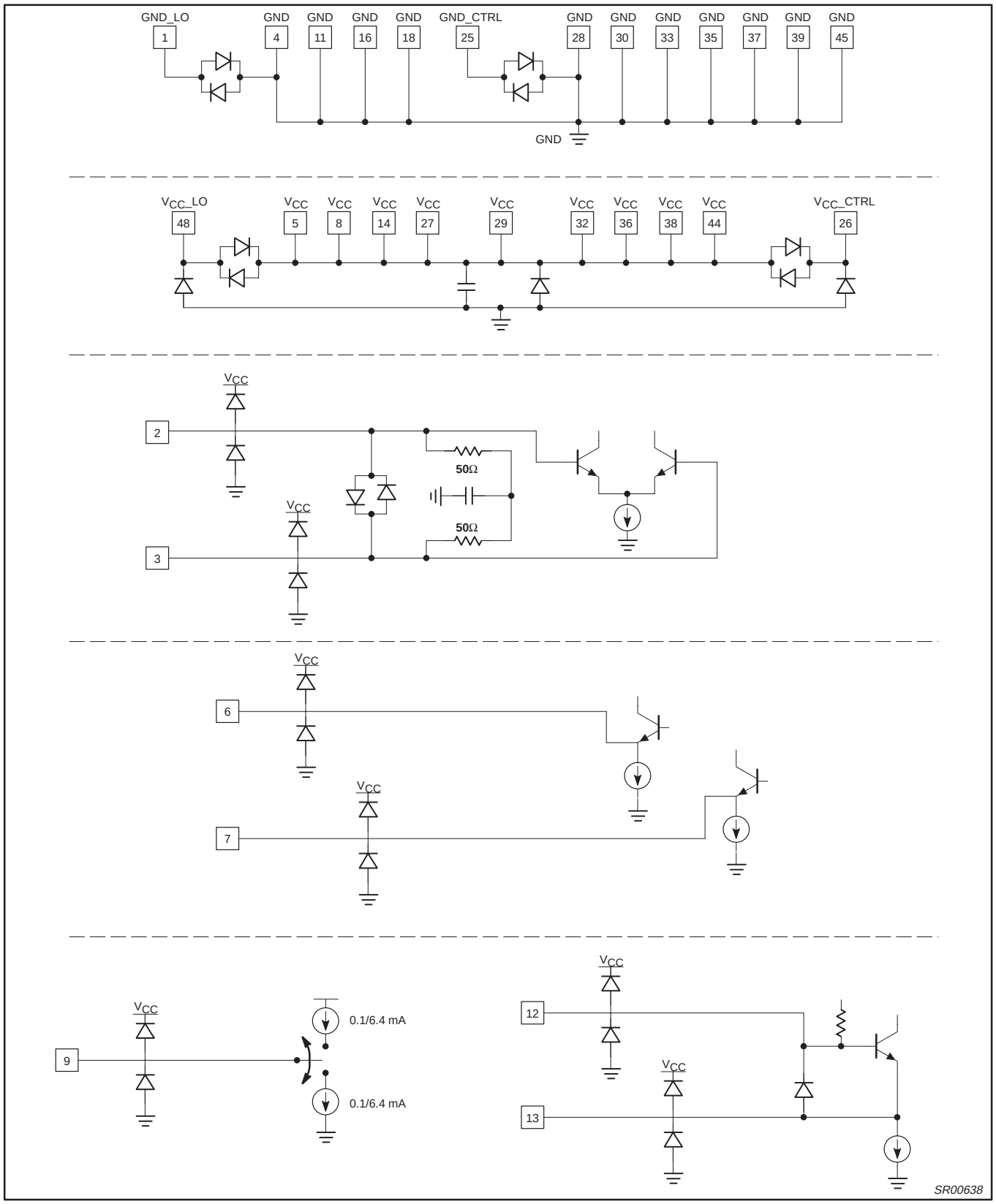


Figure 3. Pin Diagrams

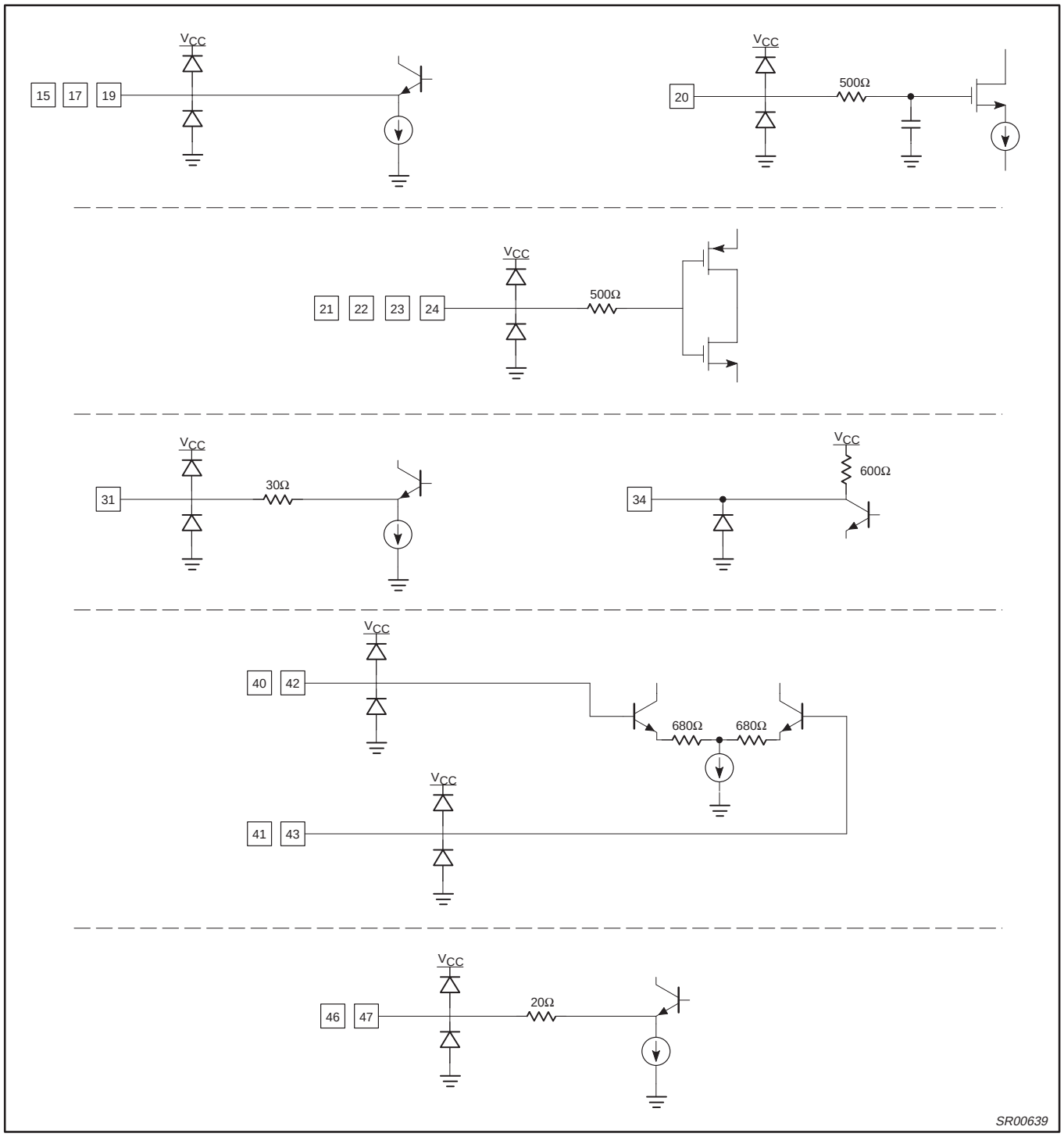


Figure 4. Pin Diagrams (cont.)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)	600	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+10	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}.
   48-pin LQFP: θ_{JA} = 67°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	3.9 to 5.1	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		3.9		5.1	V
I_{CC}	Supply current	Sleep mode		3.1		mA
		Standby mode		8.2		
		AMPS mode		27.5		
		DUAL mode		64		
I / $\overline{I}$	In-phase differential baseband input	DC		0.5V_{CC}		V
Q / $\overline{Q}$	Quadraphase differential baseband input	DC		0.5V_{CC}		V
CLKSET	Divide by 4/5/1	÷ 4		V_{CC}		V
		÷ 5		0.5V_{CC}		
		÷ 1		0		
V_{IL}	Clock, data, strobe, TXEN	Input low	–0.3		0.3V_{CC}	V
V_{IH}	Clock, data, strobe, TXEN	Input high	0.7V_{CC}		V_{CC}+0.3	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.0V, T_A = 25°C; TANK_1 = 120MHz @ 0 dBm; XO_REF = 30MHz @ –5 dBm; TxLO2 = –13 dBm, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
TXLO_1/2	Transmit LO input (AC couple) (50Ω)	Input power	-13		-10[1]	dBm
		VSWR (50Ω)		2:1		
		Frequency range	900		1040	MHz
TANK_1/2	VCO tank differential inputs	Frequency range	90[1]	120	140[1]	MHz
PHSOUT	Phase detector charge pump output	Output level	0.5		V_{CC}–0.5	V
I_{PEAK}	PHSOUT programming	R_{SET} = 24kΩ, AD=0	200	300	400	µA
		R_{SET} = 24kΩ, AD=1	0.9	1.2	1.5	mA
XTAL_1	XO transistor base	XO frequency	10[1]	30	45[1]	MHz
		External drive	150[1]	350	500[1]	mV_{P-P}
CLK1	XO divide 3/1, power down SM1=0, 50% duty cycle	Frequency range	3.33[1]	30	45[1]	MHz
	÷3, X=1, ÷1, X=0	Output level, 5kΩ || 7pF	0.7	1	1.4	V_{P-P}
CLK2	XO divide 2/1, power down SM2=0	Frequency range	5[1]	30	45[1]	MHz
	÷2, Y=1, ÷1, Y=0	Output level, 5kΩ || 7pF	0.7	1	1.4	V_{P-P}
MCLK	XO divide 4/5/1, 50% duty cycle	Frequency range	2[1]		45[1]	MHz
	÷4, CLKSET = V_{CC}, ÷5, CLKSET = 0.5V_{CC}, ÷1, CLKSET = 0V	Output level, 5kΩ || 7pF	0.7	1	1.4	V_{P-P}
CLOCK	Serial data clock input, 33% duty cycle	Max clock rate			10[1]	MHz
	Serial interface (CMOS levels)	Logic LOW			0.3V_{CC}[1]	V
	DATA, CLOCK, STROBE, TXEN	Logic HIGH	0.7V_{CC}			V
AMPSTX	AMPS output, SE=1, AD=0, TXEN=1 (AC couple)	Frequency range	820		860	MHz
		VSWR		2:1		
		Output level	–1.5	+2		dBm
	Spurious output	869 to 894MHz		-104		dBm
		824 to 849MHz		-47		dBc
		2 to 824MHz		-41		dBc
		849 to 869MHz		-41		dBc
		894MHz to 8.49GHz		-41		dBc
	TXLO and harmonics			-21		dBc
	Adjacent channel noise power	@30kHz		-95		dBc/Hz
	Alternate channel noise power	@60kHz		-101		dBc/Hz
	Broadband noise power	869 to 894MHz		-136		dBm/Hz
DUALTX	DUAL output, SE=1, AD=1, TXEN=1 (with external matching Figure 9)	Frequency range	820		920[2]	MHz
		VSWR		2:1		
		Output level (avg) (I and Q quad, 0dB VGA)	0	+2		dBm
		Gain flatness		1		dB

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DUALTX (cont.)	Linearity (0dB VGA, I and Q inphase)	3rd order	-35	-42		dBc
		5th order		-55		dBc
		7th order		-65		dBc
	Carrier suppression (I and Q quadrature)	VGA = 0dB	-35	-45		dBc
	Carrier suppression (I and Q quadrature)	VGA = –40dB	-28	-33		dBc
	Sideband suppression	I and Q quadrature	-35	-45		dBc
	Spurious output	869 to 894MHz		–104		dBm
		824 to 849MHz		–47		dBc
		2 to 824MHz		–41		dBc
		849 to 869MHz		–41		dBc
		894MHz to 8.49GHz		–41		dBc
	TXLO and harmonics			–21		dBc
	Broadband noise (0dB VGA)	869 to 894MHz		–136		dBm/Hz
		935 to 960MHz		–136		dBm/Hz
	Adjacent channel noise power	@30kHz		–95		dBc/Hz
	Alternate channel noise power	@60kHz		–101		dBc/Hz
Q/$\overline{Q}$	Baseband quadrature differential input	Max frequency		0.8	2[1]	MHz
		Differential modulation level	0.6[1]	0.8	1.0[1]	V_{P-P}
		Differential input impedance	10[1]			kΩ
I/$\overline{I}$	Baseband inphase differential input	Max frequency		0.8	2[1]	MHz
		Differential modulation level	0.6[1]	0.8	1.0[1]	V_{P-P}
		Differential input impedance	10			kΩ
LO_1/2	Buffered TXLO differential outputs (AC coupled)	Frequency range	900		1040	MHz
		VSWR (single-ended)		2:1		
	Output impedance	single-ended		50		Ω
		differential		100		Ω
	Output level	single-ended, 50Ω	50	90		mV_{P-P}
		differential, 100Ω	100	180		mV_{P-P}

NOTES:
1. Guaranteed by design.
2. Needs a different matching component. Max test frequency is 850MHz with test circuit shown in Figure 11.

FUNCTIONAL DESCRIPTION

Dual Mode Operation

The SA900 transmit modulator provides direct single sideband quadrature modulation of the difference of the TXLO and VCO frequencies, while providing quadrature LO signals for the I/Q modulator. The quadrature LO signals are modulated with high linearity by the baseband inphase (I) and quadrature (Q) signals. The summed modulator output produces the lower sideband, while rejecting the upper sideband. The I and Q inputs also provide DC biasing for the modulator inputs. The summed output of the modulator goes to a variable gain amplifier (VGA) to control the output level, it has 40.0dB of attenuation control range, with 0.63dB steps. The power control function is programmed by means of a 6-bit word (see Table 3). The VGA output drives the power amp output stage to provide +2dBm average minimum power level (at 0dB power control) into 50Ω, in conjunction with external matching components on DUALTX. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the DUAL mode function. The transition of the TXEN, from low to high turns on the modulator. The falling edge of the TXEN signal disables the synthesizer and modulator. The TXLO is a system supplied LO signal. The SA900 buffers the TXLO signal (LO_1/2) for use with the system synthesizer (such as the SA7025) to form the system LO synthesizer loop. The DUAL mode can also be used for AMPS operation. The AMPS and DUAL mode modulation is generated by the system DSP IC to provide the required I/Q baseband modulation for the SA900. The DUAL output provides low broadband noise output power (so that the receiver sensitivity is not degraded) and high linearity to meet cellular phone system needs. Table 1 provides the VGA power control limits.

The SA900 DUALTX output is externally matched with either a shunt inductor to V_{CC} and a series capacitor or a shunt inductor to V_{CC} and a series inductor. This matches the DUALTX output to 50Ω. Values of the matching components are dependent on PCB layout, typical values are shown in Figure 9.

Table 1. VGA Power Control Limits

VGA	Min.	Typ.	Max.	Relative VGA
0	0	0	0	0
1	-1	-.63	-.2	0
2	-1	-.63	-.2	1
3	-1	-.63	-.2	2
4	-1	-.63	-.2	3
5	-1	-.63	-.2	4
6	-1	-.63	-.2	5
7	-1	-.63	-.2	6
15	-6.6	-5	-3	7
23	-6.6	-5	-3	15
31	-6.6	-5	-3	23
39	-6.6	-5	-3	31
47	-6.6	-5	-3	39
55	-6.6	-5	-3	47
63	-6.6	-5	-3	55
63	-43.2	-40.4	-37.2	0

1. Guaranteed to be monotonic.

AMPS Mode Operation

The SA900 can be configured to operate in the AMPS mode, where FM modulation is applied to the SA900's VCO. For the AMPS mode, the VCO is configured with the proper synthesizer bandwidth to allow the application of the AMPS modulation to the VCO varactor tuned tank circuit. The modulated VCO signal is input into an image reject mixer along with the TXLO signal, where the upper sideband is rejected. This single sideband modulated signal then drives the AMPS output power amplifier. The PA provides +2dBm power level into 50Ω, with no external matching components required. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the AMPS mode function. The transition of the TXEN signal from low to high turns on the modulator. The falling edge of TXEN signal disables the synthesizer and the modulator.

Synthesizer Operation

The SA900 synthesizer is comprised of the differential VCO circuit, with external tank components, the Gilbert cell multiplier phase detector with programmable charge pump current, crystal oscillator and programmable prescalers. The charge pump output drives an external second order loop filter. The output of the loop filter is used to provide the control voltage to the VCO tuning varactor to complete the PLL synthesizer. The synthesized VCO output frequency is mixed with the TXLO signal to generate the transmit LO from the lower sideband (the difference of the VCO and TXLO frequencies). The output of VCO is fed to a programmable /N prescaler with user selectable divides of 6, 7, 8 and 9 (all divides configured to provide 50% duty cycle). The output of the /N divider drives the A8/1 prescaler. The A8/1 divide is selected by the AD control bit (AD=1 for /1, and AD=0 for /8). The output of the divide A8/1 is fed into one input of the phase detector. The reference input for the phase comparator is generated from the crystal oscillator (XO) output from the B8/1 prescaler. The B8/1 divide is selected by the AD control bit (AD=0 for /8, and AD=1 for /1). The phase detector compares the prescaled XO reference phase to the VCO prescaled phase, to generate a charge pump output current proportional to the phase error. The phase detector, a Gilbert cell multiplier type, having a linear output from 0 to π (π/2 ± π/2). The charge pump peak output current is programmable from 100µA for the AMPS mode (AD=0) to a maximum of 6.4mA for the DUAL mode (AD=1) by way of an external current setting resistor placed from I_{PEAK} to circuit ground. The typical loop filter network is shown in Figure 5. The charge pump current output is programmed by

$$AD = 0 \qquad I_{OUT} = 6 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

$$AD = 1 \qquad I_{OUT} = 24 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

where R_{SET} is placed between I_{PEAK} and GROUND.

The PLL frequency is determined by

$$VCO = XO \cdot N \cdot \frac{(\frac{A8}{1})}{(\frac{B8}{1})}$$

where N=6, 7, 8, 9 and A8/1 and B8/1 are controlled by the AD bit (AD=1 A8/1 and B8/1 are divide by 1, AD=0 A8/1 and B8/1 are divide 8).

Table 2. Data Word Format

Mnemonics	Bits	Function
A0	1 (MSB)	Address bit 0 (1)
A1	2	Address bit 1 (0)
A2	3	Address bit 2 (1)
A3	4	Address bit 4 (1)
PC0	5	Power control bit 0
PC1	6	Power control bit 1
PC2	7	Power control bit 2
PC3	8	Power control bit 3
PC4	9	Power control bit 4
PC5	10	Power control bit 5
N0	11	Divide N bit 0
N1	12	Divide N bit 1
AD	13	AMPS/DUAL mode select bit
SE	14	Synthesizer enable bit
NA	15	NA
SM1	16	Sleep mode 1 control bit
SM2	17	Sleep mode 2 control bit
X	18	Divide 3/1 control bit
Y	19	Divide 2/1 control bit
NA	20	NA
NA	21	NA
NA	22	NA
NA	23	NA
NA	24 (LSB)	NA

VCO Operation

The VCO is designed to operate from 90MHz to 140MHz. The VCO tank is configured using a parallel inductor and a dual common cathode tuning varactor diodes. DC blocking capacitors are used to isolate the varactor

control voltage from the VCO tank DC bias voltages. The VCO tuning voltage is generated from the output of the PLL loop filter. The VCO tank configuration is shown in Figure 6.

Crystal Oscillator (XO) Operation

For cellular radio applications, the SA900 will most likely utilize an external reference TCXO in order to provide the frequency stability necessary to operate to system requirements. The output of the system TCXO can be AC coupled to the XTAL_1 input. However, for applications that do not require such accuracy the XO circuit can be configured as a Colpitts type oscillator with the addition of two external capacitors along with the reference crystal and a trim capacitor as shown in Figure 7.

Programmable Clock Outputs

The SA900 generates three buffered XO outputs used for external reference signals. The XO feeds three sets of programmable prescalers, the prescaler outputs are buffered to provide the CLK1, CLK2 and MCLK signals. The CLK1 signal is a selectable divide 3/1 (X=1 divide 3, X=0 divide 1), 50% duty cycle, of the XO reference signal. The CLK2 signal is a selectable divide 2/1 (Y=1 divide 2, Y=0 divide 1), 50% duty cycle, of the XO reference signal. The MCLK signal is a selectable divide 4/5/1 (CLKSET = V_{CC} divide 4, CLKSET = V_{CC}/2 divide 5, and CLKSET = 0V divide 1), 50% duty cycle, of the XO reference signal. MCLK is externally set by means of the tri-level CLKSET input to provide a default master system clock prior to programming the SA900.

Programming Operation

The SA900 is configured by means of a 3-wire input (CLOCK, STROBE, DATA) to program the AMPS and DUAL modes, in addition there are two power saving modes of operation, SLEEP and STANDBY. The control logic section of the SA900 is designed using low power CMOS logic. During SLEEP mode only the circuitry required to provide a master clock (MCLK) to the digital portion of the system is enabled. During the STANDBY mode of operation MCLK, CLK1 and the TXLO and buffered LO outputs are powered on, which may be the case when the system is in the receive only mode. In the AMPS or DUAL operational modes all functions of the SA900 are powered on to support receive, transmit and system clock functions. The programming of the SA900 is identical to the programming format of the SA7025 low-voltage 1GHz fractional-N synthesizer, that can be used in conjunction with the SA900 to provide the cellular radio channel selection.

The programming data is structured as a 24 bit long serial data word; the word includes 4 address bits (dedicated 1 0 1 1) for chip select. Data bits are shifted in on the leading edge of the clock, with the least significant bit (LSB) first and the most significant bit (MSB) last. Table 2 shows data word format, the 15th and last 5 bits are not used. Figure 8 shows the chip timing diagram.

Address

A0	A1	A2	A3
1	0	1	1

Divide By N

N0	N1	Divide
0	0	6
1	0	7
0	1	8
1	1	9

AMPS/DUAL Mode

The A/D mode select enables or disables that portion of the circuitry used for either the AMPS or DUAL mode of operation.

AD	Mode
0	AMPS
1	DUAL

Synthesizer Enable

The SE bit turns on and off the synthesizer circuitry.

SE	Operation
0	Disabled
1	Enabled

Sleep Mode 1

The SM1 bit is used to power down the TXLO buffer, the divide 3/1 prescaler and the CLK1 output buffer.

SM1	Operation
0	Power down
1	Power up (STANDBY)

Sleep Mode 2

The SM2 bit is used to power down the divide 2/1 prescaler and the CLK2.

SM2	Operation
0	Power down
1	Power up (with SM1=1 normal operation)

Divide 3

X	Operation
0	Divide 1
1	Divide 3

Divide 2

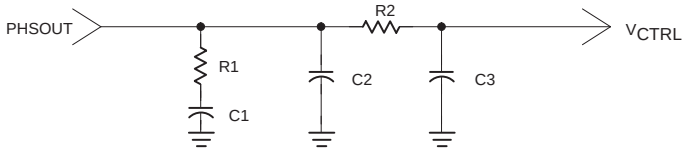
Y	Operation
0	Divide 1
1	Divide 2

Table 3. Power Control

Attenuation (dB)	PC0 (0.6dB)	PC1 (1.3dB)	PC2 (2.5dB)	PC3 (5.0dB)	PC4 (10.0dB)	PC5 (20.0dB)
0	0	0	0	0	0	0
0.6	1	0	0	0	0	0
1.3	0	1	0	0	0	0
1.9	1	1	0	0	0	0
2.5	0	0	1	0	0	0
3.2	1	0	1	0	0	0
3.8	0	1	1	0	0	0
4.4	1	1	1	0	0	0
5.0	0	0	0	1	0	0
5.7	1	0	0	1	0	0
6.3	0	1	0	1	0	0
• • •						
23.3	1	0	1	0	0	1
• • •						
39.7	1	1	1	1	1	1

Component Designator	Value	
	DUAL Mode	AMPS Mode
R1	560Ω	560Ω
R2	1kΩ	5.6kΩ
C1	2.2nF	2.7µF
C2	No Load	.27µF
C3	33pF	6.8nF
R_{SET}	15kΩ	75kΩ

Typical Filter Network



SR00640

Figure 5. PLL Loop Filter

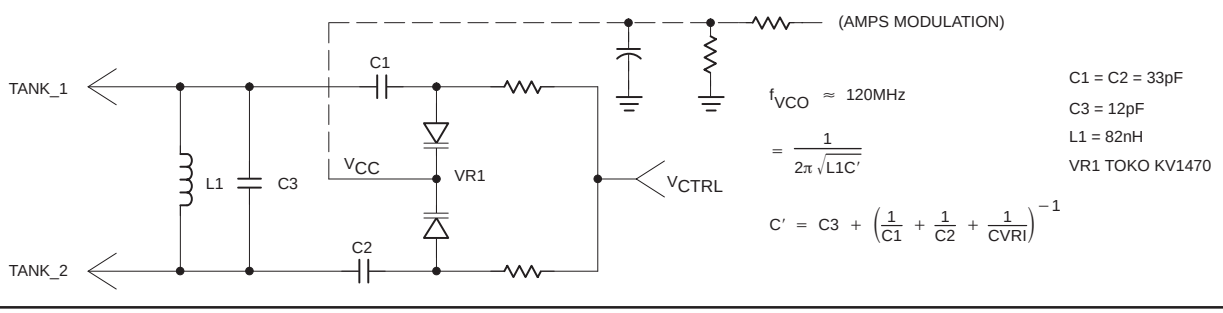


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Figure 6. VCO Tank Configuration

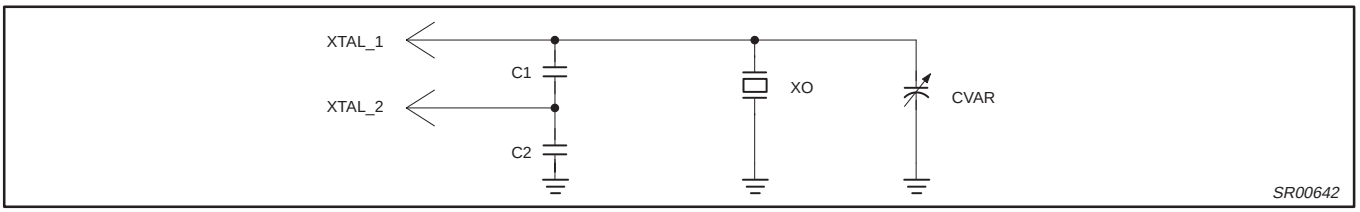


Figure 7. Crystal Oscillator Configuration

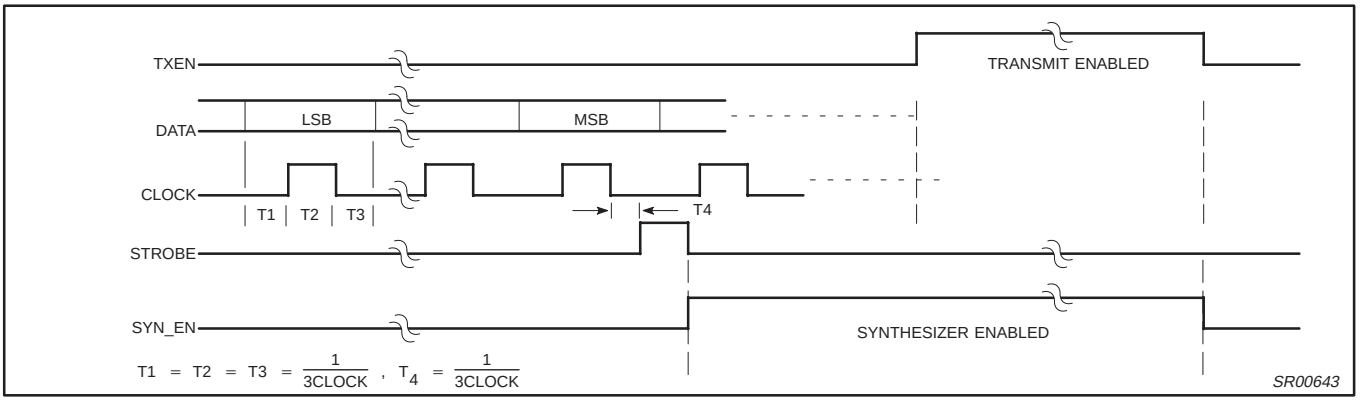


Figure 8. Chip Timing Diagram

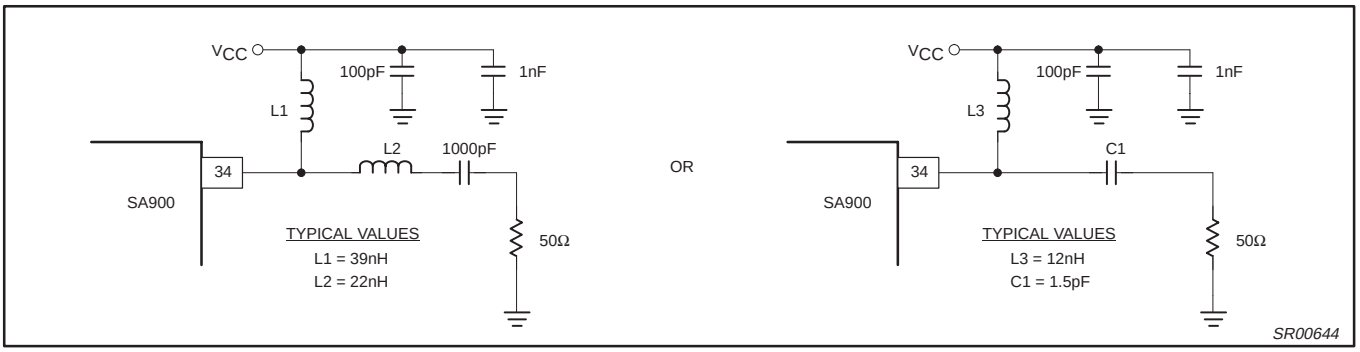


Figure 9. DUALTX Output Matching

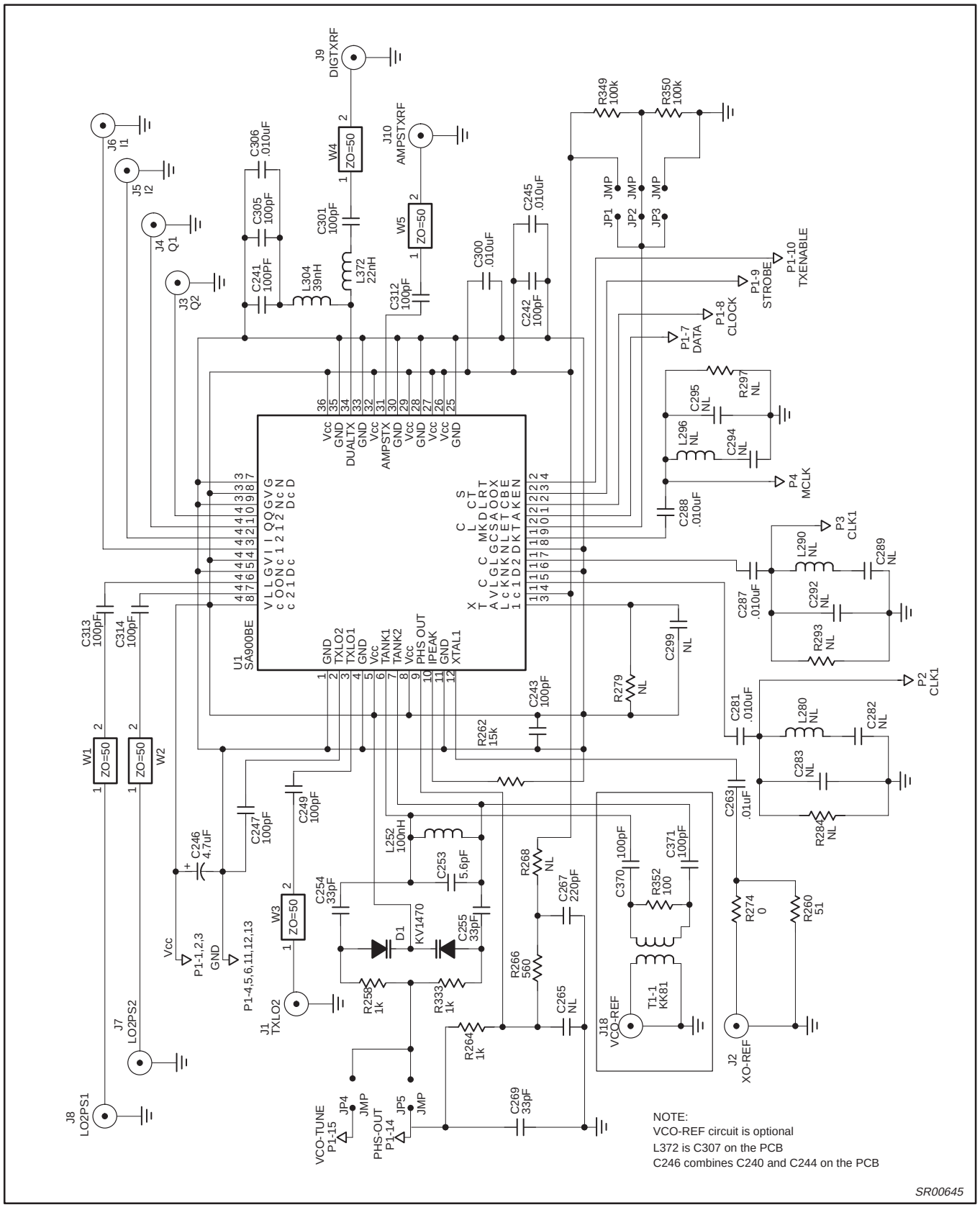


Figure 10. SA900 Application Circuit

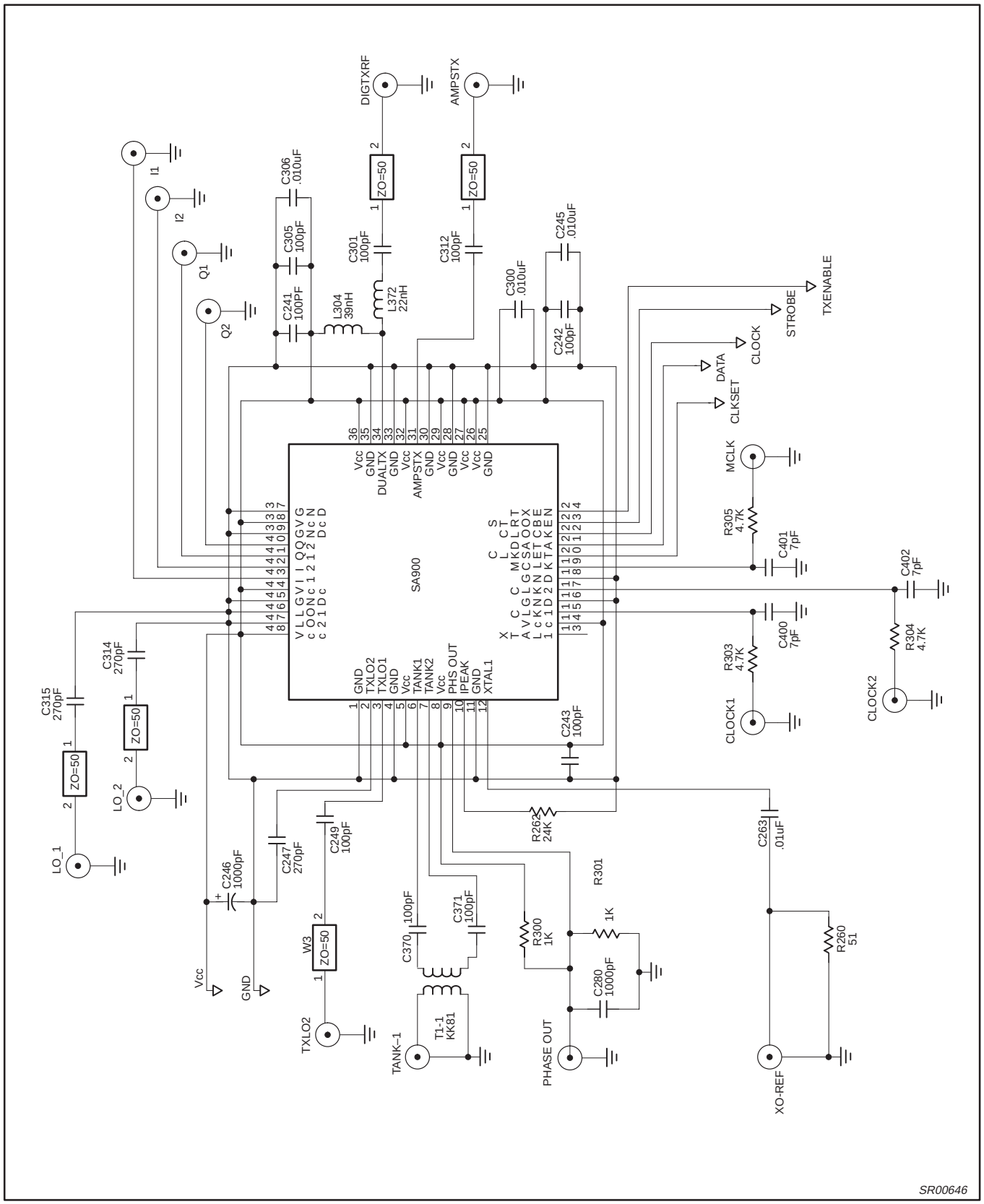
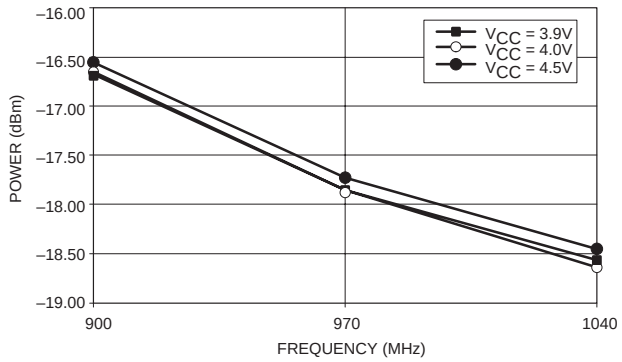
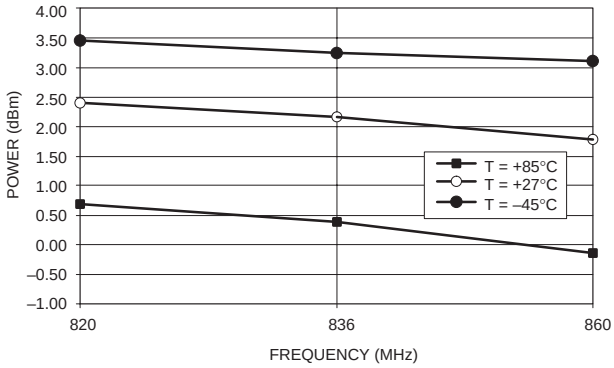


Figure 11. SA900 Test Circuit

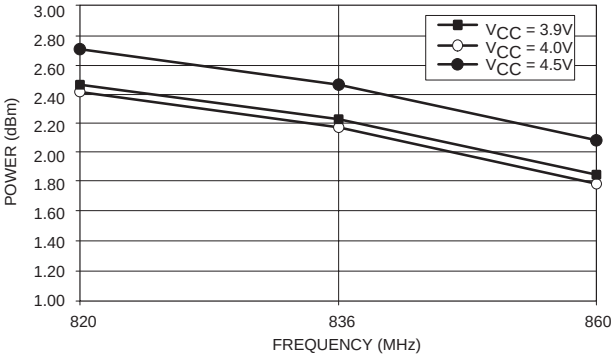
PERFORMANCE CHARACTERISTICS



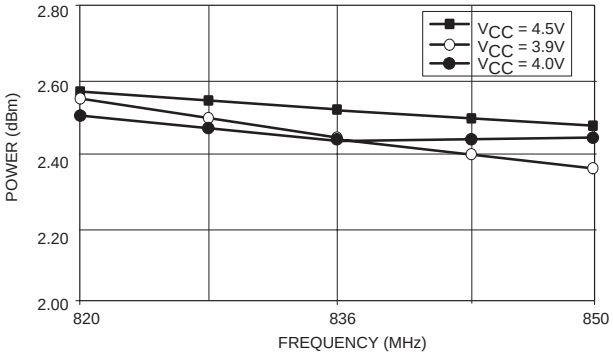
LO Buffer vs. Frequency (27°C, TXLO = –10dBm)



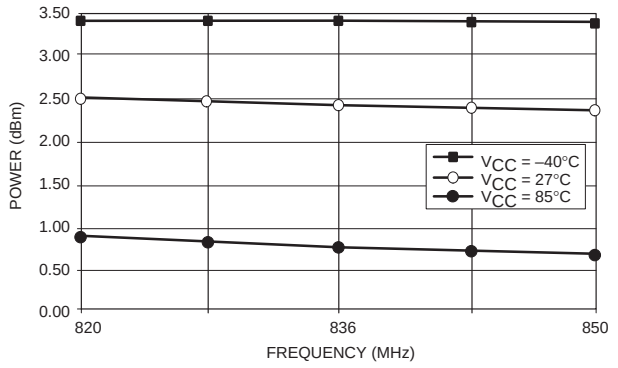
AMPTX vs. Frequency (V_{CC} = 4.0V, TXLO = –10dBm)



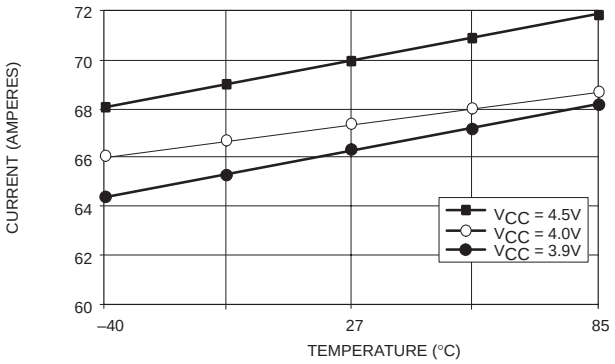
AMPTX vs. Frequency (27°C, TXLO = –10dBm)



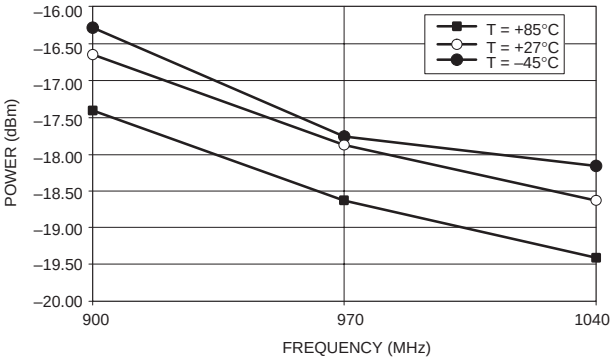
DUALTX vs. Frequency (TEMP 27°C, TXLO = –10dBm)



DUALTX vs. Frequency (V_{CC} = 4.0V, TXLO = –10dBm)



DUAL I_{CC} vs. Temperature

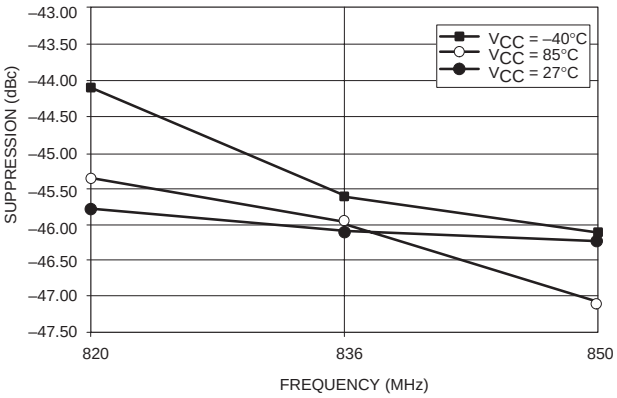


LO Buffer vs. Frequency (V_{CC} = 4.0V, TXLO = –10dBm)

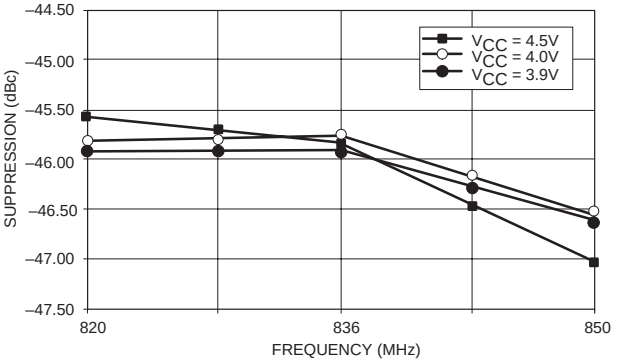
SR00647

Figure 12. Performance Characteristics

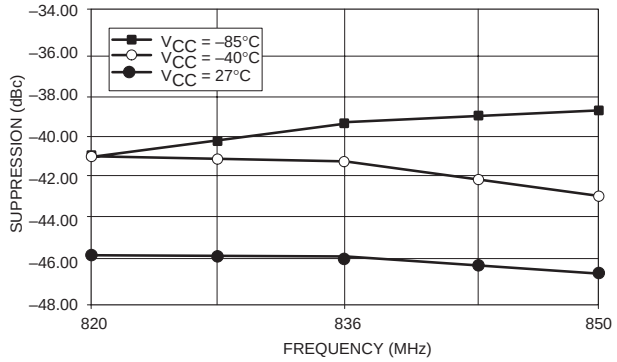
PERFORMANCE CHARACTERISTICS



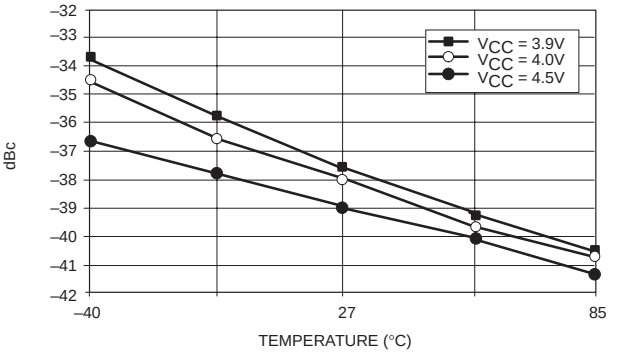
DUALTX Carrier Suppression vs. Frequency (V_{CC} = 4.0, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



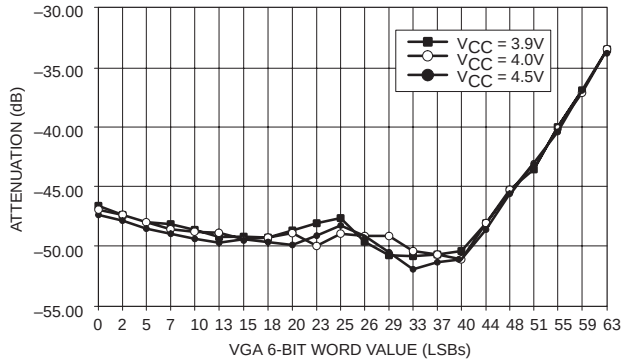
DUALTX Sideband Suppression vs. Frequency (Temperature = 27°C, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



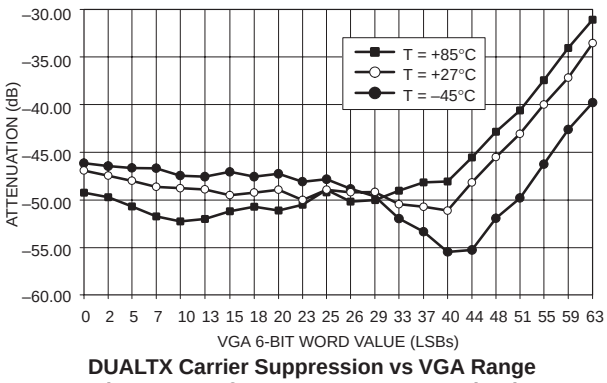
DUALTX Sideband Suppression vs Frequency (V_{CC} = 4.0V, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



DUALTX 3rd Order Products vs Temperature (TXLO = –10dBm, f = 836MHz, 0dB VGA I/Q Inphase)



DUALTX Carrier Suppression vs VGA Range (27°C, f = 836MHz, TXLO = –10dBm)



DUALTX Carrier Suppression vs VGA Range (V_{CC} = 4.0V, f = 836MHz, TXLO = –10dBm)

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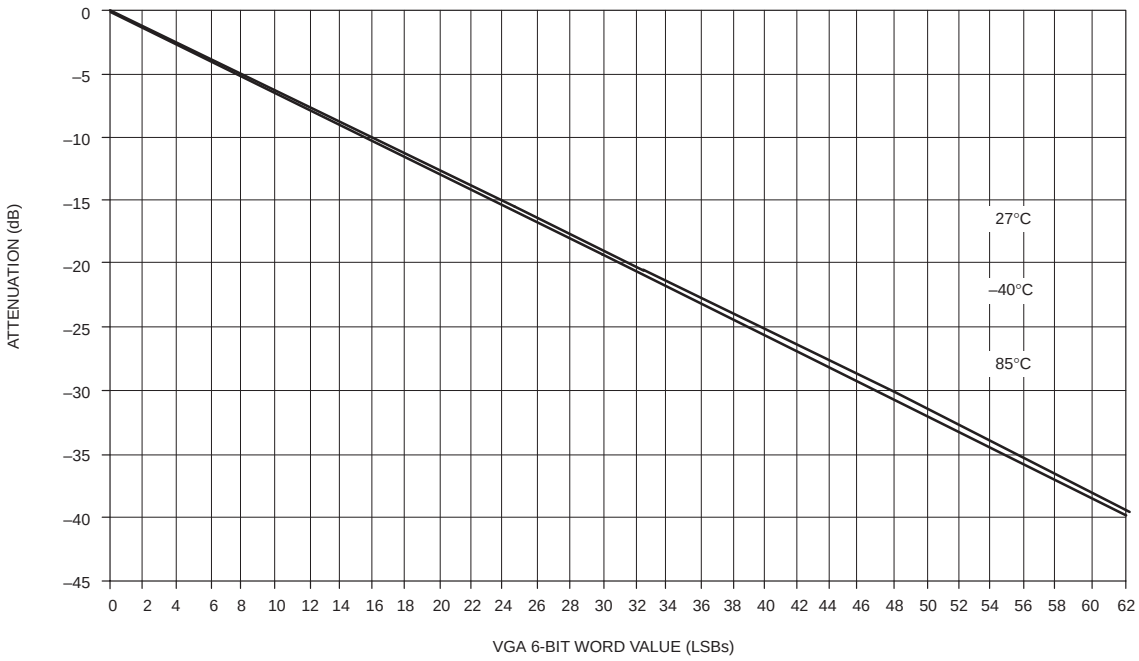
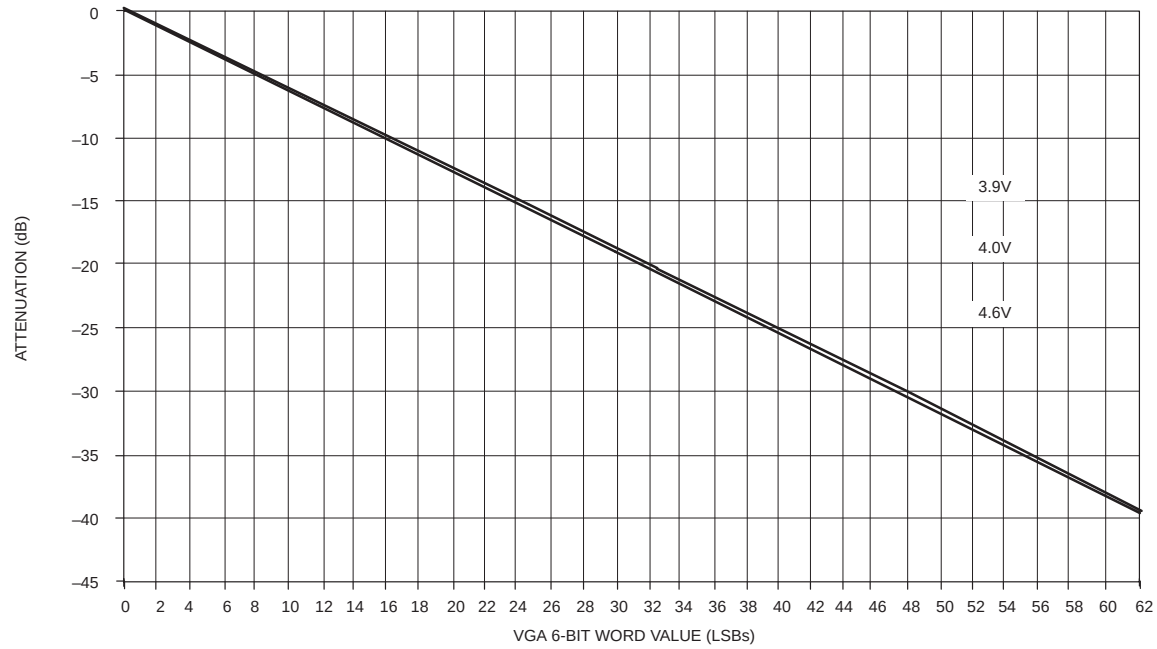
Figure 13. Performance Characteristics

PERFORMANCE CHARACTERISTICS



DUALTX VGA Attenuation Profile vs. Temperature (V_{CC} = 4.0V, F = 836MHz)



DUALTX VGA Attenuation Profile vs. V_{CC} (T = 27°C, F = 836MHz)

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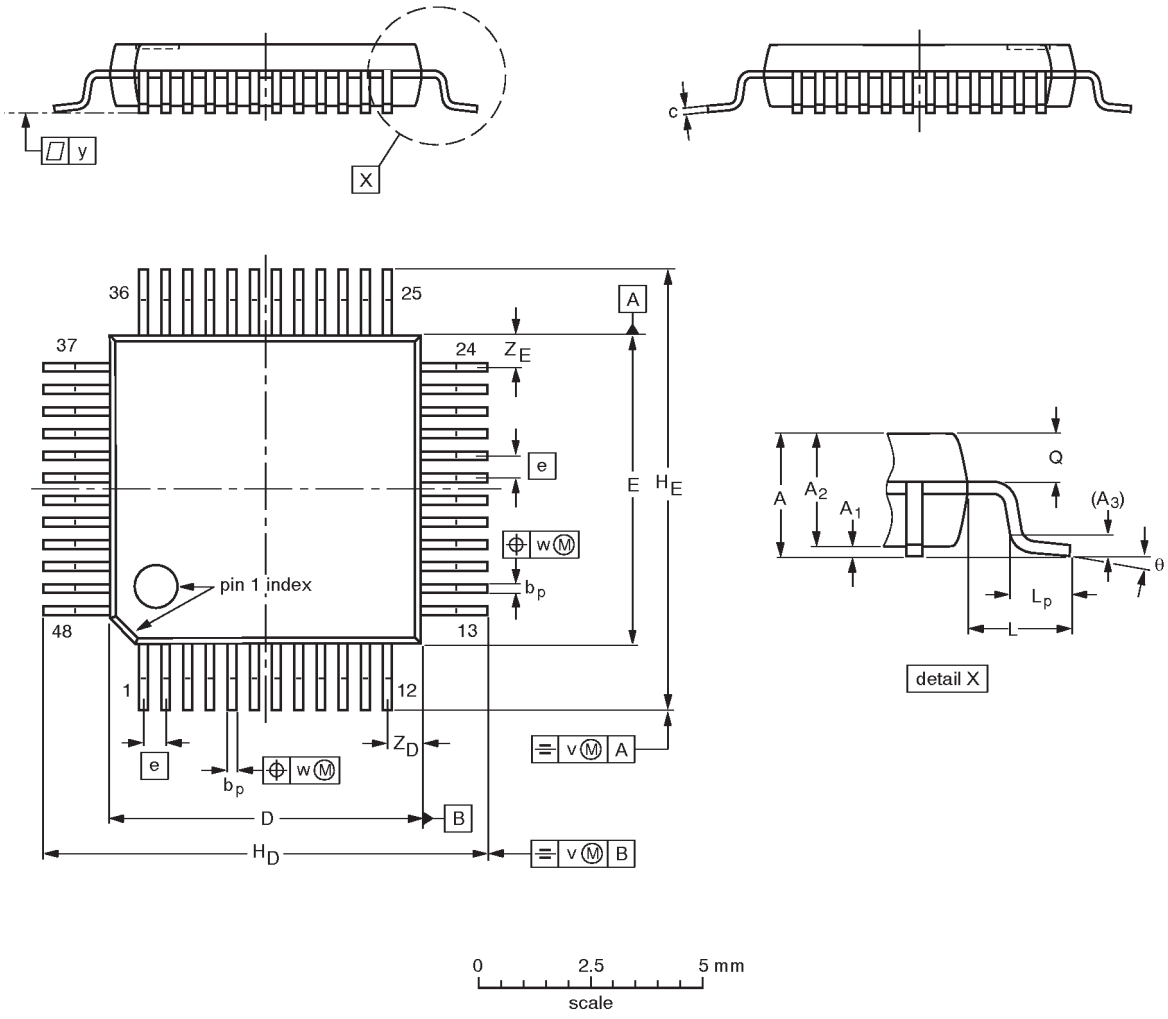
Figure 14. Performance Characteristics

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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