INTEGRATED CIRCUITS

DATA SHEET

SA910Variable gain RF predriver amplifier

Product specification





Variable gain RF predriver amplifier

SA910

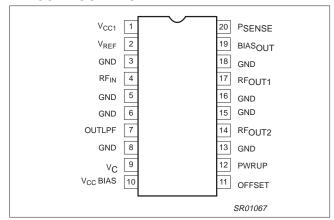
DESCRIPTION

The SA910 is a variable gain predriver amplifier designed for handheld analog cellular telephones. When used with a UHF power transistor, it forms a cost-effective, low-profile, surface mount power amplifier solution (1.2W maximum PAE > 50%). The SA910 integrates power detection and control circuitry that is stabilized over temperature and voltage. In power down mode, the SA910 draws less than $10\mu A$ of current. The SA910 is fabricated using Philips QUBiC BiCMOS process.

FEATURES

- MMIC BiCMOS predriver amplifier
- Low voltage 2.7 to 5.5V single supply operation
- 820 to 905MHz bandwidth
- High power gain >20dB
- High power output >23dBm (typical) @ 3V
- Efficiency = 35% (typical)
- Wide gain control range: >32dB
- Few external components required
- Integrated power detector and comparison gain control circuitry
- 50Ω input, open-collector output
- SSOP-20 package
- Integrated regulator with offset adjustment for biasing an external output stage

PIN CONFIGURATION



APPLICATIONS

- 900MHz analog cellular
- Handheld transmitting equipment in the 820 to 905MHz frequency range
- Cordless phone

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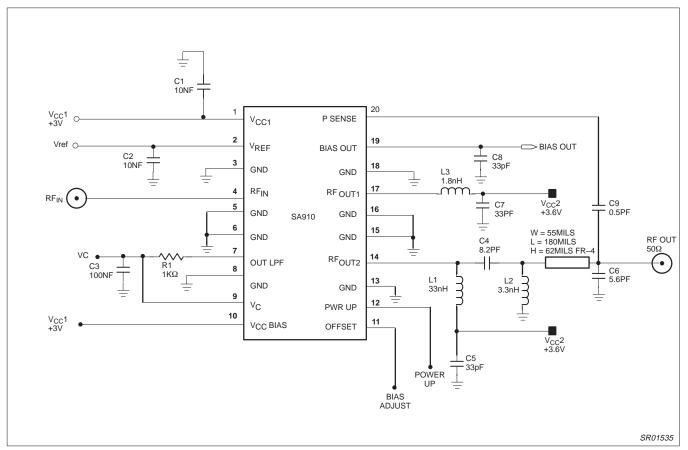


Figure 1. Application Diagram

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic SSOP (Shrink Small Outline Package)	-40 to +85°C	SA910	SOT266-1

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SA910

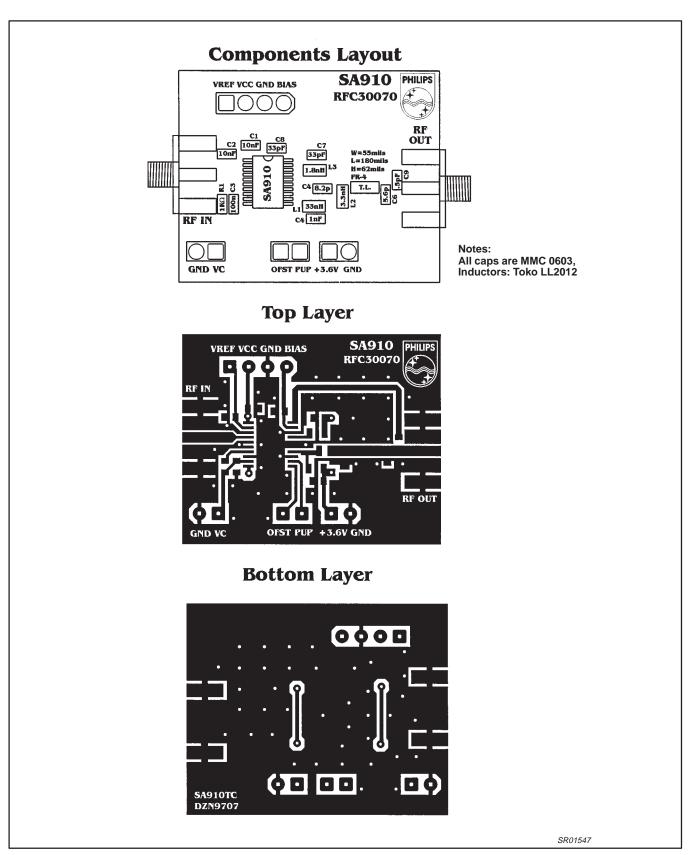


Figure 2. Application Board Layout of SA910

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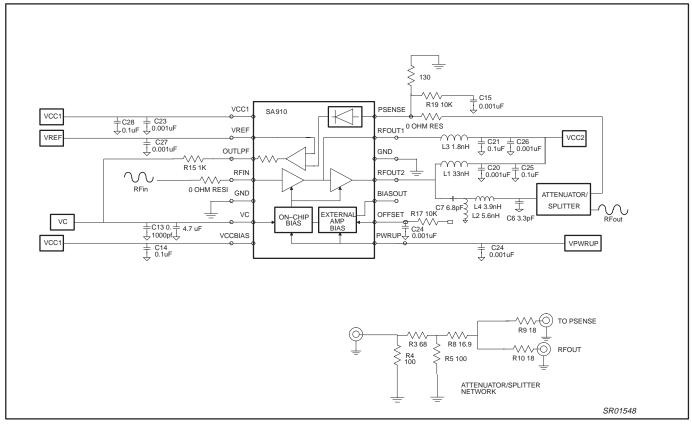


Figure 3. Test Circuit Used In Characterizing SA910

BLOCK DIAGRAM

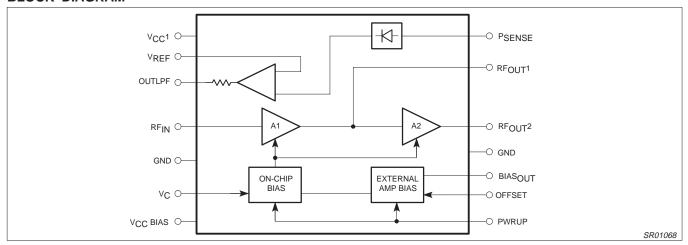


Figure 4. Block Diagram

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PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	V _{CC1}	Power supply for power sense loop and off-chip bias
2	V_{REF}	Power sense reference voltage input
3	GND	Ground
4	RF _{IN}	Pre-driver input
5	GND	Ground
6	GND	Ground
7	OUTLPF	Power sense detected output
8	GND	Ground
9	VC	Gain control input
10	V _{CC} BIAS	Power supply for on-chip bias
11	OFFSET	External power amp bias offset adjustment
12	PWRUP	Power-up input
13	GND	Ground
14	RF _{OUT2}	Pre-driver output (open collector)
15	GND	Ground
16	GND	Ground
17	RF _{OUT1}	Output of first stage (open collector)
18	GND	Ground
19	BIAS _{OUT}	Output to bias external power amplifier stage
20	P _{SENSE}	Power sense input

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V _{CC} 1/V _{CC} BIAS	DC supply voltages	-0.3 to +6.0	V
	Voltage applied to any other pin ¹	-0.3 to (V _{CC} 1 + 0.3)	V
P _D	Power dissipation	1.0	W
P _{IN}	Input drive power	5	mW
P _{DET}	Input detect power	20	mW
PL	Load power	500	mW
T _{STG}	Storage temperature range	-65 to +150	°C

NOTE

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V _{CC} 1/V _{CC} BIAS	Supply voltage	3 to 3.6	V
T _A	Operating ambient temperature range	-40 to +85	°C

NOTE:

^{1.} Except RF $_{\rm OUT}$ 1 and RF $_{\rm OUT}$ 2 which can have 8V max.

^{1.} $R_{th} = 75^{\circ} \text{ c/w}$

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AC ELECTRICAL CHARACTERISTICS

 $V_{CC}1 = V_{CC} BIAS = +3V; V_{CC} (RF_{OUT}1, RF_{OUT}2) = 3.6V; T_A = 25^{\circ}C, Z_S = Z_L = 50\Omega; V_C = 2V; RF_{IN} = 0 dBm @ 830MHz; unless otherwise stated. \\$

CVMDOL	DADAMETED	TEST CONDITIONS		LIMITO			
SYMBOL	PARAMETER	1EST CONDITIONS	MIN	TYP	MAX	UNITS	
f _{RF}	Frequency range		820	830	905	MHz	
P_{L}	Load power at RF _{OUT2}	Saturated ¹	21.5	24		dBm	
S ₂₁	Small signal gain	RF _{in} = -20dBm		31		dB	
η	Power added efficiency	$P_L = 24dBm$		35		%	
S ₁₁	Input return loss	$RF_{in} = 0dBm$		-12		dB	
G _C	Gain control range from $V_c = 0.7$ to 2V	dP/dV <120dB/V	32			dB	
S ₁₂	Reverse isolation			-40		dB	
GOFF	Gain at RF _{OUT2} during power-down (RF _{IN} = -20dBm)			-30		dB	
PSENSE	Power detector range			25		dB	

^{1.} Needs proper output matching.

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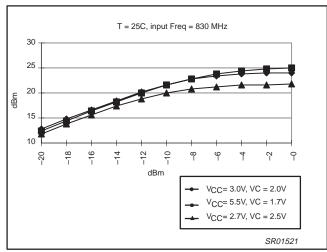
DC ELECTRICAL CHARACTERISTICS

 $V_{CC}1 = V_{CC}BIAS = ~+3V,~V_{CC}~(RF_{OUT}1,~RF_{OUT}2) = 3.6V;~T_{A} = 25^{\circ}C,~Z_{S} = Z_{L} = 50\Omega,~;~unless~otherwise~stated.$

CVMDOL	DADAMETER	TEST		UNITS					
SYMBOL	PARAMETER	CONDITIONS	MIN	-3 σ	TYP	+3 σ	MAX	UNIIS	
V _{CC}	Power supply voltage range		2.7		3.0		5.5	V	
Icc	Total DC current from all V _{CC}	Pin 12 = HIGH; Pin 9 > V _{BE}			210		300	mA	
I _{ZB}	I _{CC} under zero bias mode	Pin 12 = HIGH; Pin 9 < V _{BE}					0.7	mA	
I _{OFF}	Powerdown current	Pin 12 = LOW					10	μΑ	
,	Input ourrent to DWDID	Pin 12 = HIGH					100		
I _{PU}	Input current to PWRUP	Pin 12 = LOW					10	μΑ	
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Input level for DWDLID (Din 42)	Pin 12 = LOW	0				0.3V _{CC}	V	
V _{PU}	Input level for PWRUP (Pin 12)	Pin 12 = HIGH	0.7V _{CC}				V _{CC}	V	
I _{REF}	Input current to V _{REF} (Pin 2)						1	μΑ	
V _{REF}	Power control reference voltage (Pin 1)		0				2.0	V	
V _{BIAS}	Bias _{OUT} voltage (Pin 19) (unadjusted)	$V_{C} = 2.0V$			0.68			V	
I _{BIAS}	DC current available @ Bias-OUT (Pin 19)		30					mA	
V _C	Control voltage (Pin 9) range		0				2	V	

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V_{CC}1 = 3.0V· V_{CC}2 = 3.6V, INPUT FREQ = 830 MHZ

V_C = 2.0V

V_C = 2.0V

V_C = 2.0V

dBm

T = 27C

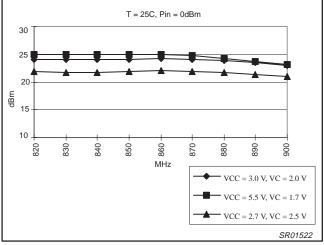
T = 85C

T = -40C

SR01524

Figure 8. PAE VS Input Power

Figure 5. Output Power VS Input Power



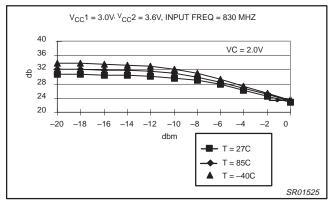
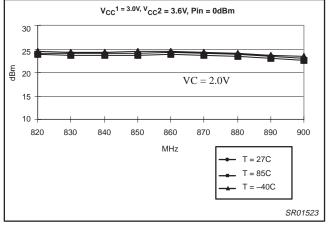


Figure 9. Signal Gain VS Input Power

Figure 6. Output Power VS Input Frequency



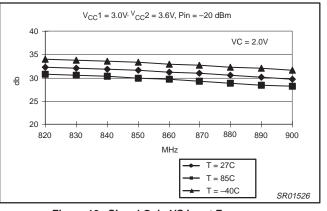


Figure 10. Signal Gain VS Input Frequency

Figure 7. Output Power VS Input Frequency

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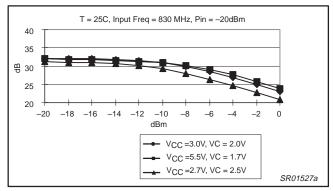


Figure 11. Signal Gain VS Input Power

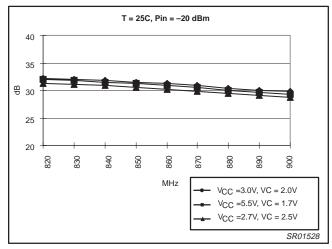


Figure 12. Signal Gain VS Input Frequency

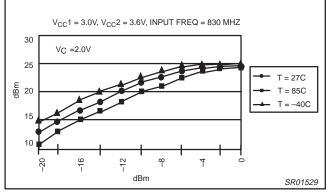


Figure 13. Output Power VS Input Power

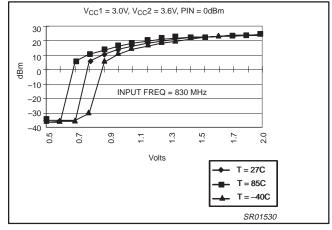


Figure 14. Output Power VS VC

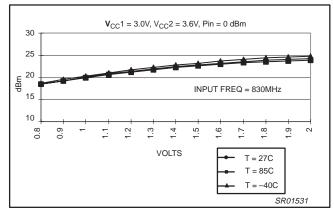


Figure 15. Output Power VS VREF (Closed Loop)

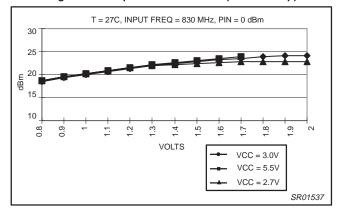


Figure 16. Output Power VS VREF (Closed Loop)

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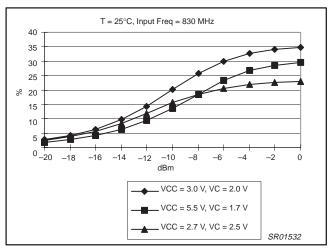
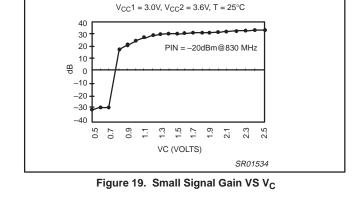


Figure 17. PAE VS Input Power



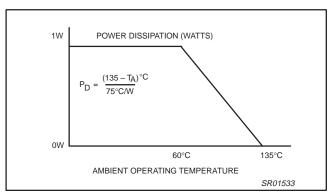


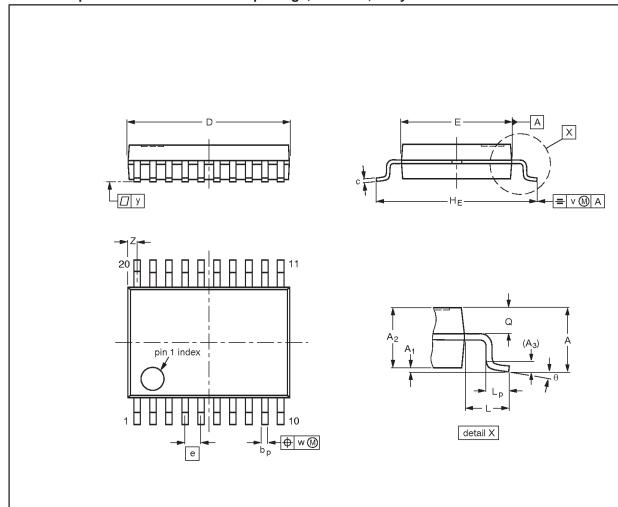
Figure 18. Power De-Rating Curve

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SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	c	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE		REFER	ENCES		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT266-1						-90-04-05- 95-02-25

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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