

# DATA SHEET

## **SAA1502ATS** Safety IC for Li-ion

Preliminary specification  
File under Integrated Circuits, IC11

1998 Jan 15

**Safety IC for Li-ion****SAA1502ATS****FEATURES**

- Integrated power switches
- Temperature protection
- Zero voltage start-up
- Discharge and charge overcurrent protection
- Automatic release of current protection at removal of charger or load
- Extremely low current consumption when battery voltage is lower than 2.3 V
- Low current consumption in normal operation mode
- Accurate voltage detection levels
- Low resistance in current path
- Able to accommodate 17.5 V charge voltage
- Read out of charge disable status
- Small package (SSOP16)
- Low external components count
- Continuous monitoring of the battery voltage and (dis)charge current.

**GENERAL DESCRIPTION**

The SAA1502ATS is manufactured in a Bipolar, CMOS and DMOS (BCD) Power Logic 70 process and is intended to be used as a protection circuit for single cell Li-ion battery packs. The current and voltage ratings are especially designed for use in battery packs for portable telephones such as GSM.

The circuit monitors the battery voltage, current and temperature and will disconnect the battery in case of an overload situation:

- Overdischarge protection prevents deep discharge of the cell; deep discharge of a Li-ion cell degrades the lifetime
- Overcharge protection for safety reasons
- Overcurrent protection on charge as well as discharge current rate
- Temperature protection for preventing charge or discharge at high temperatures.

It must be stated that the unit is a safety unit to be integrated inside a battery pack. It is not intended as an end of charge provision.

**ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |   |          |
|-------------|---------|---|----------|
|             | NAME    | DESCRIPTION   | VERSION  |
| SAA1502ATS  | SSOP16  | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |

# Safety IC for Li-ion

# SAA1502ATS

## BLOCK DIAGRAM

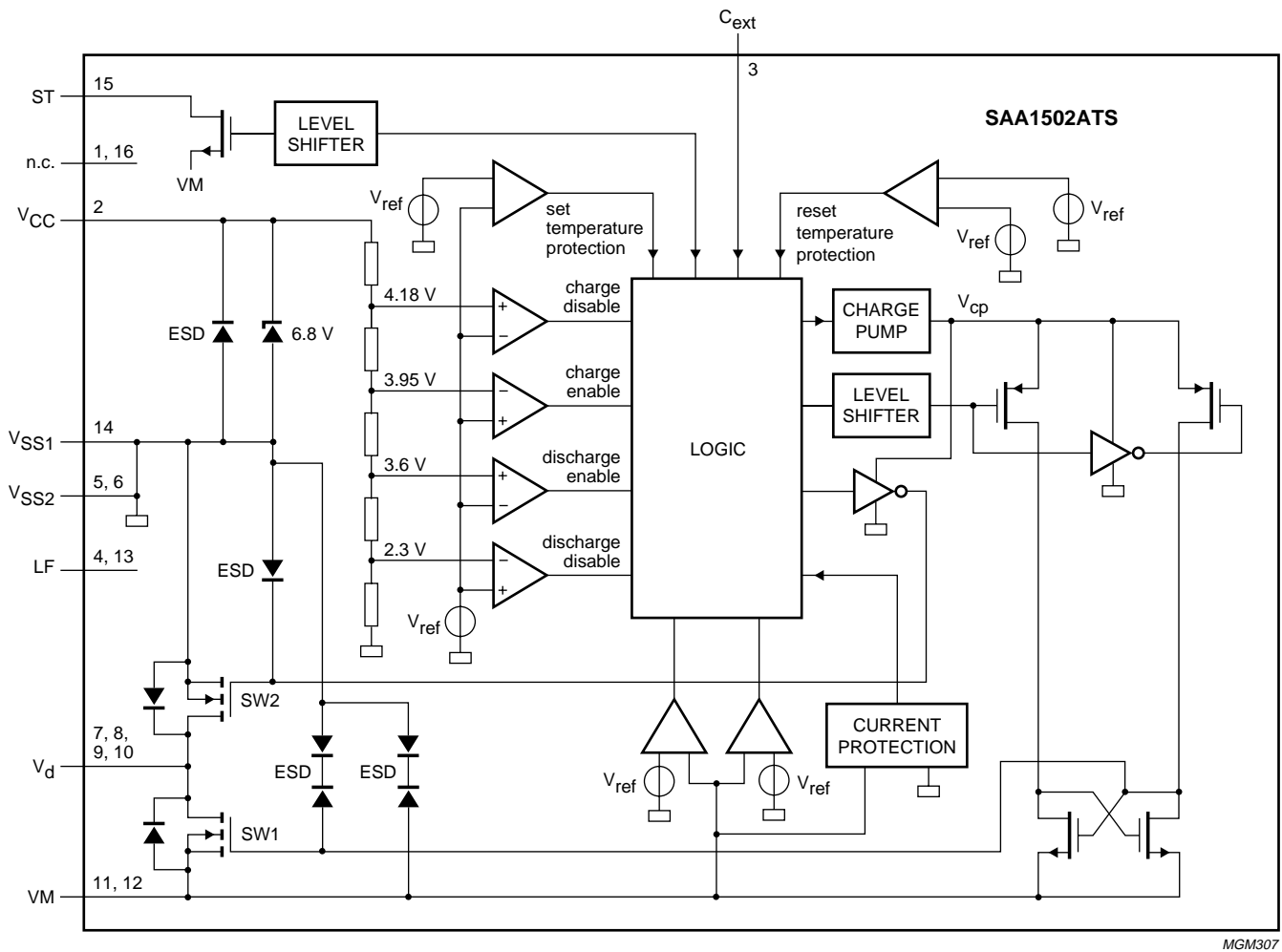


Fig.1 Block diagram.

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PINNING

| SYMBOL           | PIN         | DESCRIPTION                             |
|------------------|-------------|---|
| n.c.             | 1, 16       | not connected                           |
| V <sub>CC</sub>  | 2           | positive battery sense input            |
| C <sub>ext</sub> | 3           | external delay capacitor                |
| LF               | 4, 13       | leadframe connection control circuit    |
| V <sub>SS2</sub> | 5, 6        | negative battery input and power ground |
| V <sub>d</sub>   | 7, 8, 9, 10 | drain voltage of SW1 and SW2            |
| VM               | 11, 12      | negative sense input                    |
| V <sub>SS1</sub> | 14          | ground for the control circuit          |
| ST               | 15          | status output                           |

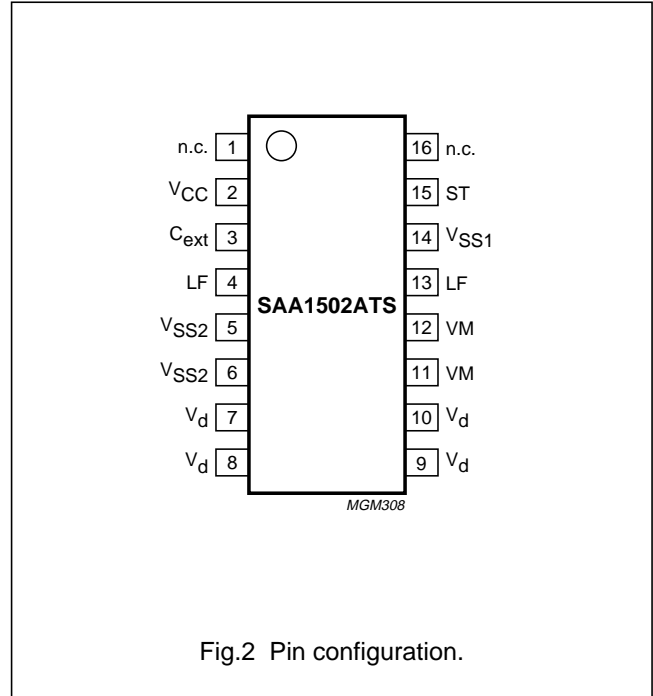


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 3 gives the connection diagram of a Li-ion battery pack. All that is contained within the solid perimeter is the safety IC SAA1502ATS. It is a Multichip Module (MCM), containing two separate but interconnected chips, one is the control IC and the other contains two vertical power NMOS transistors which are connected in anti series. Both transistors have their backgate connected to their source, resulting in two backgate diodes in anti series. The basic function of the SAA1502ATS is to protect a single Li-ion cell against overcharge and overdischarge for reasons of lifetime and safety. The voltage across the cell terminals is monitored continuously and compared to an accurate internal reference voltage. For battery voltages between 3.6 and 4.18 V and a (dis)charge current below the current protection level, the safety unit is in normal operating mode (see Fig.4). In this state both switches are driven with an elevated supply voltage (with a charge pump) which guarantees a low resistance in the main current path. This is important for fully utilizing the high energy density of Li-ion battery technology.

The discharge PowerMOS transistor SW2 is disabled to block further discharge, when the battery is discharged below 2.3 V. The battery voltage will increase stepwise, because of the sudden disconnection of the load. The unit will not re-enter the normal operation mode at this event

unless the battery voltage exceeds the voltage restarting level of 3.6 V.

When no charger is present in the discharge inhibit mode, the system will switch to the Power-down mode.

The current consumption of the unit (SAA1502ATS and the Li-ion cell) is then reduced to a typical value of 0.1 µA for minimizing the discharge of the battery pack.

Connecting a charger in the Power-down mode is detected by a voltage difference between V<sub>CC</sub> and VM of more than 3 V. The system will then return to the discharge inhibit mode. After a short transition phase characterized by conduction of the backgate diode between the drain and source leads of SW2, the system goes to the normal operating mode and SW2 is powered again.

At zero voltage start-up, the system will start at the reset mode. A special circuit keeps the charge transistor SW1 on as much as possible.

When the battery is charged to a voltage level of 4.18 V it will enter the charge inhibit mode and the charge PowerMOS transistor SW1 is switched off, disabling charging. Connecting a load is then detected by the reversal of the voltage across SW1 (I<sub>dch</sub> > 1.5 mA) and will immediately reactivate SW1, entering the discharge enable state.

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A short time is needed to charge the gate of SW1. During this time the backgate diode between drain and source of SW1 conducts.

The system will remain in the discharge enable mode unless:

- The battery voltage drops below 3.95 V, which results in re-entering normal operation. This transition is not externally noticeable, because both switches remain low ohmic.
- A charger is connected which will immediately deactivate SW1 if  $I_{ch} > 280$  mA. As an additional safety precaution also  $V_{CC} > 4.18$  V yields the same reaction, because a small current of a charger may be undetected with the condition of  $I_{ch} > 280$  mA, leading to overcharging the Li-ion cell.

Current protection will deactivate both switches and is detected by a voltage drop or rise of  $V_{VM}$  when both switches are activated. A release of this state can only be achieved by removing the load (or charger).

The temperature protection overrules all other states and yields deactivation of both switches. This situation is activated at a junction temperature of 130 °C and released at a junction temperature of 60 °C. The temperature protection is followed by a return to its preceding mode.

### Normal mode

In case of correct temperature, battery voltage and (dis)charge current, the system will be in the normal operation mode. Both the charge and discharge output will be active high, so both switches are conducting (SW1 = SW2 = 1).

### Discharge inhibit mode

If the battery drops below 2.3 V, the system will switch to the discharge inhibit mode. In this mode only charging of the battery is allowed (SW1 = 1, SW2 = 0). The system will return to the normal operation mode as soon as the battery voltage will exceed 3.6 V, or by detection of a charge current.

The overdischarge detection of 2.3 V has a delay of 40 ms typical. The voltage detection level 3.6 V has a delay of 50 ms typical. Because a charge current is necessary to increase the battery voltage, the system will normally switch to the normal operation mode at  $V_{CC} = 2.3$  V by detecting a charge current. But if the charge current is too small to detect, the 3.6 V detection is a backup.

To prevent an instable situation between the normal operation and the discharge inhibit mode when the battery

is charged at a voltage below 2.3 V, an extra condition of  $V_{bat} > 2.3$  V is included going from the discharge inhibit to the normal operation mode.

### Power-down mode

At low battery voltage the supply current is reduced to 100 nA for minimizing the discharge of the battery by the SAA1502ATS.

At the Power-down mode all analog circuitry, except circuitry for detecting a charger present ( $V_{CC} - V_{VM} > 3$  V), is disabled. The Power-down mode is entered when the system is in the discharge inhibit mode and no charger is present. The discharge inhibit mode will be entered again as soon as a charger is connected.

The detection of a charger is accomplished by detecting a voltage difference of 3 V between  $V_{CC}$  and VM. In this mode the voltage difference (see Fig.5) is:

$$V_{CC} - V_{VM} = V_{bat} - V_{R1} + V_{J(DO)} + V_{ds(CO)} \approx V_{bat} + 0.6 \text{ V.}$$

So in the application the battery has to be charged in the Power-down mode until such a voltage that  $V_{CC} - V_{VM} = 3$  V.

### Reset mode

If the battery voltage is below 1.9 V, the system will be in the reset mode. Because in this mode the charge pump is disabled and battery charging should be possible, the charge FET is switched on with a reduced  $V_{gs}$  voltage.

As soon as the battery voltage exceeds 2.25 V the system will switch to the discharge inhibit mode and the charge pump will be activated again.

### Zero voltage start-up

The system has to be able to charge the battery at '0 Volt'. This means that when connecting a charger in case of a complete empty battery, the charge FET has to be active. In the reset mode the charge FET (SW1) is connected via a diode to  $V_{CC}$ , so that the charge FET will be active when the  $V_{VM}$  voltage is negative. The discharge inhibit mode will be entered as soon as a battery voltage exceeds 2.25 V.

### Charge inhibit mode

If the battery voltage exceeds 4.18 V, the charge inhibit mode will be entered. At this mode the battery can only be discharged (SW1 = 0, SW2 = 1). The overcharge detection has a delay of 40 ms. This delay can be increased by an external capacitor. The delay time is then

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defined as:

$$t_d = 40 + (37 \times C_{ext}) \text{ [ms]}, \text{ with } C_{ext} \text{ in nF.}$$

The system will return to the normal operation mode from the charge inhibit mode when the battery voltage drops below 3.95 V.

From the discharge enable mode the charge inhibit mode will also be entered as soon as a charge current is detected.

### Discharge enable mode

When the system is in the charge inhibit mode, charging of the battery is disabled because switch SW1 is turned off. Discharge of the battery will then occur via the backgate diode of SW1. So the output voltage will be approximately 0.6 V lower and also dissipation of the backgate diode of SW1 occurs. It would be preferable to turn both switches on at that time without allowing charging of the battery until the battery voltage has dropped to 3.95 V.

If a discharge current larger than 1.5 mA is detected in the charge inhibit mode, the system will activate the discharge enable mode, activating both switches. From the discharge enable mode the charge inhibit mode will be re-entered as soon as a charge current is detected larger than 280 mA or the battery voltage exceeds 4.18 V.

The detection of a higher voltage than 4.18 V is a backup. If the battery is charged with a lower charge current than 280 mA, the system will not switch from the discharge enable mode to the charge inhibit mode. Eventually, if the battery is overcharged because of a small charge current, the battery voltage will exceed 4.18 V and the system will switch to the charge inhibit mode.

The system will return to the normal operation mode from the discharge enable mode when the battery voltage drops below 3.95 V.

If the system is in the charge inhibit mode, it will mostly go to the normal mode via the discharge enable mode. But if the system is in the charge inhibit state and the system is stored for several years, the battery voltage can drop because of the battery discharge by the SAA1502ATS and the self-discharge of the battery. So a voltage drop of the battery is possible, without detecting a discharge current. Because of this, the normal operation mode should also be entered from the charge inhibit state when the battery voltage is below 3.95 V and not only from the discharge enable mode. In this way, charging a battery is always possible if the battery voltage is below 3.95 V.

### Temperature protection

Internally the system will switch between the different modes as given in the state diagram, independent of the temperature. As the junction temperature exceeds 130 °C, the output signals will be overruled and switched to zero (SW1 = SW2 = 0).

The supply current will be reduced to approximately 100 nA when the Power-down or reset mode is activated. In these modes the temperature protection is deactivated.

When the junction temperature drops below 60 °C, the output signals will not be overruled any more.

### Overcurrent protection

When the (dis)charge current exceeds the specified maximum value, the current protection mode is entered.

An extra condition of SW1 = SW2 = 1 is necessary because of the next situation:

If the system is in the discharge inhibit and a charge current is detected (e.g.  $V_{VM} = -0.6 \text{ V}$ ) the normal operation mode will be entered. Because of a minimum time in which the gate capacitors have to be charged, the  $V_{VM}$  voltage will be  $-0.6 \text{ V}$  for a short period, when the system is already in the normal operation mode. A  $V_{VM}$  voltage of  $-0.6 \text{ V}$  could also occur when the system is charged with current exceeding the maximum charge current. To prevent that a maximum charge current is detected when coming from the discharge inhibit state, the system waits until both SW1 and SW2 are fully charged before a maximum (dis)charge current is detected.

So the voltages at SW1 and SW2 are measured to be sure that the normal operation mode is stabilized before the current protection mode can be entered.

The same applies when entering the discharge enable state from the charge inhibit state by detecting a discharge current.

The delay of the current protection as function of the (dis)charge current is given in Fig.8.

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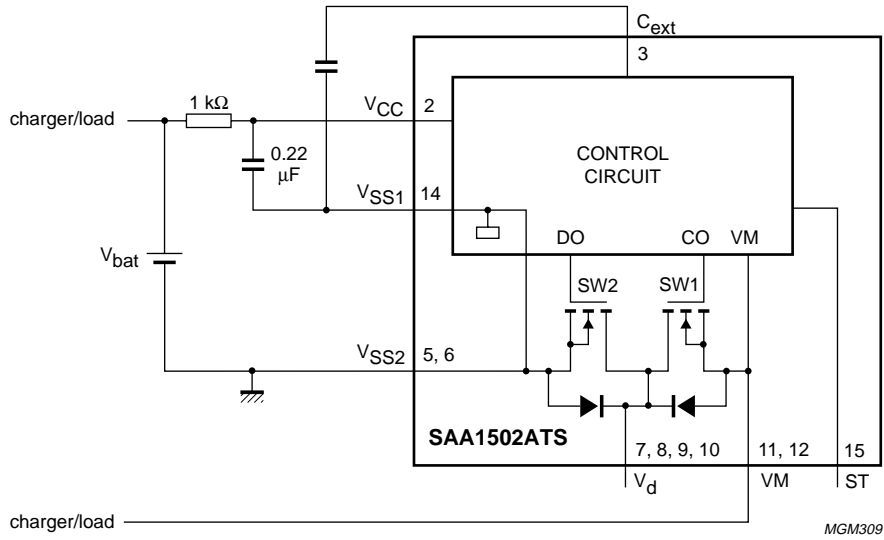


Fig.3 Connection diagram.

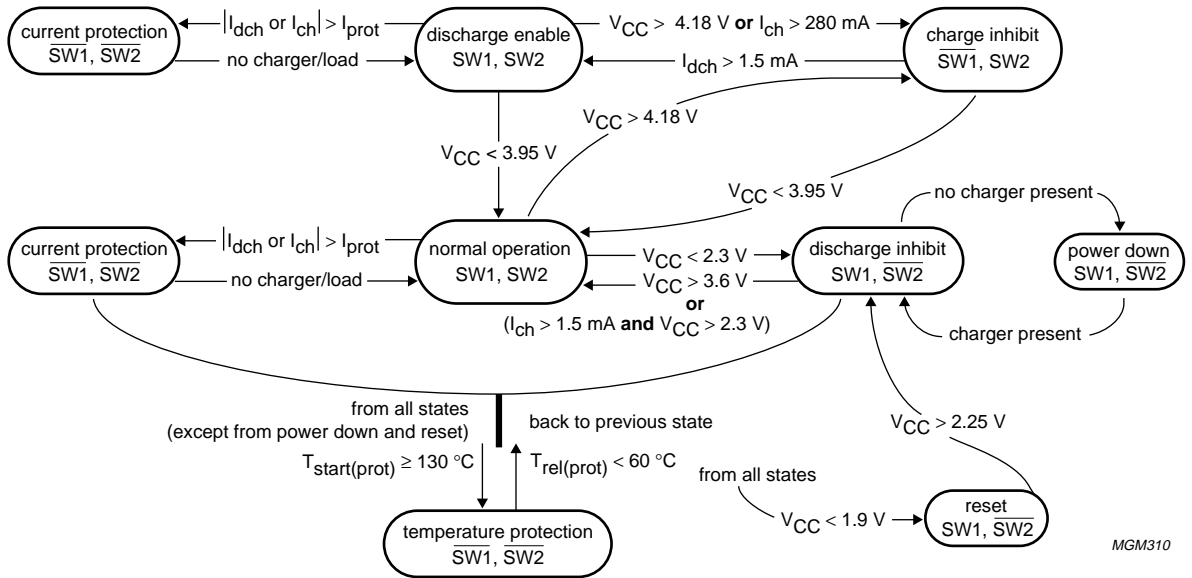


Fig.4 Flow diagram.

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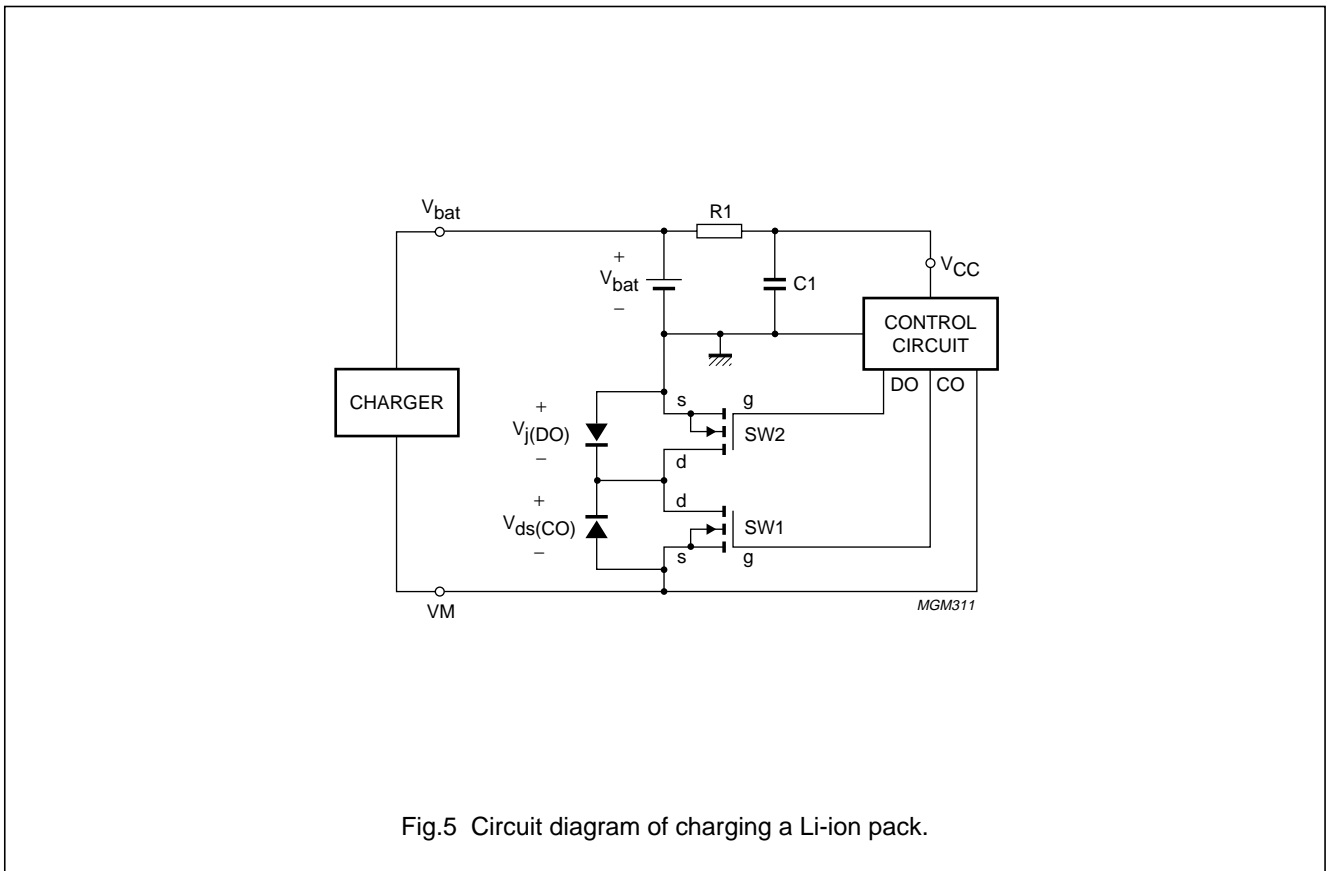


Fig.5 Circuit diagram of charging a Li-ion pack.





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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134); voltages with respect to pin  $V_{SS2}$ .

| SYMBOL                 | PARAMETER                                  | CONDITIONS                                      | MIN.            | MAX.     | UNIT |
|------------------------|--|---|-----------------|----------|------|
| $V_{CC}$               | positive battery sense input voltage       | DC constant                                     | -0.3            | +4.5     | V    |
| $V_{CC(\text{clamp})}$ | $V_{CC}$ clamping voltage                  | $t < 60 \text{ ms}$ and $I_{CC} = 7 \text{ mA}$ | -               | 8.5      | V    |
| $I_{CC}$               | maximum current through the $V_{CC}$ clamp |   | -               | 7        | mA   |
| $V_{VM}$               | negative sense input voltage               |   | $V_{CC} - 17.5$ | $V_{CC}$ | V    |
| $V_{ST}$               | status output voltage                      |   | $V_{VM}$        | $V_{CC}$ | V    |
| $I_{R\text{path}}$     | current through SW1 and SW2                |   | -               | 27       | A    |
| $T_{\text{amb}}$       | operating ambient temperature              |   | -25             | +80      | °C   |
| $T_{\text{stg}}$       | storage temperature                        |   | -55             | +150     | °C   |
| $ I_{V_{SS-VM}} $      | maximum body diode current (DC value)      |   | -               | 800      | mA   |

**THERMAL CHARACTERISTICS**

| SYMBOL                        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|-------------------------------|---|-------------|-------|------|
| $R_{\text{th}(j-a)}$          | thermal resistance from junction to ambient | in free air | 165   | K/W  |
| $R_{\text{th}(j-\text{pin})}$ | thermal resistance from junction to pin     |             | 22    | K/W  |

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## CHARACTERISTICS

$T_j = 25\text{ °C}$ ; all voltages with respect to  $V_{SS2}$ ; positive currents flow into the IC.

| SYMBOL                   | PARAMETER                                 | CONDITIONS  | MIN.  | TYP. | MAX. | UNIT          |
|--------------------------|---|---|-------|------|------|---------------|
| <b>Supply behaviour</b>  |   |   |       |      |      |               |
| $V_{CC}$                 | positive battery sense input voltage      |   | 0     | –    | 4.5  | V             |
| $I_{CC}$                 | supply current                            | $V_{CC} = 4.0\text{ V}; -13.5\text{ V} \leq V_{VM} \leq 0$                  | 4.0   | 7.0  | 10   | $\mu\text{A}$ |
| $I_q$                    | quiescent current                         | Power-down/reset mode<br>( $V_{CC} = 2.0\text{ V}$ )                        | 0.03  | 0.1  | 0.3  | $\mu\text{A}$ |
| $V_{CC}-V_{VM}$          | minimum charge voltage                    | at zero charge  | 1.8   | 2.4  | 3.0  | V             |
| <b>Voltage detection</b> |   |   |       |      |      |               |
| $V_{ec(det)}$            | excess charge detection voltage           | measured at terminals of the battery and $T_j = 25\text{ °C}$               | 4.15  | 4.18 | 4.20 | V             |
|                          |   | measured at terminals of the battery and $T_j = -5\text{ to }+55\text{ °C}$ | 4.145 | 4.18 | 4.21 | V             |
| $t_{ec(det)}$            | excess charge delay time $V_{ec(det)}$    | $C_{ext}$ not connected   | 20    | 40   | 60   | ms            |
|                          |   | $C_{ext} = 33\text{ nF} (\pm 10\%)$   | 0.5   | 1.25 | 2    | s             |
| $V_{ec(rel)}$            | excess charge release voltage             |   | 3.82  | 3.95 | 4.08 | V             |
| $t_{ec(rel)}$            | excess charge delay time $V_{ec(rel)}$    |   | 25    | 50   | 75   | ms            |
| $V_{ed(det)}$            | excess discharge detection voltage        |   | 2.2   | 2.3  | 2.4  | V             |
| $t_{ed(det)}$            | excess discharge delay time $V_{ed(det)}$ |   | 20    | 40   | 60   | ms            |
| $V_{ed(rel)}$            | excess discharge release voltage          |   | 3.3   | 3.6  | 3.9  | V             |
| $t_{ed(rel)}$            | excess discharge delay time $V_{ed(rel)}$ |   | 25    | 50   | 75   | ms            |
| $ I_{VSS-VM} $           | (dis)charge current detection             | charge inhibit state  | 0.05  | 1.5  | 37.5 | mA            |
|                          |   | discharge enable state  | 150   | 280  | 475  | mA            |
|                          |   | discharge inhibit state   | 0.05  | 1.5  | 37.5 | mA            |
| $V_{VM}$                 | negative sense input voltage              | discharge inhibit state;<br>no charge current                               | -7    | -12  | -20  | mV            |
|                          |   | current protection mode<br>no load detection                                | 70    | 90   | 120  | mV            |
|                          |   | no charger detection  | -7    | -12  | -20  | mV            |
| $V_{CC}-V_{VM}$          | charge present detection voltage          | Power-down mode   | 2.4   | 3.0  | 3.6  | V             |
| $V_{CC}$                 | positive battery sense input voltage      | start of reset mode   | 1.7   | 1.9  | 2.1  | V             |
|                          |   | excess of reset mode  | 2.05  | 2.25 | 2.45 | V             |
| $t_{d(on)}$              | switch-on delay time SW1/SW2              | $V_{CC} = 4.0\text{ V}$   | –     | 100  | –    | $\mu\text{s}$ |
| $t_{d(off)}$             | switch-off delay time SW1/SW2             | $V_{CC} = 4.0\text{ V}$   | –     | 100  | –    | $\mu\text{s}$ |

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| SYMBOL  | PARAMETER                             | CONDITIONS   | MIN. | TYP. | MAX. | UNIT |
|---|---------------------------------------|--|------|------|------|------|
| <b>Power transistors</b>                                    |                                       |  |      |      |      |      |
| R <sub>path</sub>   | main current path resistance          | V <sub>CC</sub> = 2.5 V; I <sub>VSS-VM</sub> = 2 A   | 52   | 66   | 80   | mΩ   |
|   |                                       | V <sub>CC</sub> = 4.0 V; I <sub>VSS-VM</sub> = 2 A   | 48   | 60   | 72   | mΩ   |
| <b>SW1 transistor</b>                                       |                                       |  |      |      |      |      |
| R <sub>path(SW1)</sub>                                      | current path resistance               | V <sub>CC</sub> = 2.5 V; I <sub>VSS-VM</sub> = 2 A   | 26   | 33   | 40   | mΩ   |
|   |                                       | V <sub>CC</sub> = 4.0 V; I <sub>VSS-VM</sub> = 2 A   | 24   | 30   | 36   | mΩ   |
| <b>SW2 transistor</b>                                       |                                       |  |      |      |      |      |
| R <sub>path(SW2)</sub>                                      | current path resistance               | V <sub>CC</sub> = 2.5 V; I <sub>VSS-VM</sub> = 2 A   | 26   | 33   | 40   | mΩ   |
|   |                                       | V <sub>CC</sub> = 4.0 V; I <sub>VSS-VM</sub> = 2 A   | 24   | 30   | 36   | mΩ   |
| <b>Temperature protection</b>                               |                                       |  |      |      |      |      |
| T <sub>start(prot)</sub>                                    | start of the temperature protection   |  | 120  | 130  | 140  | °C   |
| T <sub>rel(prot)</sub>                                      | release of the temperature protection |  | 50   | 60   | 70   | °C   |
| <b>Current detection at V<sub>CC</sub> = 4 V; see Fig.8</b> |                                       |  |      |      |      |      |
| I <sub>prot(min)</sub>                                      | minimum current protection level      | DC level   | 3.5  | 5    | 7    | A    |
| t <sub>d</sub>  | delay time at I <sub>prot</sub> = 8 A |  | 2    | 20   | 200  | ms   |
| t <sub>d(min)</sub>   | minimum delay time                    |  | 190  | –    | 430  | μs   |
| <b>Status; see Table 1 and Fig.7</b>                        |                                       |  |      |      |      |      |
| I <sub>ST</sub>   | output current                        | ST = 1; V <sub>CC</sub> – V <sub>VM</sub> = 17.5 V;<br>V <sub>ST</sub> – V <sub>VM</sub> = 0.5 V | 40   | –    | 200  | μA   |
|   |                                       | ST = 1; V <sub>CC</sub> – V <sub>VM</sub> = 4 V;<br>V <sub>ST</sub> – V <sub>VM</sub> = 0.5 V    | 10   | –    | 100  | μA   |
| V <sub>ST</sub>   | output voltage                        | ST = 1; I <sub>ST</sub> = 40 μA;<br>V <sub>CC</sub> – V <sub>VM</sub> = 17.5 V                   | –    | –    | 0.5  | V    |
|   |                                       | ST = 1; I <sub>ST</sub> = 10 μA;<br>V <sub>CC</sub> – V <sub>VM</sub> = 4 V                      | –    | –    | 0.5  | V    |

**Table 1** Functional table of the status output (ST);  
note 1

| CONDITIONS             | OUTPUT |
|------------------------|--------|
| Normal operation       | 0      |
| Charge inhibit         | 1      |
| Discharge enable       | 0      |
| Discharge inhibit      | 0      |
| Power-down             | 0      |
| Current protection     | 1      |
| Temperature protection | 1      |

**Note**

1. At which: '0' is active off, and '1' is active on.

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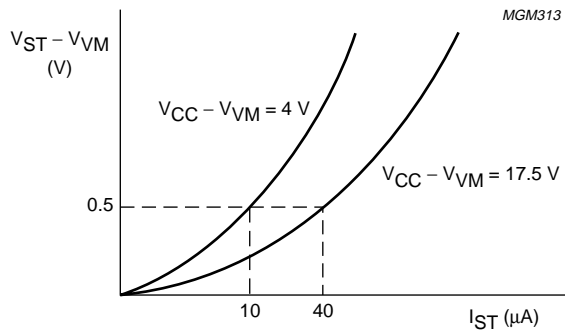


Fig.7 Status output current at different charge voltages.

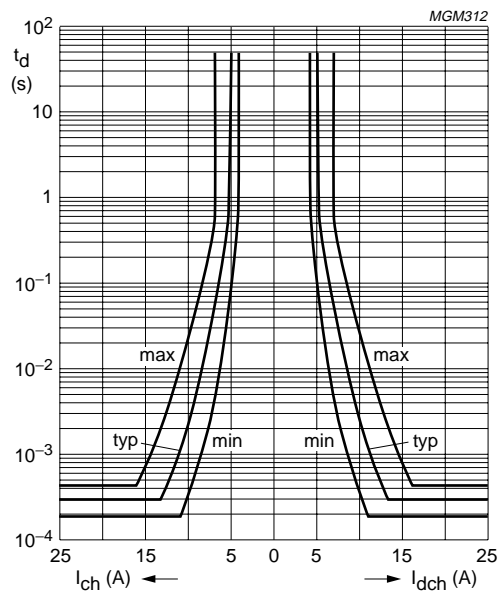
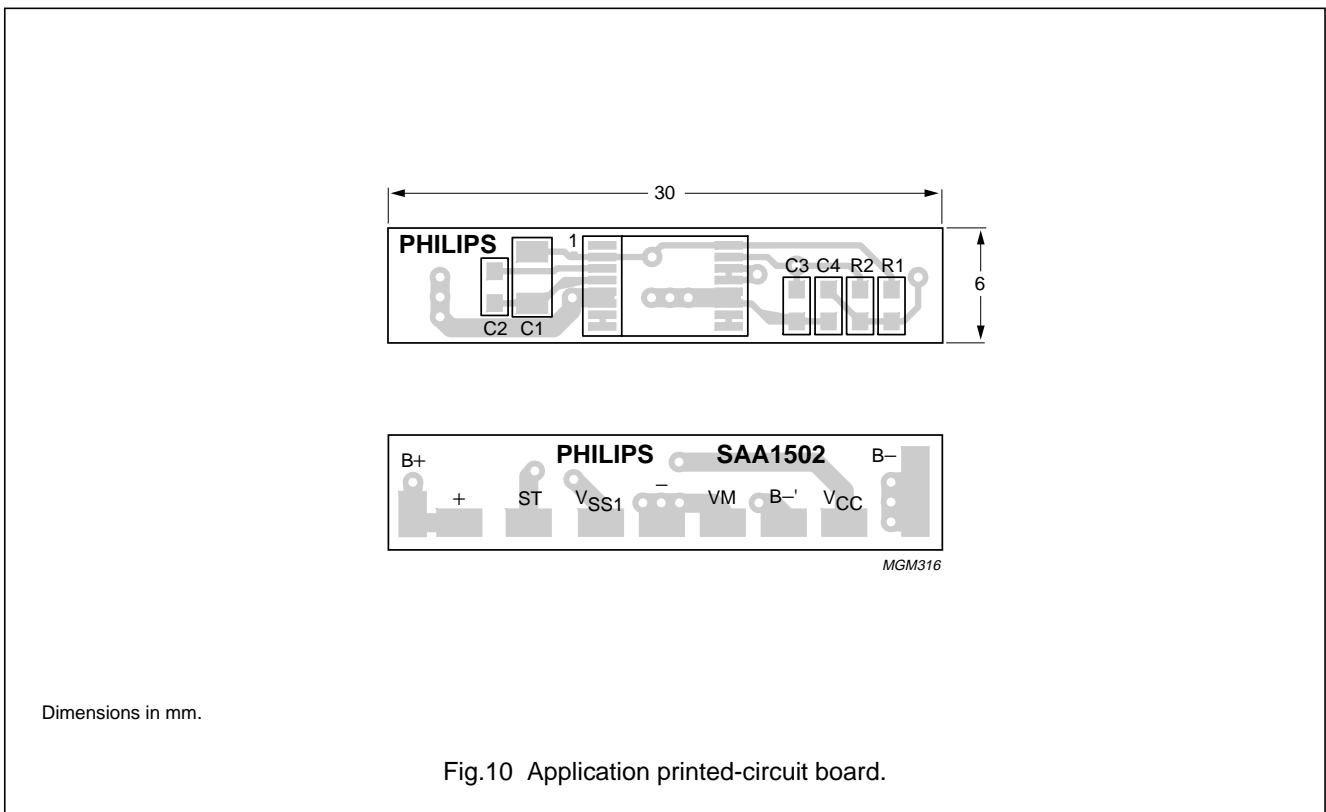
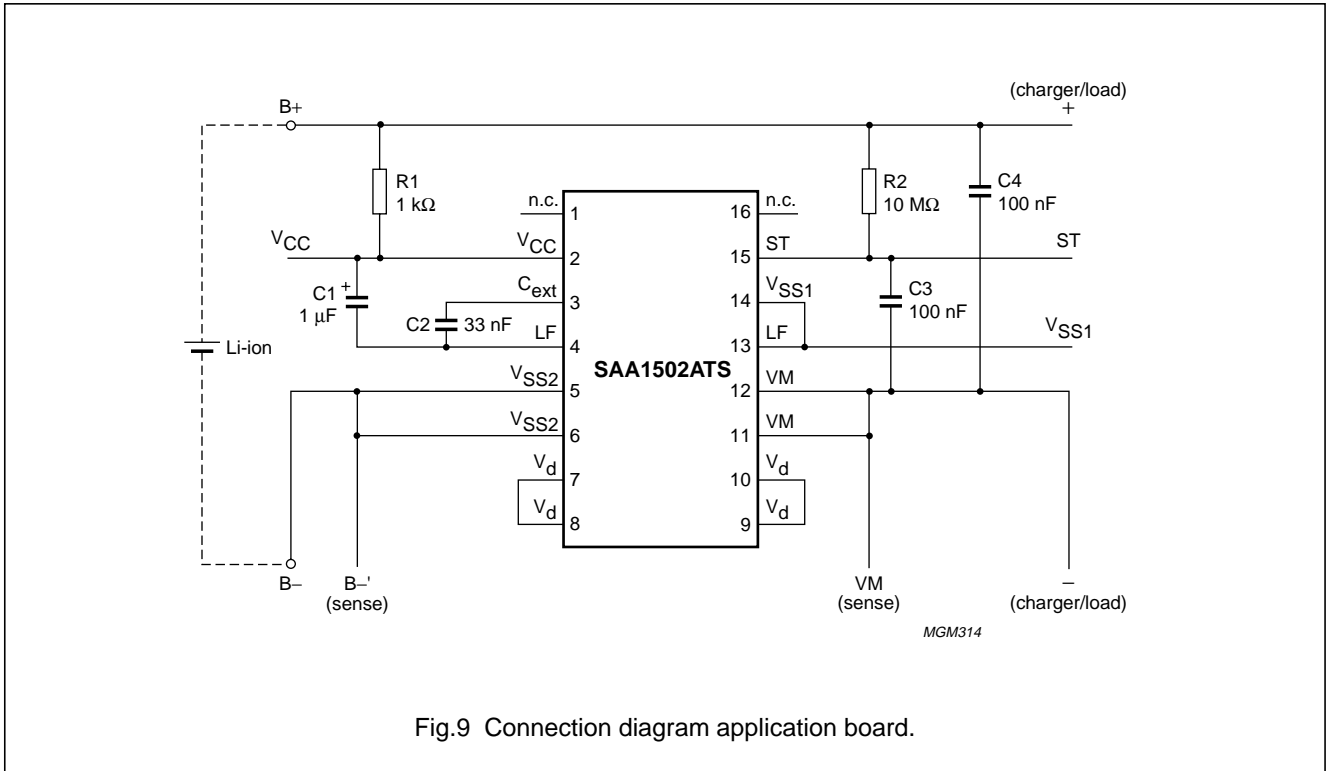


Fig.8 Current protection delay.

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APPLICATION INFORMATION



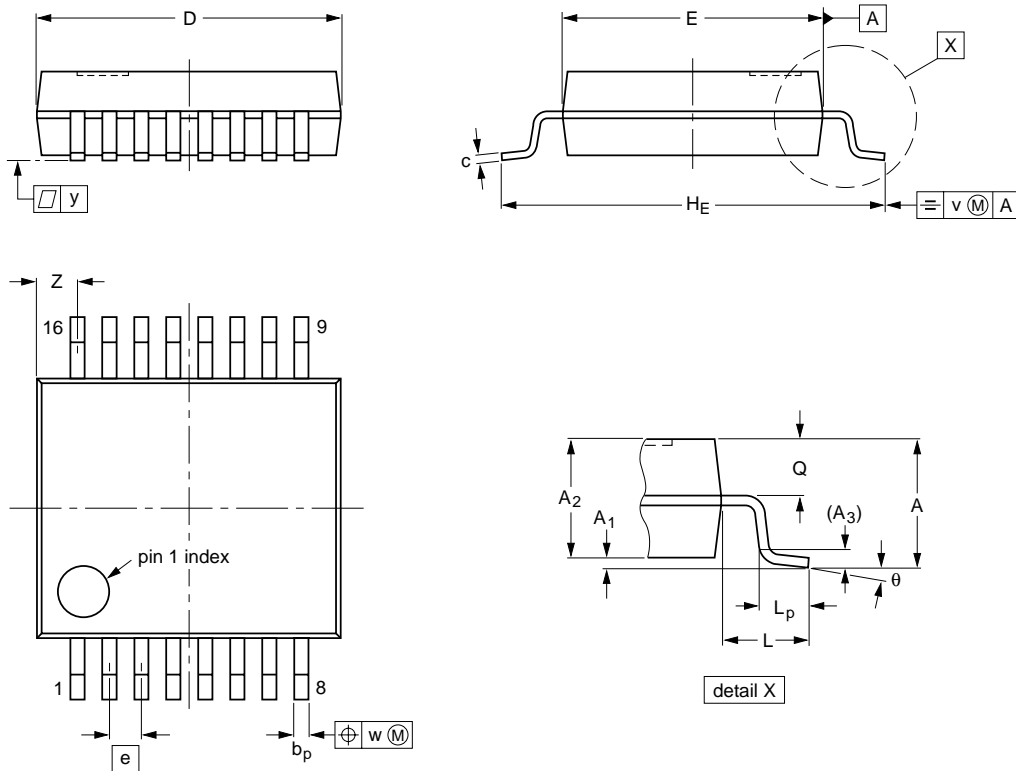
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PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L    | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | $\theta$ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 2.0    | 0.21<br>0.05   | 1.80<br>1.65   | 0.25           | 0.38<br>0.25   | 0.20<br>0.09 | 6.4<br>6.0       | 5.4<br>5.2       | 0.65 | 7.9<br>7.6     | 1.25 | 1.03<br>0.63   | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55     | 8°<br>0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT338-1        |            | MO-150AC |      |  |                     | 94-01-14<br>95-02-04 |

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



## Safety IC for Li-ion

## SAA1502ATS

**DEFINITIONS**

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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**NOTES**

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**NOTES**

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