DATA SHEET

SAA4992H
Field and line rate converter with noise reduction

Product specification
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File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Upconversion of all $1f_H$ film and video standards up to 292 active input lines per field
- 100/120 Hz 2 : 1, 50/60 Hz 1 : 1 and 100/120 Hz 1 : 1 output formats
- 4 : 1 : 1, 4 : 2 : 2 and 4 : 2 : 2 Differential Pulse Code Modulation (DPCM) input colour formats; 4 : 1 : 1 and 4 : 2 : 2 output colour formats
- Full 8-bit accuracy
- Scalable performance by applying 1, 2 or 3 external field memories
- Improved recursive de-interlacing
- Film (25 Hz, 30 Hz) upconversion to 100/120 movement phases per second
- Variable vertical sharpness enhancement
- Motion compensated 3D dynamic noise reduction
- High quality vertical zoom
- 2 Mbaud serial interface (SNERT).

2 GENERAL DESCRIPTION

The SAA4992H is a completely digital monolithic integrated circuit which can be used for field and line rate conversion of all global TV standards.

It features improved ‘Natural Motion’ performance and full film upconversion for all 50 and 60 Hz film material.

It can be configured to emulate the SAA4990H as well as the SAA4991WP. For demonstration purposes a split screen mode to show the Dynamic Noise Reduction (DNR) function and a colour vector overlay is available.

The SAA4992H supports a Boundary Scan Test (BST) circuit in accordance with IEEE 1149.

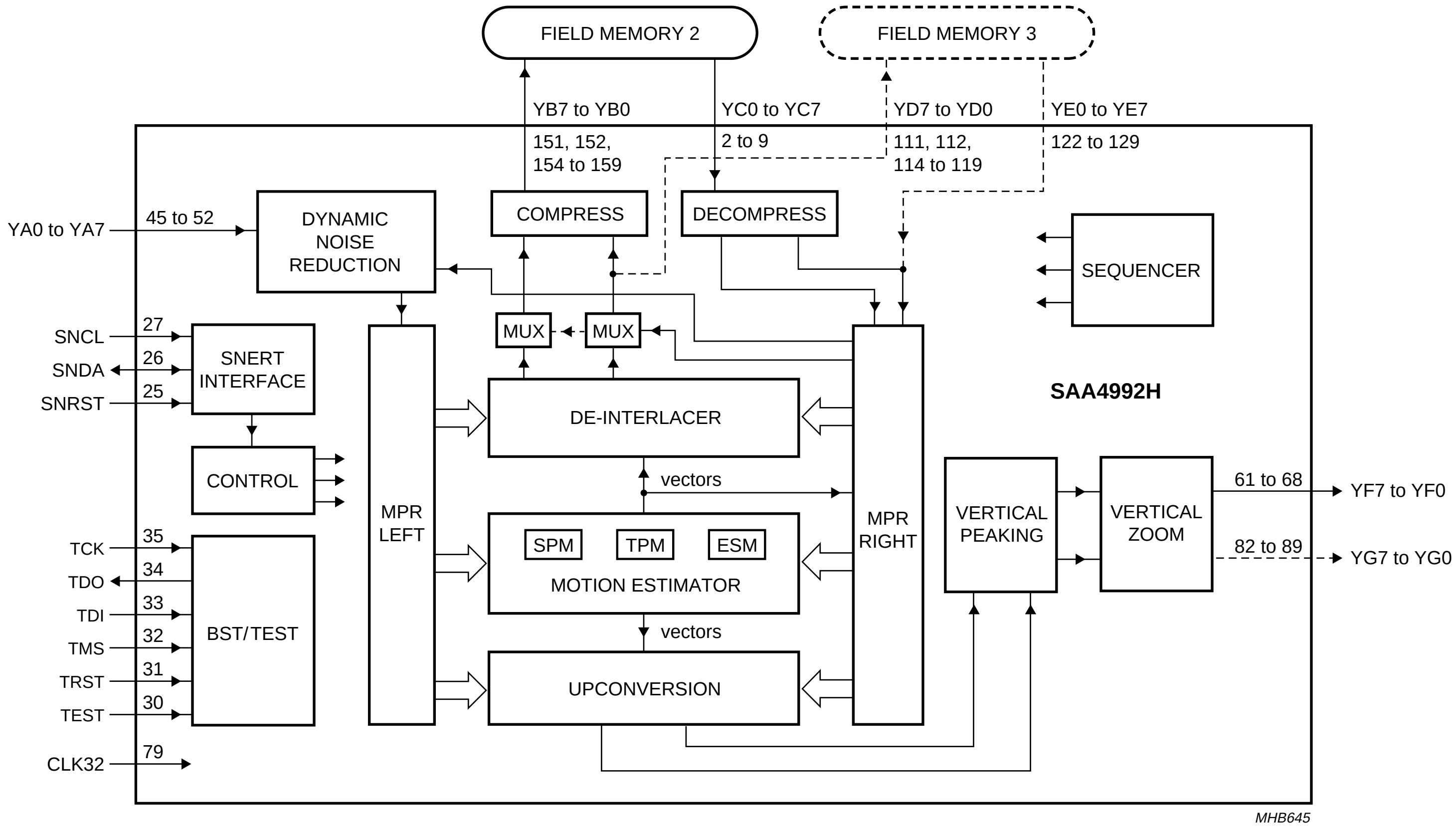
3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.0	3.3	3.6	V
I_{DD}	supply current	–	400	550	mA
f_{CLK}	operating clock frequency	–	32	33.3	MHz
T_{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

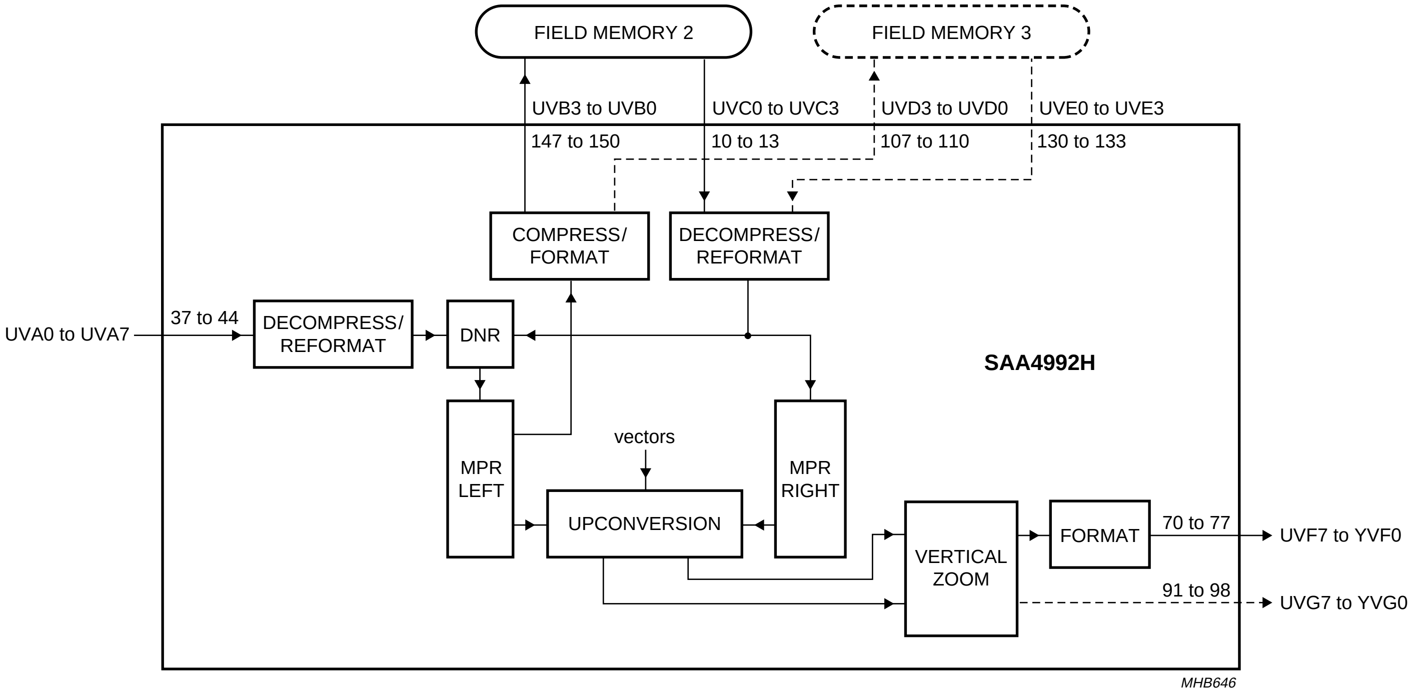
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4992H	QFP160	plastic quad flat package; 160 leads (lead length 1.6 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT322-2

5 BLOCK DIAGRAMS



The solid lines represent pixel data; the broken lines represent controls.

Fig.1 Block diagram of the luminance part.



The solid lines represent pixel data; the broken lines represent controls.

Fig.2 Block diagram of the chrominance part.

6 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION[1][2]
V_{SSE}	1	ground	ground of output pads
YC0	2	input	bus C luminance input from field memory 2 bit 0 (LSB)
YC1	3	input	bus C luminance input from field memory 2 bit 1
YC2	4	input	bus C luminance input from field memory 2 bit 2
YC3	5	input	bus C luminance input from field memory 2 bit 3
YC4	6	input	bus C luminance input from field memory 2 bit 4
YC5	7	input	bus C luminance input from field memory 2 bit 5
YC6	8	input	bus C luminance input from field memory 2 bit 6
YC7	9	input	bus C luminance input from field memory 2 bit 7 (MSB)
UVC0	10	input	bus C chrominance input from field memory 2 bit 0 (LSB)
UVC1	11	input	bus C chrominance input from field memory 2 bit 1
UVC2	12	input	bus C chrominance input from field memory 2 bit 2
UVC3	13	input	bus C chrominance input from field memory 2 bit 3 (MSB)
REC	14	output	read enable output for bus C
V_{SSE}	15	ground	ground of output pads
V_{DDE}	16	supply	supply voltage of output pads
V_{SSI}	17	ground	core ground
V_{DDI}	18	supply	core supply voltage
JUMP0	19	input	configuration pin 0; will be stored in register 0B3 e.g. to indicate presence of 3rd field memory; should be connected to ground or to V_{DDI} via pull-up resistor; note 3
JUMP1	20	input	configuration pin 1; will be stored in register 0B5 e.g. to indicate presence of 16-bit 1st field memory for full 4 : 2 : 2; should be connected to ground or to V_{DDI} via pull-up resistor; note 3
V_{DDE}	21	supply	supply voltage of output pads
V_{DDI}	22	supply	core supply voltage
V_{SSI}	23	ground	core ground
RAMTST1	24	input	test pin 1 for internal RAM testing; connect to ground for normal operation
SNRST	25	input	SNERT bus reset
SNDA	26	I/O	SNERT bus data
SNCL	27	input	SNERT bus clock
V_{SSE}	28	ground	ground of output pads
RAMTST2	29	input	test pin 2 for internal RAM testing; connect to ground for normal operation
TEST	30	input	test mode input; if not used it has to be connected to ground
TRST	31	input	boundary scan test: reset input signal; if not used it has to be connected to ground
TMS	32	input	boundary scan test: test mode select; if not used it has to be connected to V_{DDI} via pull-up resistor; note 3
TDI	33	input	boundary scan test: data input signal; if not used it has to be connected to V_{DDI} via pull-up resistor; note 3
TDO	34	output	boundary scan test: data output signal
TCK	35	input	boundary scan test: clock input signal; if not used it has to be connected to V_{DDI} via pull-up resistor; note 3

SYMBOL	PIN	TYPE	DESCRIPTION[1][2]
V_{SSE}	36	ground	ground of output pads
UVA0	37	input	bus A chrominance input from field memory 1 bit 0 (LSB)
UVA1	38	input	bus A chrominance input from field memory 1 bit 1
UVA2	39	input	bus A chrominance input from field memory 1 bit 2
UVA3	40	input	bus A chrominance input from field memory 1 bit 3
UVA4	41	input	bus A chrominance input from field memory 1 bit 4
UVA5	42	input	bus A chrominance input from field memory 1 bit 5
UVA6	43	input	bus A chrominance input from field memory 1 bit 6
UVA7	44	input	bus A chrominance input from field memory 1 bit 7 (MSB)
YA0	45	input	bus A luminance input from field memory 1 bit 0 (LSB)
YA1	46	input	bus A luminance input from field memory 1 bit 1
YA2	47	input	bus A luminance input from field memory 1 bit 2
YA3	48	input	bus A luminance input from field memory 1 bit 3
YA4	49	input	bus A luminance input from field memory 1 bit 4
YA5	50	input	bus A luminance input from field memory 1 bit 5
YA6	51	input	bus A luminance input from field memory 1 bit 6
YA7	52	input	bus A luminance input from field memory 1 bit 7 (MSB)
REA	53	output	read enable output for bus A
V_{SSE}	54	ground	ground of output pads
V_{SSI}	55	ground	core ground
V_{DDI}	56	supply	core supply voltage
V_{DDI}	57	supply	core supply voltage
V_{SSI}	58	ground	core ground
V_{SSE}	59	ground	ground of output pads
REF	60	input	read enable input for bus F and G
YF7	61	output	bus F luminance output bit 7 (MSB)
YF6	62	output	bus F luminance output bit 6
YF5	63	output	bus F luminance output bit 5
YF4	64	output	bus F luminance output bit 4
YF3	65	output	bus F luminance output bit 3
YF2	66	output	bus F luminance output bit 2
YF1	67	output	bus F luminance output bit 1
YF0	68	output	bus F luminance output bit 0 (LSB)
V_{DDE}	69	supply	supply voltage of output pads
UVF7	70	output	bus F chrominance output bit 7 (MSB)
UVF6	71	output	bus F chrominance output bit 6
UVF5	72	output	bus F chrominance output bit 5
UVF4	73	output	bus F chrominance output bit 4
UVF3	74	output	bus F chrominance output bit 3
UVF2	75	output	bus F chrominance output bit 2
UVF1	76	output	bus F chrominance output bit 1

SYMBOL	PIN	TYPE	DESCRIPTION(1)(2)
UVF0	77	output	bus F chrominance output bit 0 (LSB)
V_{SSE}	78	ground	ground of output pads
CLK32	79	input	system clock input
V_{SSI}	80	ground	core ground
V_{SSE}	81	ground	ground of output pads
YG7	82	output	bus G luminance output bit 7 (MSB)
YG6	83	output	bus G luminance output bit 6
YG5	84	output	bus G luminance output bit 5
YG4	85	output	bus G luminance output bit 4
YG3	86	output	bus G luminance output bit 3
YG2	87	output	bus G luminance output bit 2
YG1	88	output	bus G luminance output bit 1
YG0	89	output	bus G luminance output bit 0 (LSB)
V_{DDE}	90	supply	supply voltage of output pads
UVG7	91	output	bus G chrominance output bit 7 (MSB)
UVG6	92	output	bus G chrominance output bit 6
UVG5	93	output	bus G chrominance output bit 5
UVG4	94	output	bus G chrominance output bit 4
UVG3	95	output	bus G chrominance output bit 3
UVG2	96	output	bus G chrominance output bit 2
UVG1	97	output	bus G chrominance output bit 1
UVG0	98	output	bus G chrominance output bit 0 (LSB)
V_{SSE}	99	ground	ground of output pads
V_{SSI}	100	ground	core ground
V_{DDI}	101	supply	core supply voltage
V_{DDE}	102	supply	supply voltage of output pads
V_{DDI}	103	supply	core supply voltage
V_{SSI}	104	ground	core ground
V_{SSE}	105	ground	ground of output pads
WED	106	output	write enable output for bus D
UVD3	107	output	bus D chrominance output to field memory 3 bit 3 (MSB)
UVD2	108	output	bus D chrominance output to field memory 3 bit 2
UVD1	109	output	bus D chrominance output to field memory 3 bit 1
UVD0	110	output	bus D chrominance output to field memory 3 bit 0 (LSB)
YD7	111	output	bus D luminance output to field memory 3 bit 7 (MSB)
YD6	112	output	bus D luminance output to field memory 3 bit 6
V_{DDE}	113	supply	supply voltage of output pads
YD5	114	output	bus D luminance output to field memory 3 bit 5
YD4	115	output	bus D luminance output to field memory 3 bit 4
YD3	116	output	bus D luminance output to field memory 3 bit 3
YD2	117	output	bus D luminance output to field memory 3 bit 2

SYMBOL	PIN	TYPE	DESCRIPTION[1][2]
YD1	118	output	bus D luminance output to field memory 3 bit 1
YD0	119	output	bus D luminance output to field memory 3 bit 0 (LSB)
V_{SSE}	120	ground	ground of output pads
V_{SSE}	121	ground	ground of output pads
YE0	122	input	bus E luminance input from field memory 3 bit 0 (LSB)
YE1	123	input	bus E luminance input from field memory 3 bit 1
YE2	124	input	bus E luminance input from field memory 3 bit 2
YE3	125	input	bus E luminance input from field memory 3 bit 3
YE4	126	input	bus E luminance input from field memory 3 bit 4
YE5	127	input	bus E luminance input from field memory 3 bit 5
YE6	128	input	bus E luminance input from field memory 3 bit 6
YE7	129	input	bus E luminance input from field memory 3 bit 7 (MSB)
UVE0	130	input	bus E chrominance input from field memory 3 bit 0 (LSB)
UVE1	131	input	bus E chrominance input from field memory 3 bit 1
UVE2	132	input	bus E chrominance input from field memory 3 bit 2
UVE3	133	input	bus E chrominance input from field memory 3 bit 3 (MSB)
REE	134	output	read enable output for bus E
V_{SSE}	135	ground	ground of output pads
n.c.	136	–	not connected
V_{SSI}	137	ground	core ground
V_{DDI}	138	supply	core supply voltage
n.c.	139	–	not connected
n.c.	140	–	not connected
V_{DDE}	141	supply	supply voltage of output pads
V_{DDI}	142	supply	core supply voltage
V_{SSI}	143	ground	core ground
n.c.	144	–	not connected
V_{SSE}	145	ground	ground of output pads
WEB	146	output	write enable output for bus B
UVB3	147	output	bus B chrominance output to field memory 2 bit 3 (MSB)
UVB2	148	output	bus B chrominance output to field memory 2 bit 2
UVB1	149	output	bus B chrominance output to field memory 2 bit 1
UVB0	150	output	bus B chrominance output to field memory 2 bit 0 (LSB)
YB7	151	output	bus B luminance output to field memory 2 bit 7 (MSB)
YB6	152	output	bus B luminance output to field memory 2 bit 6
V_{DDE}	153	supply	supply voltage of output pads
YB5	154	output	bus B luminance output to field memory 2 bit 5
YB4	155	output	bus B luminance output to field memory 2 bit 4
YB3	156	output	bus B luminance output to field memory 2 bit 3
YB2	157	output	bus B luminance output to field memory 2 bit 2

SYMBOL	PIN	TYPE	DESCRIPTION[1][2]
YB1	158	output	bus B luminance output to field memory 2 bit 1
YB0	159	output	bus B luminance output to field memory 2 bit 0 (LSB)
V_{SSE}	160	ground	ground of output pads

Notes

1. Not used input pins (e.g. bus E) should be connected to ground.
2. Because of the noisy characteristic of the output pad supply it is recommended not to connect the core supply and the output pad supply directly at the device. The output pad supply should be buffered as close as possible to the device.
3. The external pull-up resistor should be 47 kΩ.

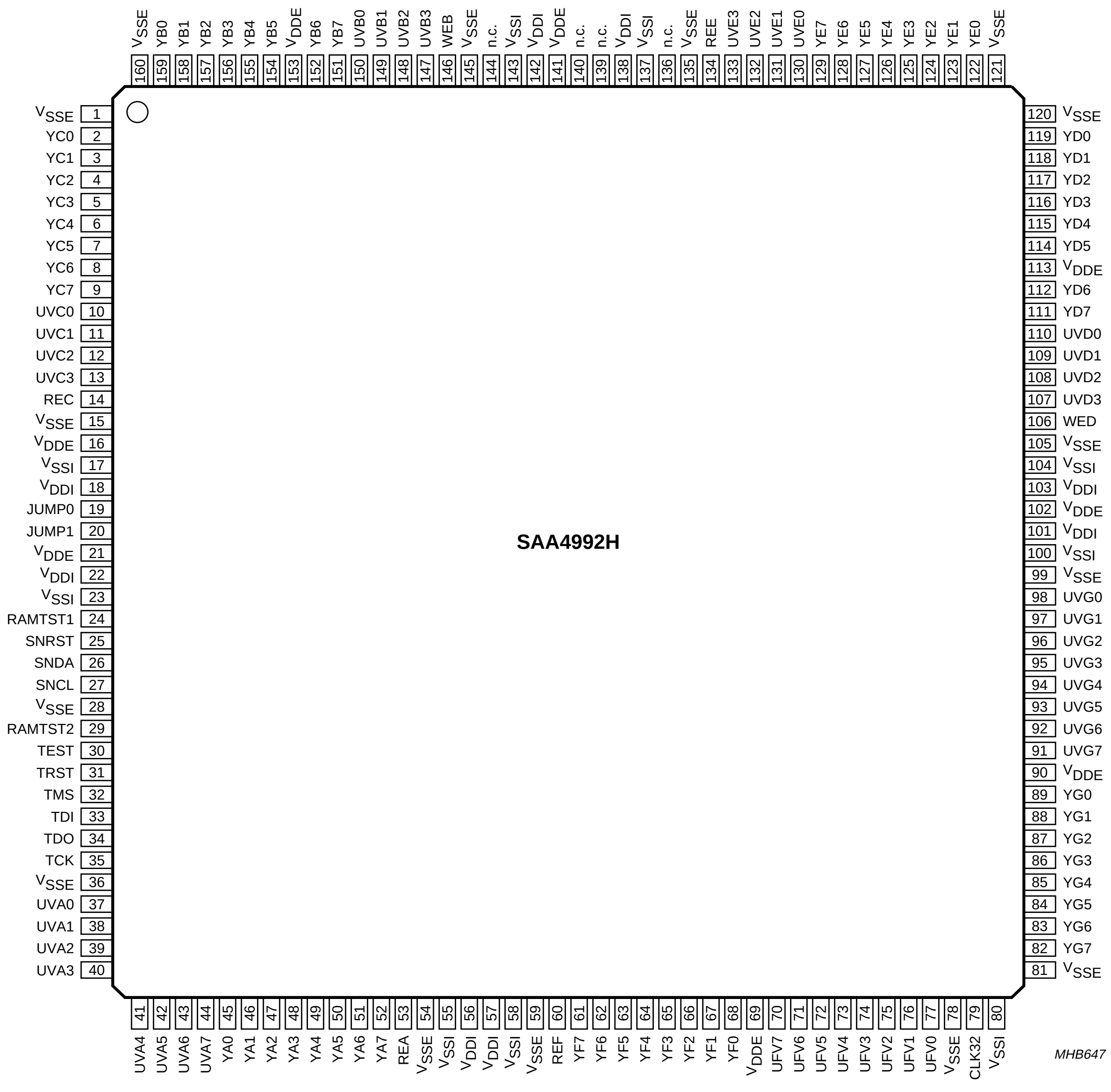


Fig.3 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The FAL (fal_top) module builds the functional top level of the SAA4992H. It connects the luminance data path (KER, kernel), the chrominance data path (COL, colour) and the luminance (de)compression (YDP, Y-DPCM) with SAA4992H inputs and outputs as well as controlling logic (LSE, line sequencer; SNE, SNERT interface). Outside of fal_top there are only the pad cells, boundary scan test cells, the boundary scan test controller, the clock tree, the test enable tree and the input port registers.

Figure 4 shows a simplified block diagram of fal_top. It displays the flow of pixel data (solid lines) and controls (broken lines) between the modules inside.

Basic functionality of the modules in fal_top is as follows:

- KER (kernel): Y (luminance) data path
- COL (colour): UV (chrominance) data path
- YDP (Y-DPCM): compression (and decompression) of luminance output (and input) data by Differential Pulse Code Modulation (DPCM)
- LSE (line sequencer): generate line frequent control signals
- SNE: Synchronous No parity Eight bit Reception and Transmission (SNERT) interface to a microcontroller.

The SNERT interface operates in a slave receive and transmit mode for communication with a microprocessor, which resides on peripheral circuits (e.g. SAA4978H) together with a SNERT master. The SNERT interface transforms serial data from the microprocessor (via the SNERT bus) into parallel data to be written into the SAA4992Hs write registers and parallel data from SAA4992Hs read registers into serial data to be sent to the microprocessor. The SNERT bus consists of 3 signals:

1. SNCL: used as serial clock signal, generated by the master
2. SNDA: used as bidirectional data line
3. SNRST: used as a reset signal, generated by the microprocessor to indicate the start of a transmission.

The processing of a video field begins on the rising edge of the RE_F input signal. As indicated in Fig.4, the SAA4992H expects its inputs and generates its outputs at the following clock cycles after RE_F (see Table 1).

Table 1 Clock cycle references

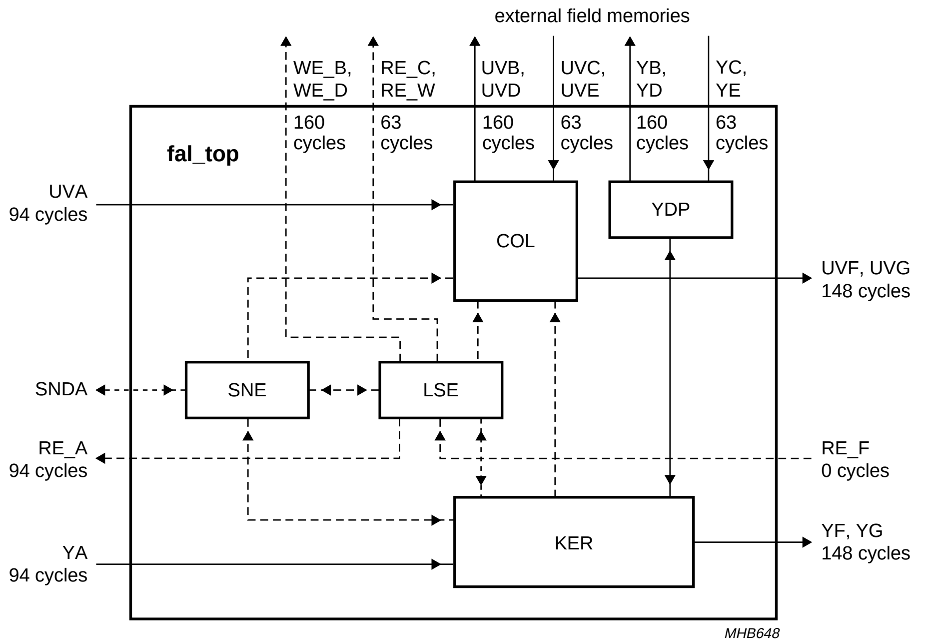
SIGNAL	LATENCY
RE_F	0
RE_C and RE_E	63 cycles + REceShift
YC, YE, UVC and UVE	63 cycles
RE_A	94 cycles + REaShift
YA and UVA	94 cycles
YF, YG, UVF and UVG	148 cycles + 3 input lines
WE_B and WE_D	160 cycles + 4 input lines + WEbdShift
YB, YD, UVB and UVD	160 cycles + 4 input lines

There is an algorithmic delay of 3 lines between input and output data. Therefore, the main data output on the F and G bus begins while the fourth input line is read. Writing to the B and D bus starts one input line later. The read and write enable signals RE_A, WE_B, RE_C, WE_D and RE_E can be shifted by control registers REaShift, WEbdShift and REceShift, which are implemented in the line sequencer.

The fal_top module itself reads the following control register bits(addresses):

- NrofFMs (017)
- MatrixOn (026)
- MemComp and MemDecom (026).

NrofFMs and MatrixOn are used to enable the D and G output bus, respectively. MemComp and MemDecom are connected to YDP to control luminance data compression and decompression. These control register signals are not displayed in Fig.4. Further information on the control registers is given in Chapter 8.



The solid lines represent pixel data; the broken lines represent controls.

Fig.4 Block diagram of fal_top.

8 CONTROL REGISTER DESCRIPTION

NAME	SNERT ADDRESS HEX	READ/ WRITE(1)	7	6	5	4	3	2	1	0	DESCRIPTION(2)
DNR/peaking/colour											
Kstep10	010	write; S									
Kstep0							X	X	X	X	set LUT value: k = 1/16 if difference below (**0 to 15**)
Kstep1			X	X	X	X					set LUT value: k = 1/8 if difference below (**0 to 15**)
Kstep32	011	write; S									
Kstep2							X	X	X	X	set LUT value: k = 2/8 if difference below (**0 to 30 in multiples of 2**)
Kstep3			X	X	X	X					set LUT value: k = 3/8 if difference below (**0 to 30 in multiples of 2**)
Kstep54	012	write; S									
Kstep4							X	X	X	X	set LUT value: k = 4/8 if difference below (**0 to 60 in multiples of 4**)
Kstep5			X	X	X	X					set LUT value: k = 5/8 if difference below (**0 to 60 in multiples of 4**)
Kstep76	013	write; S									
Kstep6							X	X	X	X	set LUT value: k = 6/8 if difference below (**0, 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, 96, 104, 112 or 120**)
Kstep7			X	X	X	X					set LUT value: k = 7/8 if difference below (**0, 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, 96, 104, 112 or 120**)
Gain_fix_y	014	write; S									
FixvalY							X	X	X	X	set fixed Y value; used when FixY = 1 or in left part of split screen (**0, 1/16 to 14/16 or 16/16**)
GainY				X	X	X					set gain in difference signal for adaptive DNR Y (**1/8, 1/4, 1/2, 1, 2 or 4**)
FixY			X								select fixed Y (**adaptive or fixed**) (full screen)
Gain_fix_uv	015	write; S									
FixvalUV							X	X	X	X	set fixed UV value; used when FixUV = 1 or in left part of split screen (**0, 1/16 to 14/16 or 16/16**)
GainUV				X	X	X					set gain in difference signal for adaptive DNR UV (**1/8, 1/4, 1/2, 1, 2 or 4**)
FixUV			X								select fixed UV (**adaptive or fixed**) (full screen)
Peak_Vcomp	016	write; S									
VecComp								X	X	X	set degree of horizontal vector compensation in Y DNR: (**0, 1/8, 2/8, 3/8, 4/8, 5/8, 6/8 or 7/8**) of the vector
PeakCoef			X	X	X	X					set vertical peaking level: (**0, +2, +3.5, +5, +6, x, x, x, x, x, x, x, x, –12, –6 or –2.5**) dB

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
DNR_Colour_mode	017	write; S									
ColourIn									X	X	select colour input format: (**4 : 1 : 1, 4 : 2 : 2, 4 : 2 : 2 DPCM or 4 : 2 : 2**)
ColourOut								X			select colour output format: (**4 : 1 : 1 or 4 : 2 : 2**)
NrofFMs							X				set number of field memories connected: (**1 or 2/3**)
ColOvl						X					select vector overlay on colour output: (**vector overlay or colour from video path**)
SlaveUVtoY					X						slave UV noise reduction to K factor of Y: (**separate or slaved**)
DnrSplit				X							select split screen mode for DNR: (**normal or split screen**)
DnrHpon			X								switch DNR high-pass on (DNR only active on low frequent spectrum: (**all through DNR or high bypassed**)
Vertical zoom											
Zoom1	018	write; F									
ZoomSt98									X	X	zoom line step bits 9 and 8; line step = vertical distance between successive output lines; usable range = 0 to 2 frame lines; resolution $^{1}/_{256}$ frame line
ZoomPo98					X	X					zoom start position bits 9 and 8; start position = vertical position of the top display line; usable range = 1 to 3 frame lines; resolution $^{1}/_{256}$ frame line
Zoom2	019	write; F									
ZoomSt70			X	X	X	X	X	X	X	X	zoom line step bits 7 to 0 (see above)
Zoom3	01A	write; F									
ZoomPo70			X	X	X	X	X	X	X	X	zoom start position bits 7 to 0 (see above)
Zoom4	01B	write; F									
ZoomEnVal							X	X	X	X	zoom run in value = number of lines without zoom active (**0 to 15** lines)
ZoomDiVal			X	X	X	X					zoom run out value = number of lines without zoom active (–**8 to +7** lines)

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
De-interlacer											
Proscan1	01C	write; S									
KlfLim							X	X	X	X	limitation of recursion factor in calculation of original line positions: (**1 to 16**); 1 limits to almost full recursion, 16 limits to no recursion
KlfOfs			X	X	X	X					The transfer curve of the de-interlacing filter coefficient is determined by the difference (Diff) between a line in the input field and the counterpart in the previous field shifted over the estimated motion vector. KlfOfs determines the bias of the transfer curve for the original input line, such that coefficient = KlfOfs + F(Diff), where the function F is calculated in the SAA4992H. The bias can take a value in the range (**0 to 15**), representing decreasing filter strength.
Proscan2	01D	write; S									
PlfLim							X	X	X	X	limitation of recursion factor in calculation of interpolated line positions: (**1 to 16**); 1 limits to almost full recursion, 16 limits to no recursion
PlfOfs			X	X	X	X					see KlfOfs; this offset applies to interpolated lines
Proscan3	01E	write; S									
PeakLim							X	X	X	X	Maximum that the peaked pixel is allowed to deviate from original pixel value: deviation (**0 to 30 in steps of 2**). Above this deviation, the peaked pixel is clipped to (original pixel + or – PeakLim).
PenInd			X	X	X	X					index to PenMed table **(–256, –128, –64, –32, –16, –8, –4, 0, 4, 8, 16, 24, 32, 64, 128 or 255)**; penalty for applying (vertical/temporal) median, in favour of applying vertical average within new field

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
Proscan4	01F	write; F									
PlfThr								X	X	X	Multiplier threshold at which to switch the lower limit of the filter coefficient for interpolated lines. Above this threshold, the differences corresponding to the two neighbouring lines are used as clipping parameters, below this threshold, the interpolated line difference is used as clipping level. This parameter can be used to optimize the de-interlacing quality in slowly moving edges; it is not likely to have effect if PlfLim is high.
ProDiv					X	X					Scaling factor to control the strength of the filtering for the interpolated lines. A value 0 means no scaling (normal filtering), while 3 means scaling by factor 8 (very strong filtering). This parameter can be used to adjust the de-interlacing to varying level of noise in the input picture; use higher scaling for higher noise.
UseVec				X							Enables use of estimated vectors to shift pixels from previous frame to the current time (**null vector or estimated vectors**). It is best switched to ‘null vector’, if vectors are unreliable.
KplOff			X								disable all recursion in calculating pixels for frame memory (**recursive or non recursive**); to be true SAA4991WP and digital scan emulation modes
General											
NrBlks	020	write; S									
NrBlks					X	X	X	X	X	X	number of blocks in active video (**6 to 53**, corresponds to 96 to 848 pixels), to be set as $\frac{1}{16}$ (number of active pixels per line + 15); take remarks on TotalPxDiv8 into consideration
TotalLnsAct98			X	X							total number of output lines (bits 9 and 8)
TotalLnsAct70	021	write; S	X	X	X	X	X	X	X	X	total number of output lines (bits 7 to 0)
TotalPxDiv8	022	write; S	X	X	X	X	X	X	X	X	Total number of pixels per line divided-by-8 (**80 to 128**, corresponds to 640 to 1024 pixels). The horizontal blanking interval is calculated as TotalPxDiv8 – 2 × NrBlks and has to be in the range from 12 to 124 (corresponds to 96 to 992 pixels). Conclusion: TotalPxDiv8 has to be set to 12 + 2 × NrBlks < TotalPxDiv8 < 124 + 2 × NrBlks and NrBlks has to be set to $\frac{TotalPxDiv8 - 124}{2} < NrBlks < \frac{TotalPxDiv8 - 12}{2}$
REaShift	023	write; S						X	X	X	shift of REa signal in number of pixels (**0, +1, +2, +3, –4, –3, –2 or –1**)

–

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
WEbdREceShift	024	write; S									
WEbdShift								X	X	X	shift of WEb and WEd signal in number of pixels (**0, +1, +2, +3, –4, –3, –2 or –1**)
REceShift				X	X	X					shift of REc and REe signal in number of pixels (**0, +1, +2, +3, –4, –3, –2 or –1**)
POR	025	write; S								X	power-on reset command, to be set high temporarily during start-up (**normal or reset**); note 3
Mode control											
Control1	026	write; F									
EstMode										X	Set estimator mode; **0** = line alternating use of left and right estimator: use in progressive scan except with vertical compress. **1** = field alternating use of left and right estimator: use in field doubling and progressive scan with vertical compress.
FilmMode									X		set film mode; **0** = video camera mode; **1** = film mode
UpcMode							X	X			select upconversion quality; **00** = full, **01** = economy (DPCM), **10** = SAA4991WP, **11** = SAA4990H
MatrixOn						X					set matrix output mode; **1** = double output, disabling vertical peaking; **0** = normal single output mode
EmbraceOn					X						Master enable for embrace mode (**off or on**); SwapMpr in control2 should be at ‘swap’ position to really cross-switch FM1 and FM3 field outputs. Should be set to logic 0 except in film mode and FM3 is present, or in SAA4991WP film mode and MemComp bit is active.
MemComp				X							set memory compression (luminance DPCM) (**off or on**)
MemDecom			X								set memory decompression (luminance DPCM) (**off or on**)

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
Control2	027	write; F									
QQcurr										X	Quincunx phase of current field (in TPM) (**phase0 or phase1**); this needs to toggle each time a new field comes from FM1. In phase0 the estimator operates on a checker-board pattern that starts with the left upper block; in phase1 the other blocks are estimated.
QQprev									X		quincunx phase of previous field (in TPM) (**phase0 or phase1**); this is the value of QQcur during the last estimate written into the temporal prediction memory
FldStat								X			Field status (**same input field or new input field**); reflects whether the output of FM1 is a new or a repeated field. This bit will toggle field by field in field doubling mode and is continuously HIGH in progressive output mode.
FieldWeYUV							X				enable writing FM2 and FM3 for both luminance and chrominance (recirculation of data for luminance alone can be controlled with OrigFmEnY and IntpFmEnY in Control3) (**off or on**)
OddFM1						X					odd input field (**even or odd**), this is to be set equal to the detected field interlace for the field that comes out of FM1
SwapMpr					X						Swap multi port RAMs (**normal or swap**); this bit needs to be set to get real frame data at the temporal position from FM1. If swapped, the current field (FM1) will be stored in the right line memory tree, while the original lines from the stored frame (FM2/3) are stored in the left memory tree. Should be set only in film mode if FM3 is present; EmbraceOn must be set as well.
VecOffs			X	X							Set vertical vector offset (**0, +1,** – **or** –**1**) frame lines; vertical offset of the right line memory tree with respect to the left line memory tree. A higher offset value means: on the right memory tree access to less delayed video lines is taken; in interlaced video operation, the vertical offset will be –1 with an odd field on the left side and +1 with an even field on the left. With non-interlaced input, vertical offset should be constantly 0. In film mode, vertical offset is dynamically switched between +1, 0 and –1.

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
Control3	028	write; F									
OddLeft										X	interlace (**even or odd**) phase of the field which is written to the left line memory tree (left MPRAM)
OrigFmEnY									X		enables writing luminance from de-interlacer in original field memory (FM2), otherwise recirculation of luminance that is just read from FM2 (**recirculate or update**)
IntpFmEnY								X			enables writing luminance from de-interlacer in interpolated field memory (FM3), otherwise recirculation of luminance that is just read from FM3 (**recirculate or update**)
FillTPM							X				Enables writing in temporal prediction memory (**keep or update**); FillTPM should be set to ‘keep’ in SAA4991WP/film mode, in those output fields where FM1 and FM2 contain the same motion phase. FillTPM should be set to ‘update’ in all other situations.
VertOffsDNR					X	X					Set vertical vector offset of DNR (**0, +1,** – **or** –**1**) frame lines; vertical offset of the right line memory tree with respect to the left line memory tree, before the swap action. A higher offset value means: on the right memory tree access to less delayed video lines is taken; in interlaced video operation, the vertical offset will be –1 with an odd field on the left side and +1 with an even field on the left. With non-interlaced input, vertical offset should be constantly logic 0; in film mode, vertical offset is dynamically switched between +1, 0 and –1. It should be noted that the signal OddFM1 is used to determine this offset.
Upconversion											
Upconv1	029	write; F									
UpcShFac					X	X	X	X	X	X	temporal interpolation factor used in luminance upconverter; value ranges from **0** (for current field position) **to 32** (for previous field position)
Upconv2	02A	write									
YVecClip		S						X	X	X	value used for coring the vertical vector component before application in the upconverter; range: **0 to 3.5** in steps of 0.5 line; should remain at logic 0 in normal operation
RollBack		F	X	X	X	X	X				roll back factor ranging from **0** (use 0% of estimated vectors) **to 16** (use 100% of estimated vectors)

NAME	SNERT ADDRESS HEX	READ/ WRITE(1)	7	6	5	4	3	2	1	0	DESCRIPTION(2)
Upconv3	02B	write; S									
MelzLfbm										X	SAA4991WP type local fallback method instead of more robust local fallback (**complex or SAA4991WP type fallback**)
Melzmemc									X		SAA4991WP film mode memory control (**normal or SAA4991WP type**); should be set in SAA4991WP film mode to ensure that only original lines are selected as output when UpcShFac is 0 or 32
MelDeint								X			use (as in SAA4991WP) horizontal motion compensated median for upconverter de-interlacing (**normal or SAA4991WP type de-interlacing**)
MixCtrl				X	X	X					Upconverter sensitivity: **0 to 3**: smoothness dependent weighting between vector shifted pixels and static pixels. 0 = sensitive to unsmoothness for taking more of the static pixels ‘conservative’, up to 3 = hardly sensitive to unsmoothness for taking more of static pixels ‘confident in vector shifting’. **4 to 7**: static weighting between vector shifted pixels and static pixels. 4 = take most of vector shifted pixels ‘confident in vector shifting’, up to 7 = take most of the static pixels ‘conservative’.
UpcColShiFac	0C4	write; F			X	X	X	X	X	X	temporal interpolation factor used in chrominance upconverter; value ranges from **0** (for current field position) **to 32** (for previous field position)
Motion estimator											
Motest1	02C	write; S									
PenOdd								X	X	X	additional penalty on vector candidates with odd vertical component (**0, 8, 16, 32, 64, 128, 256 or 511**)
SpcThr					X	X	X				Active when EstMode = 0; replace the spatial prediction of one estimator (left or right) by that of the other if the match error of the former exceeds that of the latter by more than (**0, 8, 16, 32, 64, 128, 256 or 511**). A higher threshold means the two estimators are very independent.
BmsThr			X	X							Active when EstMode = 0; select as estimated vector the output of the right estimator unless its match error exceeds that of the left estimator by more than (**0, 8, 16 or 32**). This parameter should normally be set to logic 0.

NAME	SNERT ADDRESS HEX	READ/ WRITE(1)	7	6	5	4	3	2	1	0	DESCRIPTION(2)
Motest2	02D	write; S									
TavLow										X	If the difference between the current vector and the previous one in the same spatial location is within a small window, then the two vectors are averaged to improve temporal consistency. TavLow is the lower threshold of this window (**1 or 2**).
TavUpp								X	X		see above; TavUpp is the upper threshold (**0, 4, 8 or 16**)
MedEns						X	X				scaling factor to reduce all sizes of update vectors in the ensemble with medium sized vector templates (**1, $\frac{1}{2}$, $\frac{1}{4}$ or $\frac{1}{8}$**)
LarEns				X	X						scaling factor to reduce all sizes of update vectors in the ensemble with large sized vector templates (**1, $\frac{1}{2}$, $\frac{1}{4}$ or $\frac{1}{8}$**)
Motest3	02E	write; F									
MotShiFac					X	X	X	X	X	X	Motion estimator shift factor, being the temporal position used in the estimator at which the matching is done; value **32** for matching at previous field position down **to 0** for matching at current field position. Keeping MotShiFac equal to UpShiFac in the next upconverted output field estimates for minimum matching errors (minimum Halo's). MotShiFac at value **16** gives the largest natural vector range (twice as large as with value 0 or 32). Going above the range with MotShiFac $\neq$ 16 is dealt with in SAA4992H by shifting towards 16, but for the horizontal and vertical component separately (consequence is that vector candidates tend to rotate towards the diagonal directions).

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
Motest4	02F	write; S									
PenRng										X	Penalty for vectors estimated on the first row and the first column (if left estimator is used) or the right column (if right estimator is used), whenever the spatial prediction candidate is selected (**16 or 64**). For noisy pictures, this register could be set to logic 1 to improve border processing in the estimator.
CndSet									X		choice of candidate set (**left or right**) for which data (Candidate1 to Candidate8) is written in this field (becomes active in next field); see note 3
ErrThr						X	X	X			threshold on block match error for considering a block to be bad (**16, 32, 64, 128, 256, 512, 1024 or 2032**)
ErrHbl				X	X						number of horizontally adjacent blocks that have to be all bad before considering an occurrence of a burst error (**1, 2, 4 or 8**) (counting of burst errors is read out with BlockErrCnt, address 0A8)
TstMod			X								to be kept to logic 1 for normal operation
Candidate1	090	write; S									
Candidat1								X	X	X	selection Candidate1 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update1						X	X				update for Candidate1 (**zero update, medium update, large update or zero update**)
Penalty1			X	X	X						penalty for Candidate1 (**0, 8, 16, 32, 64, 128, 256 or 511**)
Candidate2	091	write; S									
Candidat2								X	X	X	selection Candidate2 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update2						X	X				update for Candidate2 (**zero update, medium update, large update or zero update**)
Penalty2			X	X	X						penalty for Candidate2 (**0, 8, 16, 32, 64, 128, 256 or 511**)
Candidate3	092	write; S									
Candidat3								X	X	X	selection Candidate3 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update3						X	X				update for Candidate3 (**zero update, medium update, large update or zero update**)
Penalty3			X	X	X						penalty for Candidate3 (**0, 8, 16, 32, 64, 128, 256 or 511**)

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
Candidate4	093	write; S									
Candidat4								X	X	X	selection Candidate4 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update4						X	X				update for Candidate4 (**zero update, medium update, large update or zero update**)
Penalty4			X	X	X						penalty for Candidate4 (**0, 8, 16, 32, 64, 128, 256 or 511**)
Candidate5	094	write; S									
Candidat5								X	X	X	selection Candidate5 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update5						X	X				update for Candidate5 (**zero update, medium update, large update or zero update)**
Penalty5			X	X	X						penalty for Candidate5 (**0, 8, 16, 32, 64, 128, 256 or 511**)
Candidate6	095	write; S									
Candidat6								X	X	X	selection Candidate6 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update6						X	X				update for Candidate6 (**zero update, medium update, large update or zero update**)
Penalty6			X	X	X						penalty for Candidate6 (**0, 8, 16, 32, 64, 128, 256 or 511**)
Candidate7	096	write; S									
Candidat7								X	X	X	selection Candidate7 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update7						X	X				update for Candidate7 (**zero update, medium update, large update or zero update**)
Penalty7			X	X	X						penalty for Candidate7 (**0, 8, 16, 32, 64, 128, 256 or 511**)
Candidate8	097	write; S									
Candidat8								X	X	X	selection Candidate8 (**SpatLeft, SpatRight, TemporalRight, TemporalLeft, TemporalCentre, Null, Panzoom or Max**)
Update8						X	X				update for Candidate8 (**zero update, medium update, large update or zero update**)
Penalty8			X	X	X						penalty for Candidate8 (**0, 8, 16, 32, 64, 128, 256 or 511**)
PZpositionLeftUppX	098	write; S			X	X	X	X	X	X	X position of LeftUpp measurement point for pan-zoom calculations (resolution: 16 pixels)

NAME	SNERT ADDRESS HEX	READ/ WRITE[1]	7	6	5	4	3	2	1	0	DESCRIPTION[2]
PZpositionLeftUppY	099	write; S		X	X	X	X	X	X	X	Y position of LeftUpp measurement point for pan-zoom calculations (resolution: 4 lines)
PZpositionRightLowX	09A	write; S			X	X	X	X	X	X	X position of RightLow measurement point for pan-zoom calculations (resolution: 16 pixels)
PZpositionRightLowY	09B	write; S		X	X	X	X	X	X	X	Y position of RightLow measurement point for pan-zoom calculations (resolution: 4 lines)
PZvectorStartX	09C	write; F	X	X	X	X	X	X	X	X	X start value of pan-zoom vectors
PZvectorDeltaX	09D	write; F	X	X	X	X	X	X	X	X	X delta value of pan-zoom vectors
PZvectorStartY	09E	write; F	X	X	X	X	X	X	X	X	Y start value of pan-zoom vectors
PZvectorDeltaY	09F	write; F	X	X	X	X	X	X	X	X	Y delta value of pan-zoom vectors
Read data; note 3											
GlobalMSEmsb	0A0	read; F	X	X	X	X	X	X	X	X	Global Mean Square Error (MSE) = summation within a field period of squared differences in comparing vector shifted video from frame memory (FM2/3) with new field input (FM1) in those lines coinciding with new field lines. The window for the measurement is kept at 40 pixels horizontal and 20 field lines vertical from the border of the video. Measurements is only done in fields where the de-interlacer is active, otherwise reading is zero. In field doubling mode, MSE is zero at the end of every new input field.
GlobalMSElsb	0A1	read; F	X	X	X	X	X	X	X	X	
GlobalMTImsb	0A2	read; F	X	X	X	X	X	X	X	X	Global Motion Trajectory Inconsistency (MTI) = summation within a field period of squared differences comparing shifted video from frame memory (FM2/3 output) with filtered data that is rewritten to the frame memory (FM2/3 input) in those lines coinciding with new field lines. The window for the measurement is kept at 40 pixels horizontal and 20 field lines vertical from the border of the video. Measurement is done only in fields where de-interlacer is active, otherwise reading is zero; in field doubling mode, MTI is zero at the end of every new input field.
GlobalMTIlsb	0A3	read; F	X	X	X	X	X	X	X	X	
GlobalACTmsb	0A4	read; F	X	X	X	X	X	X	X	X	global activity (ACT) = summation over a field period of the horizontal plus the vertical components of the vectors of all blocks
GlobalACTlsb	0A5	read; F	X	X	X	X	X	X	X	X	
VectTempCons	0A6	read; F	X	X	X	X	X	X	X	X	Vector temporal consistency = summation over a field period of absolute differences of horizontal plus vertical components of vectors newly estimated for each block compared with those vectors estimated in the previous run at the same spatial block position. It should be noted that a lower figure implies better consistency.

NAME	SNERT ADDRESS HEX	READ/ WRITE(1)	7	6	5	4	3	2	1	0	DESCRIPTION(2)
VectSpatCons	0A7	read; F	X	X	X	X	X	X	X	X	Vector spatial consistency = summation over a field period of absolute differences of horizontal and vertical components of vectors compared with those of the neighbour blocks (L, R, U and D); in the comparison, all vector data is used from the previous estimator run. It should be noted that a lower figure implies better consistency
BlockErrCnt	0A8	read; F	X	X	X	X	X	X	X	X	burst error count (number of burst errors)
LeastErrSum	0A9	read; F	X	X	X	X	X	X	X	X	least error sum (summation over a field period of the smallest match error that the estimator has found for each block: indicates reliability of the estimation process)
YvecRangeErrCntmsb	0AA	read; F	X	X	X	X	X	X	X	X	Y vector range error count (number of vectors that have a vertical component that is out of range for upconversion at the chosen temporal position) (15 to 8)
YvecRangeErrCntlsb	0AB	read; F	X	X	X	X	X	X	X	X	Y vector range error count (7 to 0)
RefLineCountPrev	0AC	read; F	X	X	X	X	X	X	X	X	read out of (number of input (run-) lines – 40) used in previous field
RefLineCountNew	0AD	write; F	X	X	X	X	X	X	X	X	Write of [number of input (run-) lines – 40] to be used in new field (actual maximum number of input lines in normal operation: 292; register value 252). Nominally this is to be set as an exact copy of the value read from RefLineCountPrev before a new field starts. In case the effective number of input (run-) lines has increased, RefLineCountNew should, for one field, be set to 255. This will occur e.g. with decreasing vertical zoom magnification or changing from 525 lines video standard to 625 lines standard. If this is not done, a deadlock will occur with too few lines processed correctly by the motion estimator.
PanZoomVec0-X	0B0	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 0 (8-bit X value)
PanZoomVec0-Y	0B1	read									
FalconIdent		S	0								SAA4992H identification: fixed bit, reading this bit as zero means SAA4992H is present
PanZoomVec0-Y		F		X	X	X	X	X	X	X	pan-zoom vector 0 (7-bit Y value)
PanZoomVec1-X	0B2	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 1 (8-bit X value)
PanZoomVec1-Y	0B3	read									
StatusJump0		S	X								read out of configuration pin JUMP0
PanZoomVec1-Y		F		X	X	X	X	X	X	X	pan-zoom vector 1 (7-bit Y value)
PanZoomVec2-X	0B4	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 2 (8-bit X value)

NAME	SNERT ADDRESS HEX	READ/ WRITE(1)	7	6	5	4	3	2	1	0	DESCRIPTION(2)
PanZoomVec2-Y	0B5	read									
StatusJump1		S	X								read out of configuration pin JUMP1
PanZoomVec2-Y		F		X	X	X	X	X	X	X	pan-zoom vector 2 (7-bit Y value)
PanZoomVec3-X	0B6	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 2 (8-bit X value)
PanZoomVec3-Y	0B7	read; F		X	X	X	X	X	X	X	pan-zoom vector 3 (7-bit Y value)
PanZoomVec4-X	0B8	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 4 (8-bit X value)
PanZoomVec4-Y	0B9	read; F		X	X	X	X	X	X	X	pan-zoom vector 4 (7-bit Y value)
PanZoomVec5-X	0BA	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 5 (8-bit X value)
PanZoomVec5-Y	0BB	read; F		X	X	X	X	X	X	X	pan-zoom vector 5 (7-bit Y value)
PanZoomVec6-X	0BC	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 6 (8-bit X value)
PanZoomVec6-Y	0BD	read; F		X	X	X	X	X	X	X	pan-zoom vector 6 (7-bit Y value)
PanZoomVec7-X	0BE	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 7 (8-bit X value)
PanZoomVec7-Y	0BF	read; F		X	X	X	X	X	X	X	pan-zoom vector 7 (7-bit Y value)
PanZoomVec8-X	0AE	read; F	X	X	X	X	X	X	X	X	pan-zoom vector 8 (8-bit X value)
PanZoomVec8-Y	0AF	read; F		X	X	X	X	X	X	X	pan-zoom vector 8 (7-bit Y value)
EggSliceRgtMSB	0C0	read; F	X	X	X	X	X	X	X	X	result of right pixels egg-slice detector (15 to 8)
EggSliceRgtLSB	0C1	read; F	X	X	X	X	X	X	X	X	result of right pixels egg-slice detector (7 to 0)
EggSliceMixMSB	0C2	read; F	X	X	X	X	X	X	X	X	result of mixed pixels egg-slice detector (15 to 8)
EggSliceMixLSB	0C3	read; F	X	X	X	X	X	X	X	X	result of mixed pixels egg-slice detector (7 to 0)

Notes

1. S means semi static, used at initialization or mode changes; F means field frequent, in general updated in each display field.
2. Selectable items are marked bold.
3. Almost all of the R(ead) and W(rite) registers of SAA4992H are double buffered. The Write registers are latched by a signal called New_field. New_field gets set, when RE_f rises after RSTR (New_field is effectively at the start of active video). The Read registers are latched by a signal called Reg_upd. Reg_upd gets set, when half the number of active pixels of the fourth line of vertical blanking have entered the SAA4992H (Reg_upd will effectively be active 3 and a halve lines after the RE_a, RE_c and RE_e have ended). The only exceptional registers, which are not double buffered, are:
   a) Write register 025: power_on_reset
   b) Write register 02F, bit 1: CndSet
   c) Read register 0B0 to 0BF, 0AE and 0AF: pan_zoom_vectors, including FalconIdent (= 0), jump0 and jump1.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+3.6	V
I_{DD}	supply current	–	600	mA
I_o	output current	–	2.0	mA
V_i	input voltage for all I/O pins	–0.5	+3.6	V
T_{stg}	storage temperature	–55	+150	°C
T_j	junction temperature	0	125	°C

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	27	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		2.9	K/W

11 CHARACTERISTICS

V_{DD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{DD}	supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current		–	400	550	mA
V_{OH}	HIGH-level output voltage		2.4	–	–	V
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{IH}	HIGH-level input voltage		2.0	–	3.6	V
V_{IL}	LOW-level input voltage		0	–	0.8	V
I_{OL}	LOW-level output current		–	–	2	mA
$C_{o(L)}$	output load capacitance		–	–	50	pF
C_i	input capacitance		–	–	8	pF
I_{LI}	input leakage current		–	–	1	μA
Outputs; note 1; see Fig.5						
I_{OZ}	output current in 3-state mode	$–0.5 < V_o < 3.6$	–	–	1	μA
$t_{d(o)}$	output delay time		–	–	21	ns
$t_{h(o)}$	output hold time		4	–	–	ns
SR	slew rate		300	–	700	mV/ns
Inputs; note 2; see Fig.5						
$t_{su(i)}$	input set-up time		8	–	–	ns
$t_{h(i)}$	input hold time		2	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input CLK32; see Fig.5						
t_r	rise time		–	–	4	ns
t_f	fall time		–	–	4	ns
δ	duty factor		40	–	60	%
T_{cy}	cycle time		30	–	39	ns
SNERT interface; see Fig.7						
t_{SNRSTH}	SNRST pulse HIGH time		500	–	–	ns
$t_{d(SNRST-SNCL)}$	delay SNRST pulse to SNCL LOW time		200	–	–	ns
$T_{cy(SNCL)}$	SNCL cycle time		0.5	–	1	μs
$t_{su(i)(SNCL)}$	input set-up time to SNCL		53	–	–	ns
$t_{h(i)(SNCL)}$	input hold time to SNCL		10	–	–	ns
$t_{h(o)}$	output hold time		30	–	–	ns
$t_{d(o)}$	output delay time		–	–	330	ns
$t_{o(en)}$	output enable time		210	–	–	ns
BST interface; see Fig.6						
$T_{cy(BST)}$	BST cycle time		–	1	–	μs
$t_{su(i)(BST)}$	input set-up time		3	–	–	ns
$t_{h(i)(BST)}$	input hold time		6	–	–	ns
$t_{h(o)(BST)}$	output hold time		4	–	–	ns
$t_{d(o)(BST)}$	output delay time		–	–	30	ns

Notes

1. Timing characteristics are measured with C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ.
2. All inputs except SNERT, CLK32 and BST.

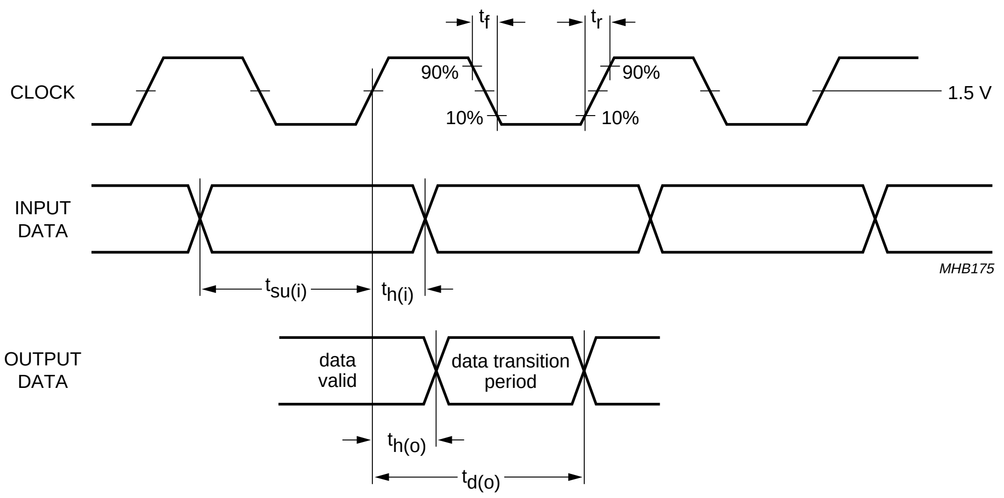


Fig.5 Data input/output timing diagram.

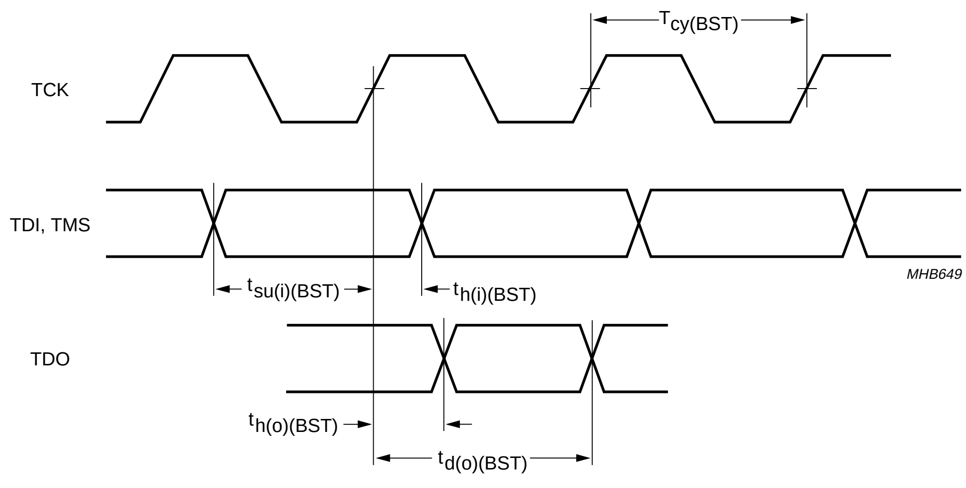


Fig.6 Boundary scan test interface timing diagram.

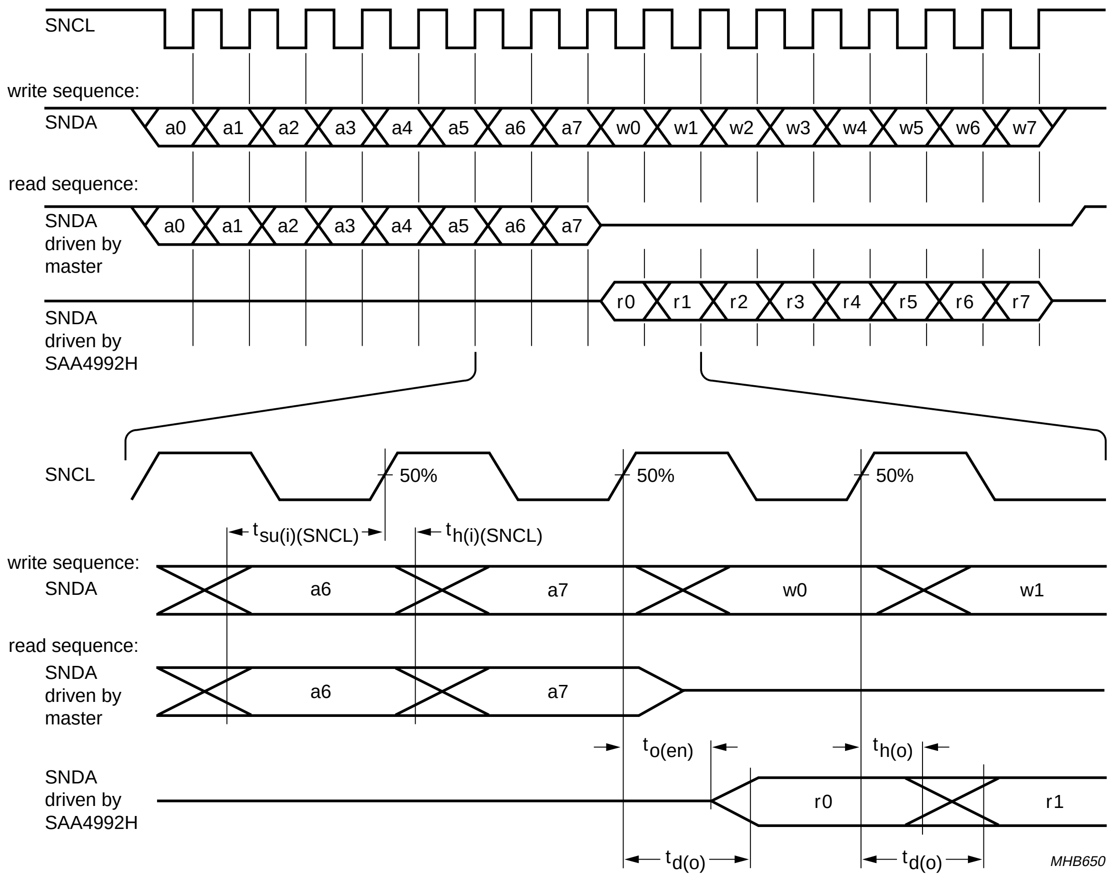


Fig.7 SNERT interface timing diagram.

Table 2 YUV formats; note 1

I/O PIN(1)	4 : 1 : 1 FORMAT(2)				4 : 2 : 2 FORMAT		4 : 2 : 2 DPCM FORMAT(2)	
YX7	Y07	Y17	Y27	Y37	Y07	Y17	Y07	Y17
YX6	Y06	Y16	Y26	Y36	Y06	Y16	Y06	Y16
YX5	Y05	Y15	Y25	Y35	Y05	Y15	Y05	Y15
YX4	Y04	Y14	Y24	Y34	Y04	Y14	Y04	Y14
YX3	Y03	Y13	Y23	Y33	Y03	Y13	Y03	Y13
YX2	Y02	Y12	Y22	Y32	Y02	Y12	Y02	Y12
YX1	Y01	Y11	Y21	Y31	Y01	Y11	Y01	Y11
YX0	Y00	Y10	Y20	Y30	Y00	Y10	Y00	Y10
UVX7	U07	U05	U03	U01	U07	V07	UC03	VC03
UVX6	U06	U04	U02	U00	U06	V06	UC02	VC02
UVX5	V07	V05	V03	V01	U05	V05	UC01	VC01
UVX4	V06	V04	V02	V00	U04	V04	UC00	VC00
UVX3	X	X	X	X	U03	V03	X	X
UVX2	X	X	X	X	U02	V02	X	X
UVX1	X	X	X	X	U01	V01	X	X
UVX0	X	X	X	X	U00	V00	X	X

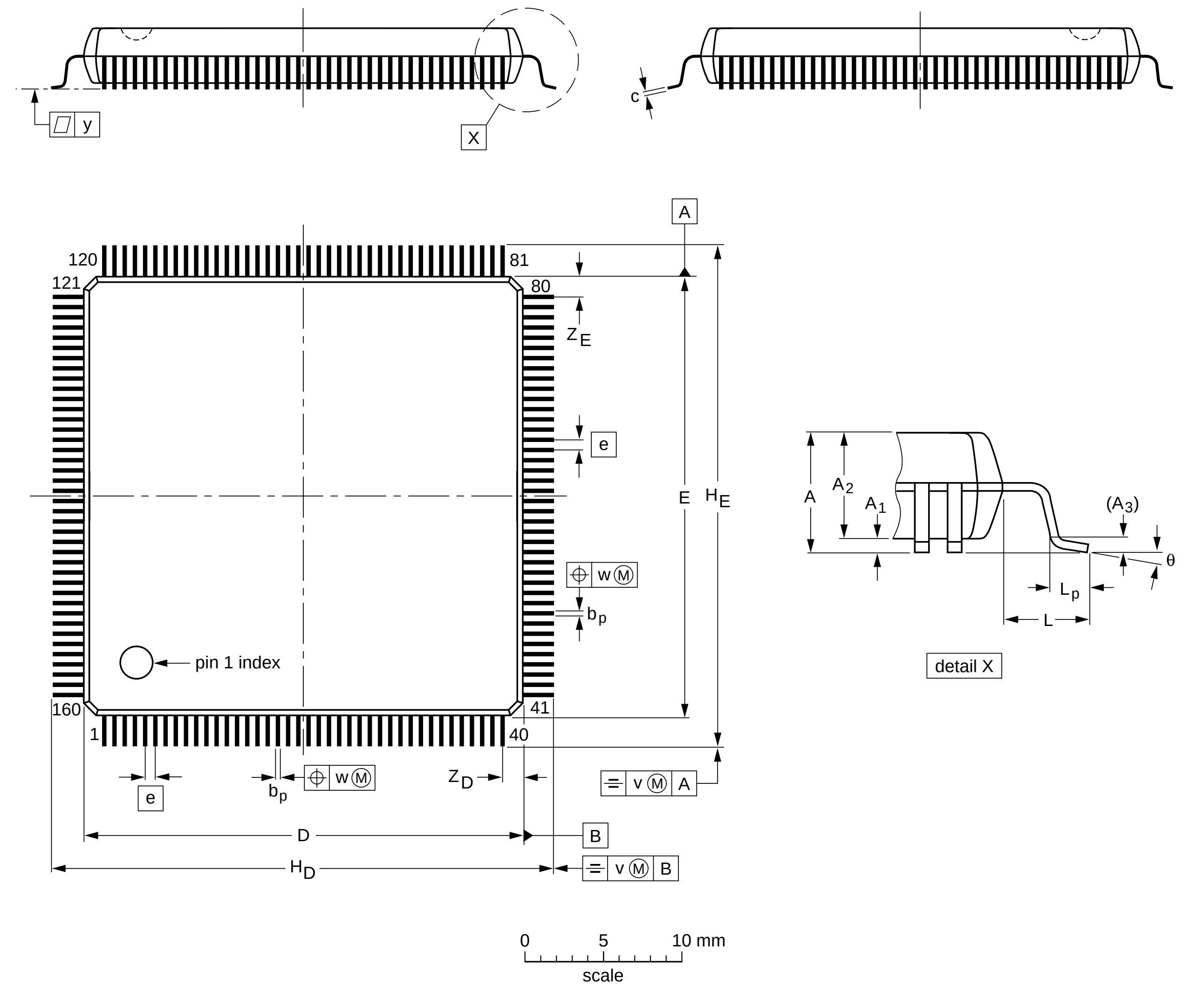
Notes

1. Index X refers to different I/O buses:
   a) X = A: input from 1st field memory
   b) X = B: output to 2nd field memory
   c) X = C: input from 2nd field memory
   d) X = D: output to 3rd field memory
   e) X = E: input from 3rd field memory
   f) X = F: main output
   g) X = G: 2nd output for matrix purposes.

   The first index digit defines the sample number, the second defines the bit number.
2. X = don’t care or not available.

12 PACKAGE OUTLINE

**QFP160: plastic quad flat package;
160 leads (lead length 1.6 mm); body 28 x 28 x 3.4 mm; high stand-off height** **SOT322-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	4.07	0.50 0.25	3.60 3.20	0.25	0.38 0.22	0.23 0.13	28.1 27.9	28.1 27.9	0.65	31.45 30.95	31.45 30.95	1.6	1.03 0.73	0.3	0.13	0.1	1.5 1.1	1.5 1.1	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT322-2	135E12	MS-022				~~99-11-03~~ 00-01-19

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

15 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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