DATA SHEET

SAA7152
Digital Video Comb Filter (DCF)

Product specification
File under Integrated Circuits, IC02

August 1996

Philips
Semiconductors

PHILIPS

Digital Video Comb Filter (DCF) SAA7152

FEATURES

- Comb filter circuit for luminance and chrominance separation
- Applicable for standards
  - PAL B/G, M and N
  - PAL 4.43 (525 lines, 60 Hz)
  - NTSC M and N
  - NTSC 4.43 (50 and 60 Hz)
- Luminance and chrominance bypasses with short delay in case of no filtering
- Line-locked system clock; CCIR-compatible
- I^2C-bus controlled

GENERAL DESCRIPTION

The CMOS digital comb filter circuit is located between video analog-to-digital converters and the video multistandard decoder SAA7151B (not applicable for SAA7191B). The two-dimensional filtering is only appropriate for standard signals from a source with constant phase relationship between subcarrier signal and horizontal frequency. The comb-filter has to be switched off for VTR-signals and for separate VBS and C signals. In VCR and S-Video operation the luminance low-pass and the chrominance bandpass parts can still be used for noise reduction purposes. The processing delay is:

$21 \times$ LL27 clocks in active mode, or

$3 \times$ LL27 in short delay bypass mode (BYPS = 1)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 11, 34, 44)	4.5	5.0	5.5	V
I_P	total supply current	–	85	180	mA
V_i	input levels	TTL-compatible			
V_o	output levels	TTL-compatible			
LL27	typical system clock frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7152	44	PLCC	plastic	SOT187 (1)

Note

1. SOT187-2; 1997 January 06.

BLOCK DIAGRAM

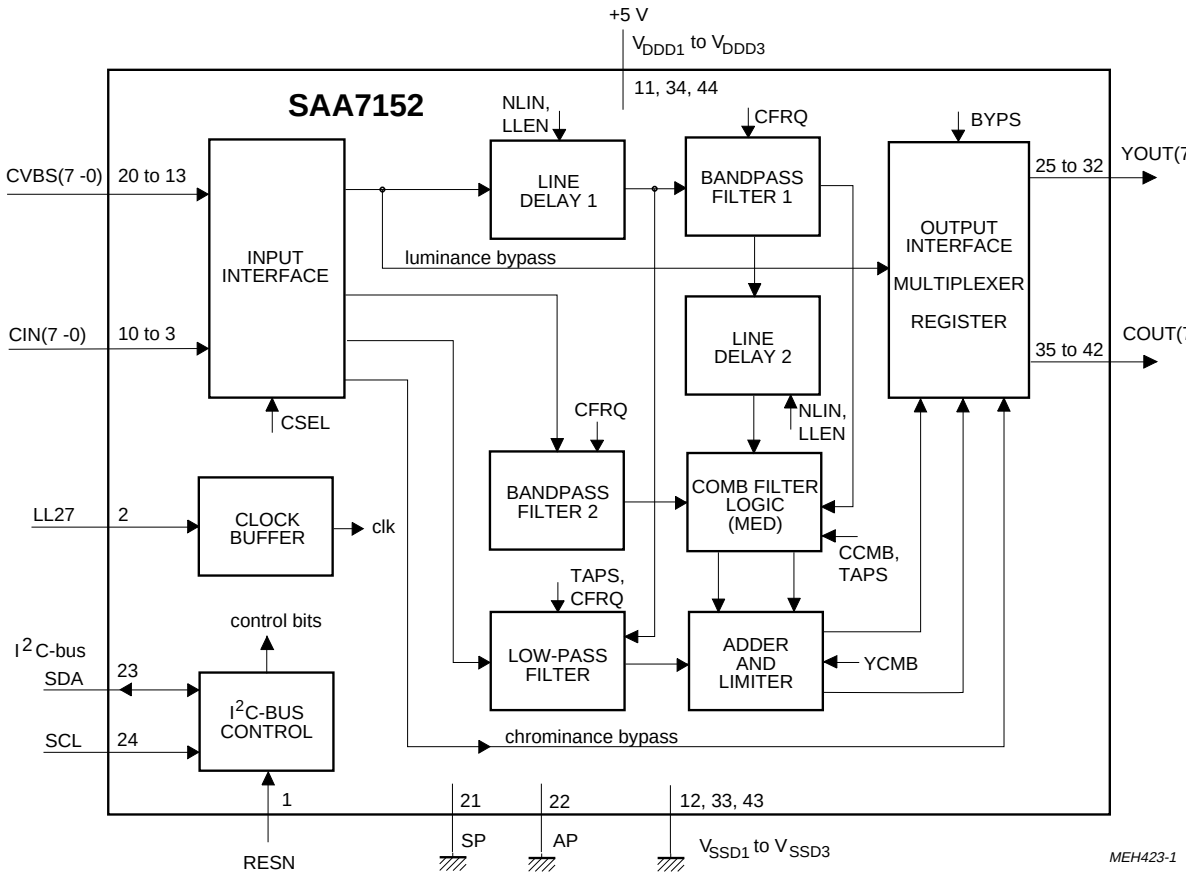


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RESN	1	reset input; active low
LL27	2	line-locked system clock input (27 MHz)
CIN0	3	chrominance input data bits CIN0 to CIN7
CIN1	4	
CIN2	5	
CIN3	6	
CIN4	7	
CIN5	8	
CIN6	9	
CIN7	10	
V_{DD1}	11	+5 V supply input
V_{SS1}	12	ground 1 (0 V)
CVBS0	13	CVBS input data bits 0 to 7
CVBS1	14	
CVBS2	15	
CVBS3	16	
CVBS4	17	
CVBS5	18	
CVBS6	19	
CVBS7	20	
SP	21	connected to ground (shift pin for testing)
AP	22	connected to ground (action pin for testing)
SDA	23	I^2C-bus data line
SCL	24	I^2C-bus clock line
YOUT7	25	luminance (Y) output data bits 7 to 0
YOUT6	26	
YOUT5	27	
YOUT4	28	
YOUT3	29	
YOUT2	30	
YOUT1	31	
YOUT0	32	
V_{SS2}	33	ground 2 (0 V)
V_{DD2}	34	+5 V supply input 2

SYMBOL	PIN	DESCRIPTION
COUT7	35	chrominance (C) output data bits 7 to 0
COUT6	36	
COUT5	37	
COUT4	38	
COUT3	39	
COUT2	40	
COUT1	41	
COUT0	42	
V_{SS3}	43	ground 3 (0 V)
V_{DD3}	44	+5 V supply input 3

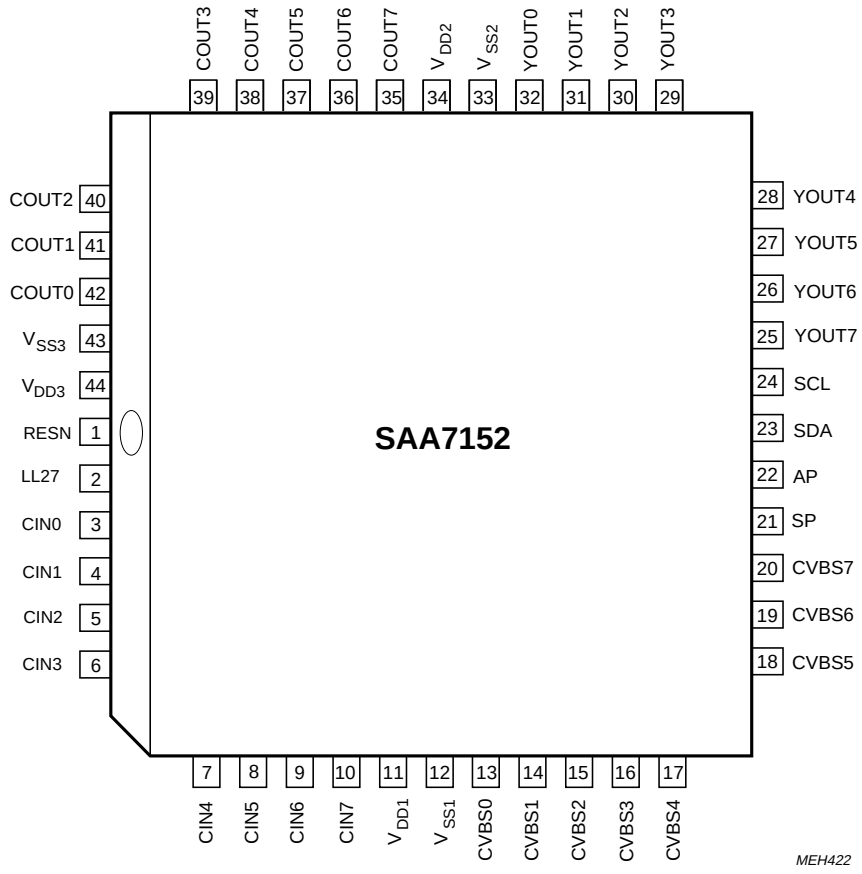


Fig.2 Pin configuration.

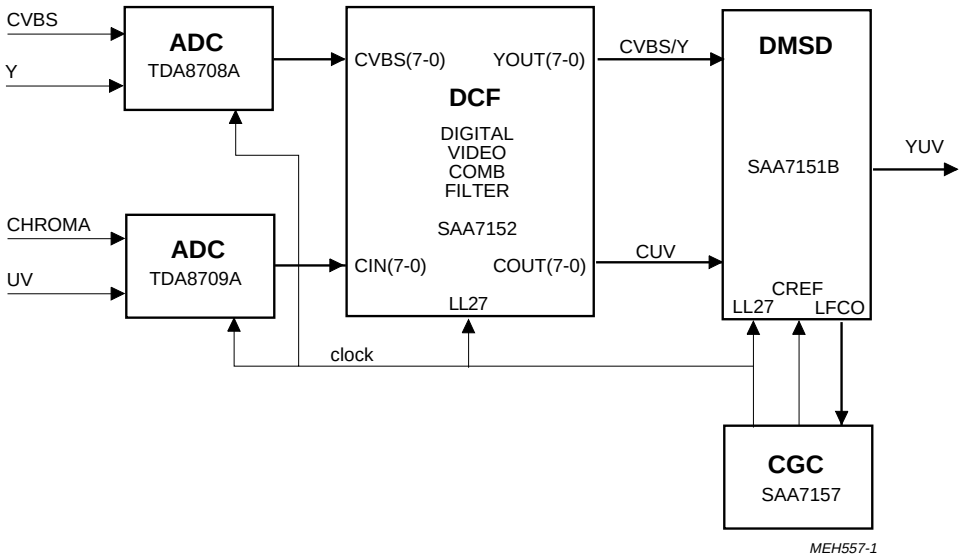


Fig.3 System environment.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	.....	DATAn	A	P

S	=	start condition
SLAVE ADDRESS	=	1011 0010 (B2 h)
A	=	acknowledge, generated by the slave
SUBADDRESS (1)	=	subaddress byte (Table 1)
DATA	=	data byte (Table 1)
P	=	stop condition
X	=	read/write control bit
		X = 0, order to write (the circuit is slave receiver)
		X = 1, order to read (the circuit is slave transmitter)

Note

1. If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I^2C-bus; subaddress and data bytes for writing (after X = 0 in address byte)

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Controls	00	BYPS	CSEL	CCMB	YCMB	TAPS	CFRQ	NLIN	LLEN

Function of the bits of Table 1:

BYPS	Select bypass with a short delay; all other functions are disabled:	0 = no bypass
		1 = comb filter bypassed (delay is 3 LLC)
CSEL	Input mode select:	0 = CVBS selected
		1 = Y/C selected
CCMB	Select comb filtering	0 = chrominance is bandpassed
		1 = chrominance is comb-filtered
YCMB	Enable chrominance substruction from CVBS signal:	0 = disabled, CVBS/Y signal is only low-passed
		1 = enabled (chrominance trap or comb filtering)
TAPS	Selects tap for switching Y and C to adder:	0 = for bandpass/low-pass combination
		1 = for comb filter active
CFRQ	Select centre frequency and matching factor of chrominance filter:	0 = 4.43 MHz
		1 = 3.58 MHz
NLIN	Select delay (number of lines):	0 = 4-line comb filter for standard PAL
		1 = 2-line filter for standard NTSC
LLEN	Selects the number of clocks for each line delay:	0 = 1728 clocks (625 lines; 50 Hz)
		1 = 1716 clocks (525 lines; 60 Hz)

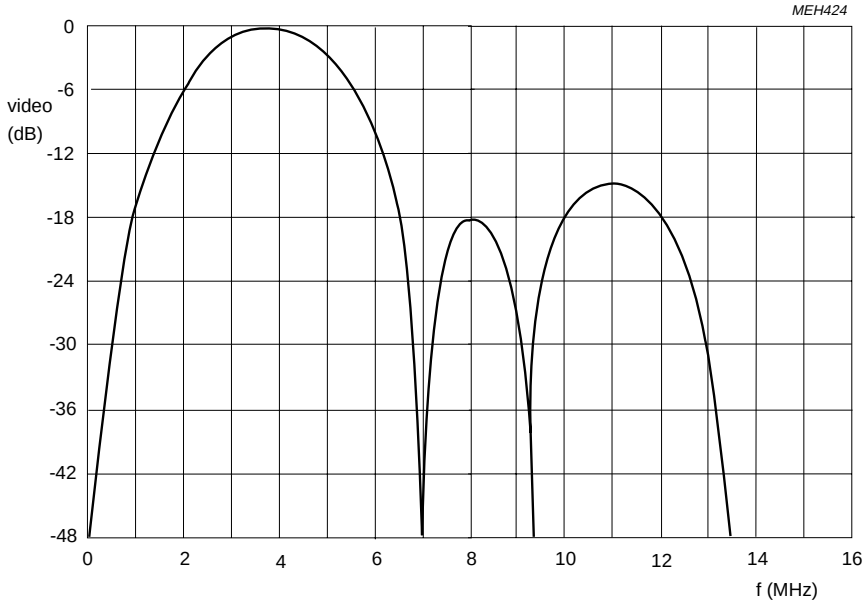


Fig.4 Frequency response of bandpass filters 1 and 2 with CFRQ-bit = 1.

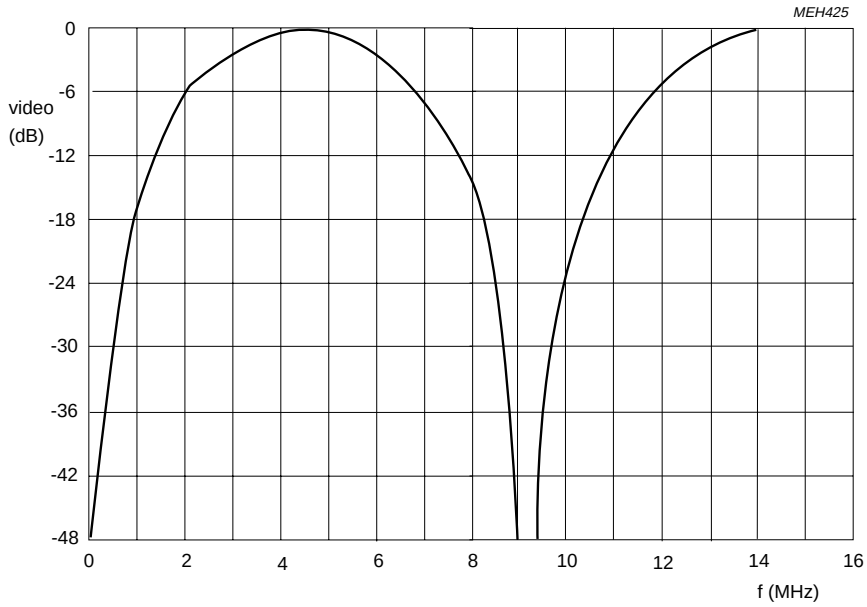


Fig.5 Frequency response of bandpass filters 1 and 2 with CFRQ-bit = 0.

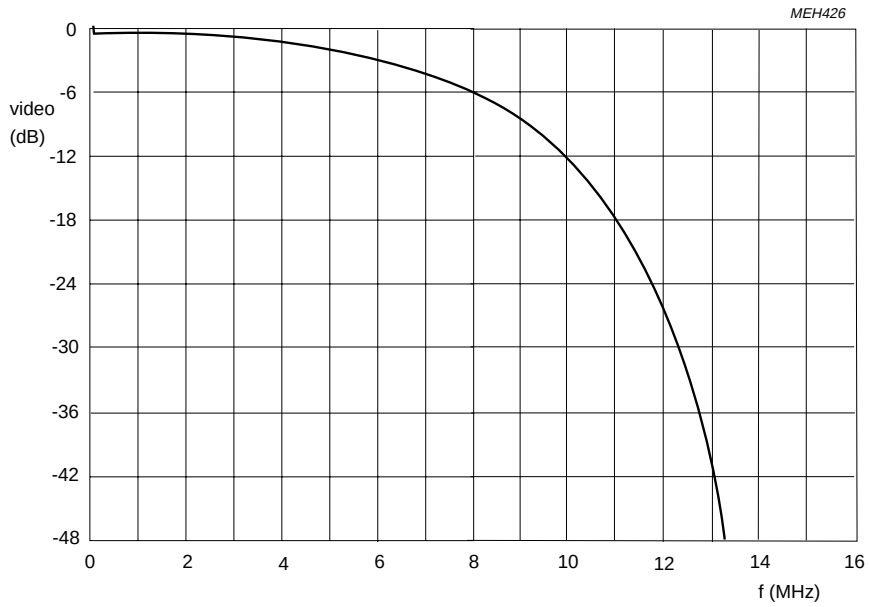


Fig.6 Frequency response of low-pass filter with CFRQ-bit = 1.

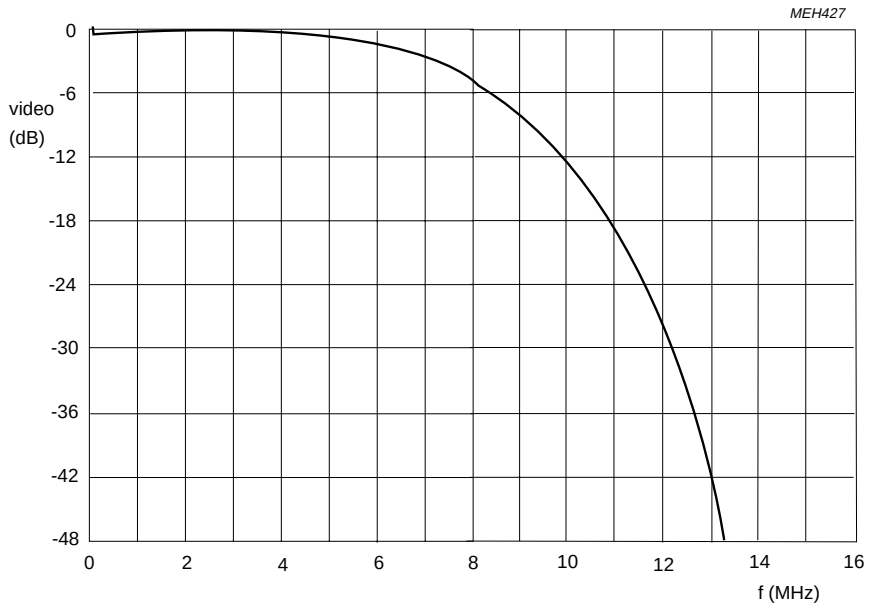


Fig.7 Frequency response of low-pass filter with CFRQ-bit = 0.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 11, 34, 44)	–0.5	7.0	V
V_I	voltage on all inputs	–0.5	V_{DD} + 0.5	V
V_O	voltage on all outputs ($I_{O\,max}$ = 20 mA)	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	1.0	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling(1) for all pins	–	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended (see *"Handling MOS Devices"*).

CHARACTERISTICS

V_{DD1} to V_{DD3} = 5 V; T_{amb} = 0 to 70 °C and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 11, 34, 44)		4.5	5.0	5.5	V
I_{DD}	total supply current (pins 11, 34, 44)	V_{DD} = 5 V; inputs LOW; outputs not connected	–	85	180	mA
I^2C-bus, SDA and SCL (pins 23 and 24)						
V_{IL}	input voltage LOW		–0.5	–	1.5	V
V_{IH}	input voltage HIGH		3	–	V_{DD}+0.5	V
$I_{23, 24}$	input current		–	–	±10	µA
I_{ACK}	output current on pin 23	acknowledge	3	–	–	mA
V_{OL}	output voltage at acknowledge	I_{23} = 3 mA	–	–	0.4	V
Data and clock inputs (pins 2 to 10 and pins 13 to 20)						
V_{IL}	LL27 input voltage (pin 2)	LOW	–0.5	–	0.6	V
V_{IH}		HIGH	2.4	–	V_{DD}+0.5	V
V_{IL}	other input voltages	LOW	–0.5	–	0.8	V
V_{IH}		HIGH	2.0	–	V_{DD}+0.5	V
I_{leak}	input leakage current		–	–	10	µA
C_I	input capacitance	data inputs	–	–	8	pF
		clock inputs	–	–	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	–	–	ns
$t_{HD.DAT}$	input data hold time		3	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data outputs (pins 25 to 32 and pins 35 to 42)						
V_{OL}	output voltage LOW		0	–	0.6	V
V_{OH}	output voltage HIGH		2.4	–	V_{DD}	V
C_L	load capacitor		8	–	25	pF
Timing of data outputs		Fig.8				
t_{OH}	output signal hold time from positive edge of LL27	C_L = 8 pF	3	–	–	ns
t_{OD}	output delay from positive edge of LL27	C_L = 25 pF	–	–	32	ns
Line locked clock input LL27 (pin 2)		Fig.8				
t_{LL27}	cycle time	note 1	35	–	39	ns
t_p	duty factor	t_{LL27H} / t_{LL27}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns

Note

1. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

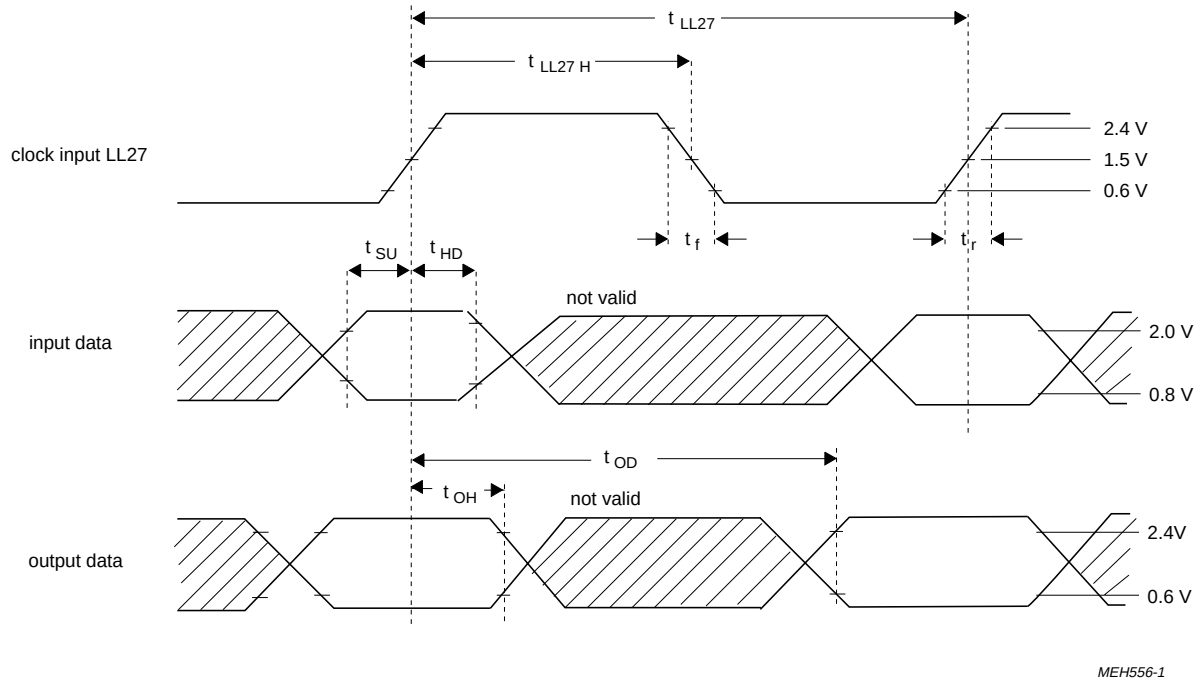
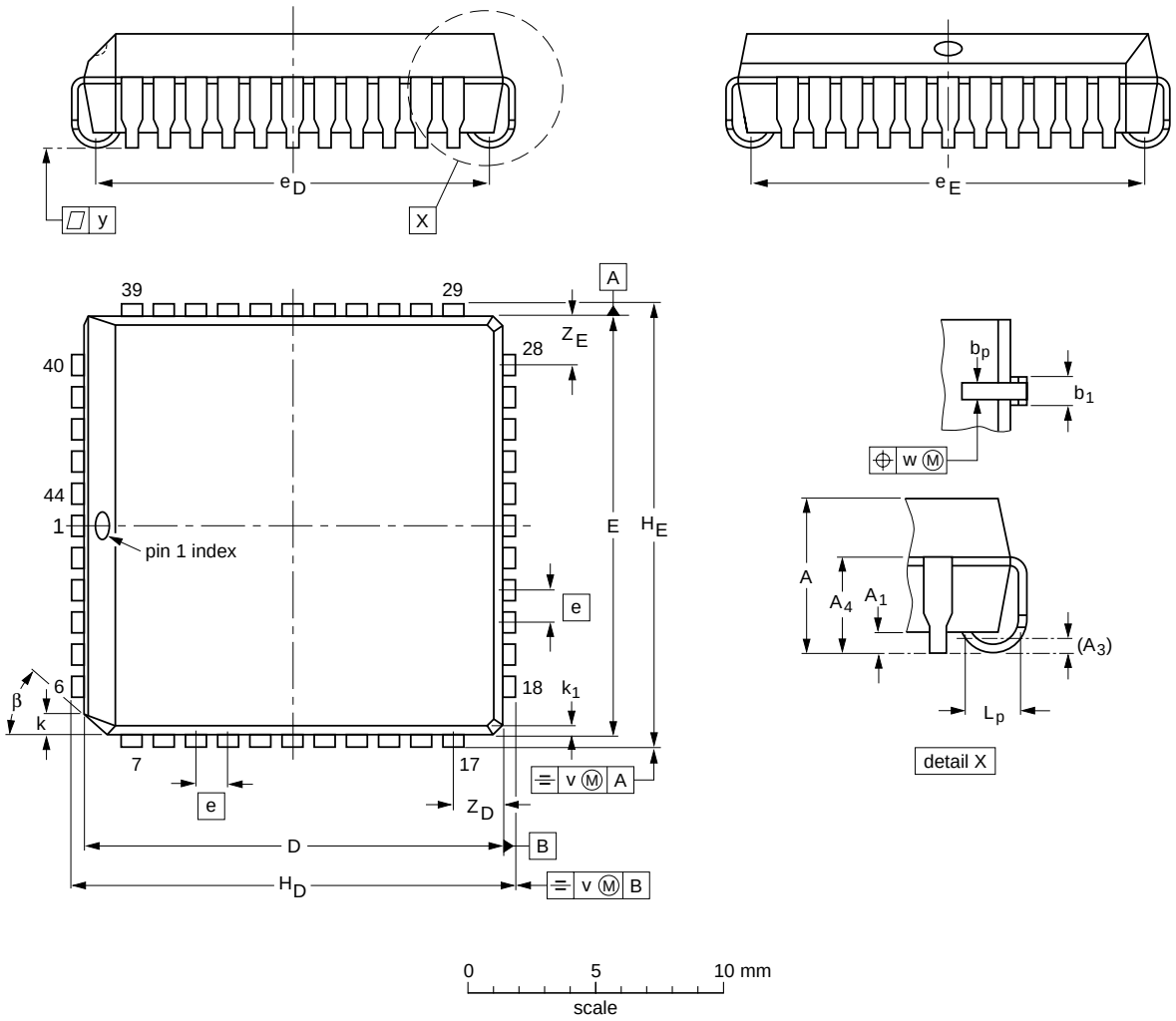


Fig.8 Data input and output timing.

PACKAGE OUTLINE

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC and QFP packages.

The choice of heating method may be influenced by larger PLCC or QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

PLCC

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

QFP

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

METHOD (PLCC AND QFP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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