DIGITAL FILTER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

GENERAL DESCRIPTION

The SAA7220 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. For descriptive purposes, the SAA7220 is referred to as the B-chip and the SAA7210 as the A-chip.

Features

- 16-bit serial data input (two's complement)
- Interpolated data replaces erroneous data samples
- −12 dB attenuation via the active LOW attenuation input control (ATSB)
- Smoothed transitions before and after muting
- Two identical finite impulse response transversal filters each with a sampling rate of four times that of the normal digital audio data
- Digital audio output of 32-bit words transmitted in biphase-mark code
- I^2S data transfer between SAA7210 and 16-bit dual DAC (TDA1541)

QUICK REFERENCE DATA

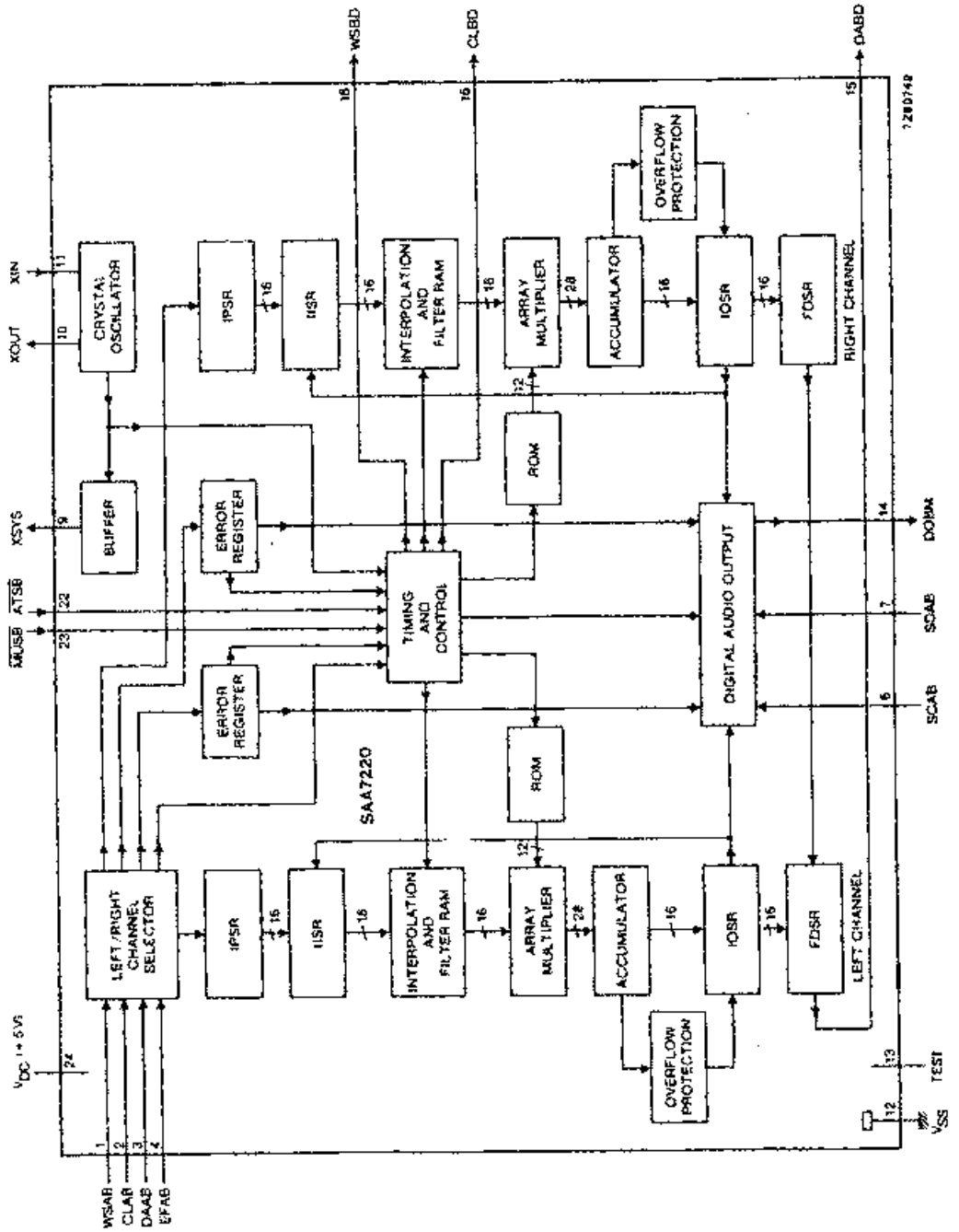
Supply voltage (pin 24)	V_{DD}	typ.	5 V
Supply current (pin 24)	I_{DD}	typ.	180 mA
Input voltage ranges			
WSAB, DAAB, EFAB, SDAB,			
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$			
Input voltage LOW	V_{IL}		−0,3 to +0,8 V
Input voltage HIGH	V_{IH}		2,0 to V_{DD} +0,5 V
Output voltage ranges			
DABD, CLBD, WSBD			
Output voltage LOW	V_{OL}		0 to 0,4 V
Output voltage HIGH	V_{OH}		2,4 to V_{DD} V
DOBM			
Voltage across a 75 Ω load via attenuator; see Fig. 10 (peak-to-peak value)	$V_{L(p-p)}$		0,4 to 0,6 V
Oscillator operating frequency XTAL	f_{XTAL}	typ.	11,2896 MHz
Operating ambient temperature range	T_{amb}		−20 to +70 °C

Note

All outputs are short-circuit protected except crystal oscillator output.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

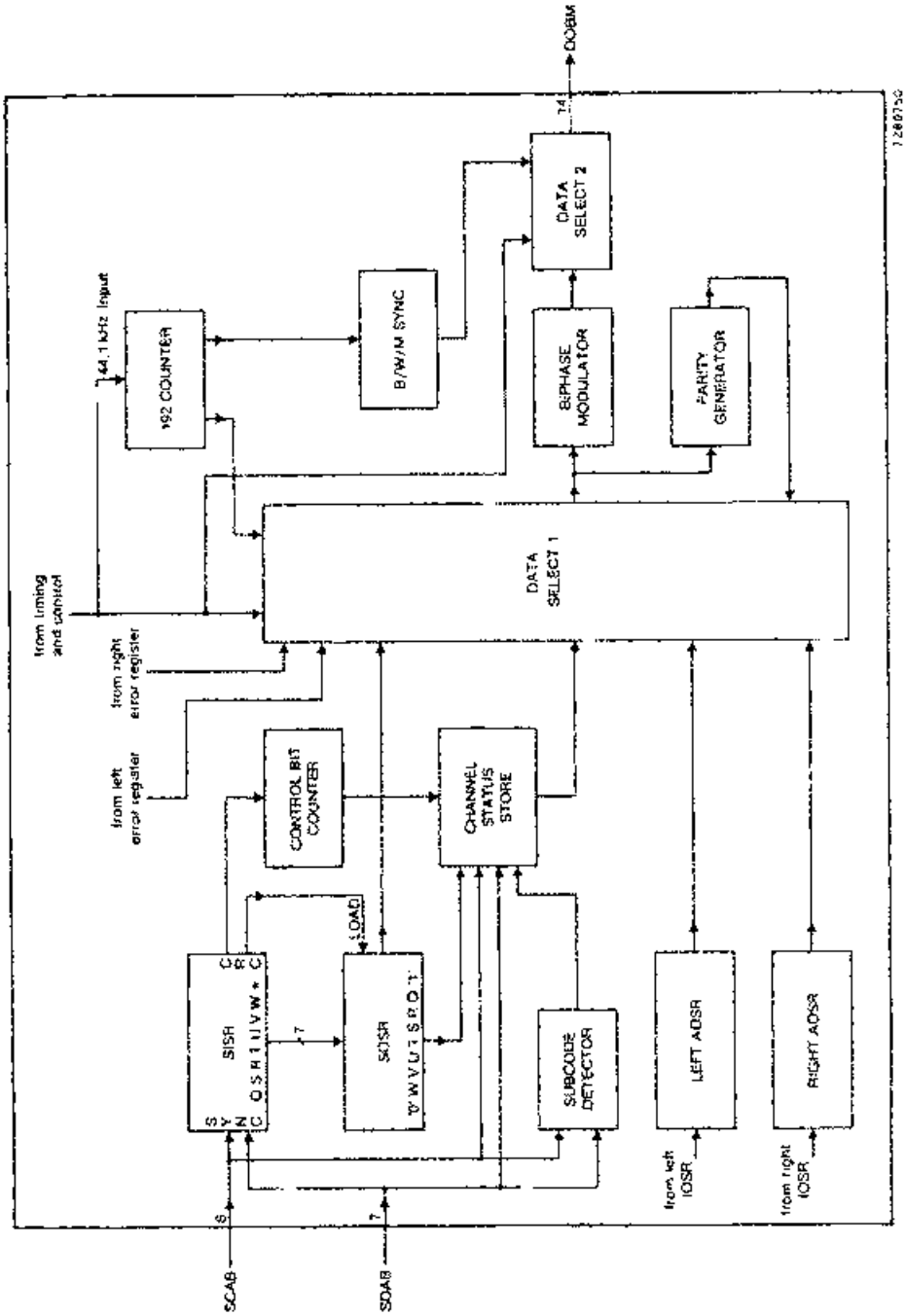


Where:

IPSR = Input Shift Register
IISR = Intermediate Input Shift Register
IOSR = Intermediate Output Shift Register
FOSR = Filter Data Shift Register

Fig. 1 Digital filter block diagram.

DEVELOPMENT DATA



Where:

SISR = Subcode Input Shift Register
SOSR = Subcode Output Shift Register
IOSR = Intermediate Output Shift Register
AOSR = Audio Output Shift Register
• = Subcode word error flag

Fig. 2 Digital audio output block diagram.

PINNING

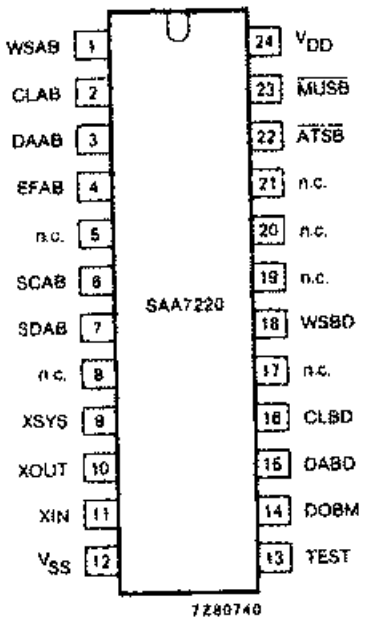


Fig. 3 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	WSAB	**Word Select:** input from A-chip.
2	CLAB	**Clock:** input from A-chip; has an internal pull-up.
3	DAAB	**Data:** input from A-chip.
4	EFAB	**Error Flag:** active HIGH input from A-chip indicating unreliable data. This input has an internal pull-down.
5	n.c.	not connected.
6	SCAB	**Subcode Clock:** a 10-bit burst clock 2,8224 MHz (typ.) input which synchronizes the subcode data. This input has an internal pull-up.
7	SDAB	**Subcode Data:** a 10-bit burst of data, including flags and sync bits serially input from the A-chip once per frame clocked by burst clock input SCAB (see Fig. 8). This input has an internal pull-down.
8	n.c.	not connected.
9	XSYS	**System clock output:** 11,2896 MHz (typ.) output to DAC and to A-chip as slave clock input.
10	XOUT	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
11	XIN	**Crystal oscillator input:** input from crystal oscillator or slave clock.

pin no.	mnemonic	description
12	V_{SS}	**Ground:** circuit earth potentional.
13	TEST	**Test input:** this input has an internal pull-down. In normal operation pin 13 should be open-circuit or connected to V_{SS}.
14	DOBM	**Digital audio output:** this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data. Transmission is by biphase-mark code.
15	DABD	**Data:** this output which is fed to the DAC, together with its clock (CLBD) and word select (WSBD) outputs, conforms to the I^2S format (see Fig. 7).
16	CLBD	**Clock:** output to DAC.
17	n.c.	not connected.
18	WSBD	**Word Select:** output to DAC.
19	n.c.	not connected.
20	n.c.	not connected.
21	n.c.	not connected.
22	$\overline{ATSB}$	**Attenuation:** when active LOW this control input provides −12 dB attenuation. This input has an internal pull-up.
23	$\overline{MUSB}$	**Mute:** active LOW control input with internal pull-up.
24	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

General

The SAA7220 incorporates the following functions:

- Interpolation of data in error
- Attenuation
- Muting
- Finite impulse response transversal filtering with a four times increased sampling rate
- A digital audio output

Serial data formatted in two's complement (DAAB; pin 3) is clocked in by its bit clock (CLAB; pin 2) together with word select (WSAB; pin 1) and error flag (EFAB; pin 4) as shown in Fig. 1. After resynchronization with the internal clocks the data is separated into left and right channels and fed to two identical Input Shift Registers (IPSR). Internal timing and control loads the data into the interpolation RAM via the Intermediate Input Shift Register (IISR).

After interpolation, attenuation and muting the data is fed serially from the Intermediate Output Shift Register (IOSR) to the Audio Output Shift Register (AOSR) and to the IISR. From the IISR it is loaded into the filter RAM.

After filtering the data is passed to the Filter Data Shift Register (FDSR). From the FDSR it is transmitted serially to the data output (DABD; pin 15) together with the appropriate word select (WSBD; pin 18) and bit clock (CLBD; pin 16), in accordance with the I^2S bus specification. Data is again formatted in two's complement. Outputs DABD, WSBD and CLBD are strobed to maintain the correct timing relationship with the system clock output (XSYS) at pin 9 (see Fig. 12).

FUNCTIONAL DESCRIPTION (continued)

The subcode data (SDAB; pin 7) and 10-bit burst clock (SCAB; pin 6) are resynchronized to the internal clocks within the digital audio output block. SCAB clocks the data into the Subcode Input Shift Register (SISR; Fig. 2). Data is transferred to the Subcode Output Shift Register (SOSR) on receipt of all of the 10-bit burst clocks. The subcode data is then mixed with the data from the AOSR and the error flag to provide the output DOBM at pin 14. SISR is reset when no clocks are detected on the SCAB input.

Interpolation

When, for either left or right channel, unreliable samples are flagged between two correct samples, linear interpolation is used to replace the erroneous samples (up to a maximum of 8 consecutive errors).
When the error flag is set, the sample is replaced by a value calculated by the following formula:

$$S(n) = \frac{x}{x+1} \cdot S(n-1) + \frac{1}{x+1} \cdot S(n+x)$$

Where: $S(n)$ = new sample value
x = number of successive erroneous samples following $S(n-1)$
$S(n-1)$ = the preceding sample
$S(n+x)$ = the first following correct sample

The value of x is detected (1 to 8) to determine the coefficients for the multiplications. Eight coefficient pairs are stored in the ROM. If $x = 0$ or ≥ 9 then $S(n)$ will remain unchanged.

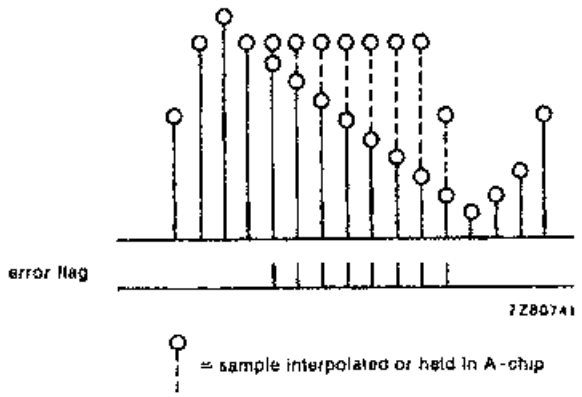


Fig. 4 Example of an eight sample linear interpolation.

Attenuation

Attenuation is controlled by the ATSB input at pin 22. When the input is active LOW the sample is multiplied by a coefficient that provides −12 dB attenuation. If the input is HIGH the multiplication factor is 1.

Mute

Mute is controlled by the MUSB input at pin 23. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. 32 coefficients are used to step down the value of the data, each one being used 31 times before stepping onto the next. When MUSB is released (pin 23 HIGH) the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order.

Filtering

The SAA7220 incorporates two identical finite impulse response transversal filters with the equivalent of 120 taps, one filter for each stereo channel. The corresponding 120 coefficients are structured as 4 sections of 30 coefficients.
(Each ROM contains only 60 filter coefficients, the same 60 being used a second time, but in the reverse order, to make a total of 120.)

Data is stored in a 480-bit RAM (30 words x 16 bits). The 30 words are sequentially addressed 4 times to generate the 4 output samples.

When a new word is moved from the interpolation RAM to the filter RAM, the oldest word is discarded and all other words moved one position with respect to the ROM coefficients. The data storage effectively forms a 30 sample wide moving window on the input data. The samples move within this window at 5,6448 MHz and the window moves one sample every 22,6 μs.

An output word is formed by multiplying 30 samples from the filter RAM with 30 coefficients from the ROM using a 16 x 12 array multiplier. The result is added in an accumulator. At the end of the 30 multiplications the 16 MSB's are passed from the accumulator via the IOSR to the FDSR, and the accumulator is reset. Overflow protection is incorporated so that the output always limits cleanly in the event of accumulator overflow. Also, to simplify the design of the digital-to-analogue converter a d.c. offset of + 5% is added to the accumulator.

The filtered data is output in the I²S format at a 5,6448 MHz bit rate and a sample rate of 176 kHz.

Digital audio output

The digital audio output (DOBM; pin 14) consists of 32-bit words transmitted in biphase-mark code. That is, two transitions for a logic 1 and one transition for a logic 0. The 32-bit words are transmitted in blocks of 384 words. Table 1 shows the information contained in each word.
The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns (B, M and W) indicate the following situations:

- Sync B; start of a block of 384 words, contains left sample (11101000)
- Sync M; word contains left sample, but is not a block start (11100010)
- Sync W; word contains right sample (11100100)

In the SAA7220 sync words are always preceded by 0.

Left and right samples are transmitted alternately.
Audio samples are available for digital audio output after interpolation, attenuation and muting, but before filtering.
Data held in the Subcode Output Shift Register (SOSR) is transmitted via the user data bit and is asynchronous with the block rate.

Digital audio output (continued)

Table 1 Composition of the 32-bit digital audio output word

bit number	description	information
1 to 4	sync	—
5 to 8	auxiliary	not used (always zero)
9 to 28	audio sample	bits 9 to 12 not used (always zero), bits 13 (LSB) to 28 (MSB) two's complement
29	audio valid	copy of the error flag
30	user data	used for subcode data
31	channel status	indication of control bits and category code
32	parity bit	even parity for all word bits excluding sync pattern

Channel status

The channel status bit is the same for both left and right words. Therefore a block of 384 words contains 192 channel status bits as shown in Table 2.

When there is no subcode the channel status will switch over to the general format. 'No subcode' is identified by the subcode detector when SCAB is a continuous HIGH or LOW.

Table 2 Channel status bit assignment

bit number	description	subcode provided	no subcode provided
1 to 4	control	copy of Q channel	bits 1 and 2 zero bit 3 image of SCAB bit 4 image of SDAB
5 to 8	reserved	always zero	always zero
9 to 16	category code	CD category bit 9 logic 1	general category all bits zero
17 to 192		always zero	always zero

If a subcode clock is provided but there is no subcode data (SDAB is a continuous HIGH or LOW) the control bits will be zero and the category code will be CD.

The SYNC bit and the cyclic redundancy check bit (CRC) in the subcode data from the A-chip to the B-chip have the format shown by Fig. 5. Typical subcode data output waveforms are shown by Fig. 8.

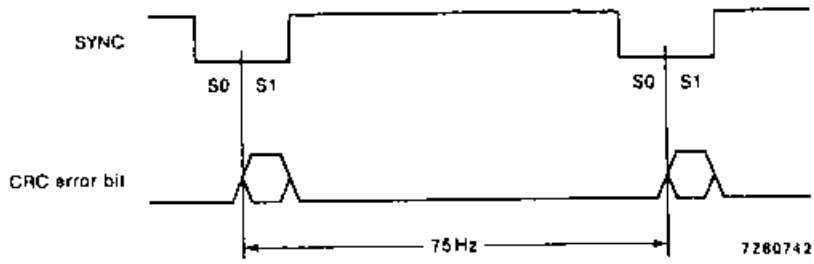


Fig. 5 Subcode data format for SYNC and CRC bits.

SYNC is active LOW and indicates the start of a subcode block, which contains 98 words including 2 sync words, S0 and S1.
CRC is always LOW except during SYNC S1 when:

- CRC = logic 1; previous Q block was true
- CRC = logic 0; previous Q block was false

Two 32-bit words are transmitted at the sample frequency of 44,1 kHz (2 x 32 x 44,1 kHz = 2,8224 Mbits/s data rate). An internal 5,6448 MHz clock (XSYS/2) is used in the biphase modulator.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 24)	V_{DD}	−0,5 to + 7,0 V
Maximum input voltage range	V_I	−0,5 to V_{DD} + 0,5 V
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Electrostatic handling*	V_{es}	−1000 to + 1000 V

All outputs are short-circuit protected except the crystal oscillator output.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 24)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)	I_{DD}	–	180	–	mA
Inputs					
WSAB, DAAB					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	I_{LI}	−10	0	+ 10	µA
Input capacitance	C_I	–	–	7	pF
EFAB, SDAB (note 1)					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	µA
at V_I = V_{DD}	I_{LI}	–	–	+ 50	µA
Input capacitance	C_I	–	–	7	pF
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$ (note 2)					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−30	–	–	µA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	µA
Input capacitance	C_I	–	–	7	pF
Crystal oscillator (see Fig. 10)					
Input XIN					
Output XOUT					
Mutual conductance at 100 kHz	G_m	1,5	–	–	mA/V
Small signal voltage gain ($A_V = G_m \times R_O$)	A_V	3,5	–	–	V/V
Input capacitance	C_I	–	–	10	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Output capacitance	C_O	–	–	10	pF
Input leakage current	I_{LI}	−10	0	+ 10	µA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Slave clock mode					
Input voltage (note 3) (peak-to-peak value)	$V_{I(p-p)}$	1,6	–	V_{DD} + 0,5	V
Input voltage LOW (note 4)	V_{IL}	0	–	1	V
Input voltage HIGH (note 4)	V_{IH}	2,4	–	V_{DD} + 0,5	V
Input rise time (note 5)	t_r	–	–	20	ns
Input fall time (note 5)	t_f	–	–	20	ns
Input HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%
Outputs					
DABD, CLBD, WSBD					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
XSYS (note 6)					
Output voltage LOW	V_{OL}	0	–	0,4	V
Output voltage HIGH	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
DOBM					
Voltage across a 75 Ω load via attenuator; see Fig. 10 (peak-to-peak value)	$V_{L(p-p)}$	0,4	–	0,6	V
TIMING					
Operating frequency (XTAL)	f_{XTAL}	10,16	11,2896	12,42	MHz
Inputs (see Fig. 11)					
SCAB, CLAB (note 7)					
SCAB clock frequency (burst clock)	f_{SCAB}	–	2,8224	–	MHz
CLAB clock frequency	f_{CLAB}	–	2,8224	–	MHz
or (note 8)	f_{CLAB}	–	1,4112	–	MHz
Clock LOW time	t_{CKL}	110	–	–	ns
Clock HIGH time	t_{CKH}	110	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DAAB, WSAB, EFAB (note 9)					
Data set-up time	$t_{SU;DAT}$	40	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
SDAB (note 10)					
Subcode data set-up time	$t_{SU;SDAT}$	40	–	–	ns
Subcode data hold time	$t_{HD;SDAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
Outputs (see Fig. 12)					
WSBD (notes 7 and 11)					
Word select set-up time	$t_{SU;WS}$	40	–	–	ns
Word select hold time	$t_{HD;WS}$	0	–	–	ns
WSBD (note 7)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 7 and 11)					
Data set-up time	$t_{SU;DATD}$	40	–	–	ns
Data hold time	$t_{HD;DATD}$	0	–	–	ns
DABD (note 7)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
CLBD (notes 7 and 11)					
Clock period	t_{CK}	161	177	197	ns
Clock LOW time	t_{CKL}	65	–	–	ns
Clock HIGH time	t_{CKH}	65	–	–	ns
Clock set-up time	$t_{SU;CLD}$	40	–	–	ns
Clock hold time	$t_{HD;CLD}$	0	–	–	ns
CLBD (note 7)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 7 and 12)					
Data set-up time	$t_{SU;DATBD}$	40	–	–	ns
Data hold time	$t_{HD;DATBD}$	60	–	–	ns

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
WSBD (notes 7 and 12)					
Word select set-up time	$t_{SU;DATWSD}$	40	–	–	ns
Word select hold time	$t_{HD;DATWSD}$	60	–	–	ns
DOBM (note 13)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
Data bit 0					
pulse width HIGH	$t_{HIGH(0)}$	–	354	–	ns
pulse width LOW	$t_{LOW(0)}$	–	354	–	ns
Data bit 1					
pulse width HIGH	$t_{HIGH(1)}$	–	177	–	ns
pulse width LOW	$t_{LOW(1)}$	–	177	–	ns
XSVS					
Output rise time (note 7)	t_r	–	–	20	ns
Output fall time (note 7)	t_f	–	–	20	ns
Output HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%

DEVELOPMENT DATA

Notes to the characteristics

1. Inputs EFAB and SDAB both have internal pull-downs.
2. Inputs CLAB, SCAB, $\overline{ATSB}$ and $\overline{MUSB}$ have internal pull-ups.
3. I_6 used in a.c. coupled mode.
4. $V_{IH} - V_{IL} \geqslant 1{,}6$ V.
5. Reference levels = 2,4 V.
6. The output current conditions are dependent on the drive conditions.
   When a crystal oscillator is being used the output current capability is I_{OL} = + 1,6 mA; I_{OH} = −0,2 mA; But if a slave input is being used the output currents are reduced to I_{OL} = +0,2 mA; I_{OH} = −0,2 mA.
7. Reference levels = 0,8 V and 2,0 V.
8. The signal CLAB can run at either 2,8 MHz (1/4 system clock) or 1,4 MHz (1/8 system clock) under typical conditions. If does not have a minimum or maximum frequency, but is limited to being 1/4 or 1/8 of the system clock frequency.
9. Input set-up and hold times measured with respect to clock input from A-chip (CLAB). Reference levels = 0,8 V and 2,0 V.
10. Input set-up and hold times measured with respect to subcode burst clock input from A-chip (SCAB). Reference levels = 0,8 V and 2,0 V.
11. Output set-up and hold times measured with respect to system clock output (XSYS).
12. Output set-up and hold times measured with respect to clock output (CL8D).
13. Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level.

DEVELOPMENT DATA

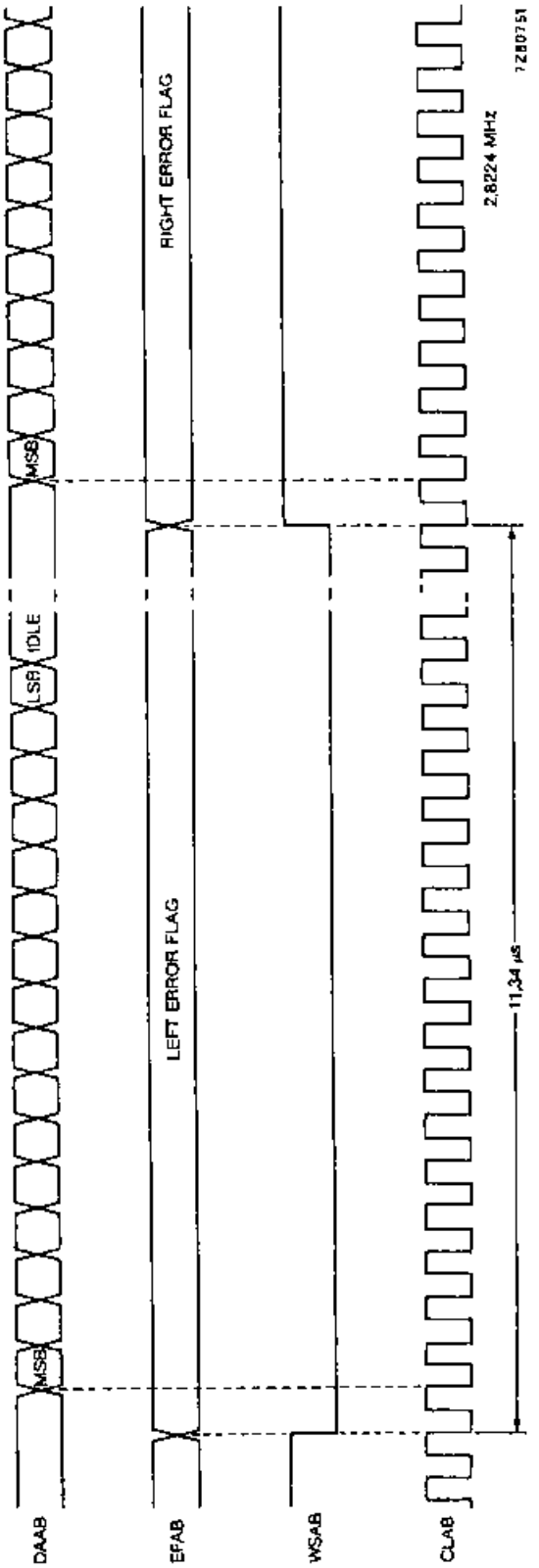


Fig. 6a Typical sample data input waveforms from A-chip (2,8 MHz).

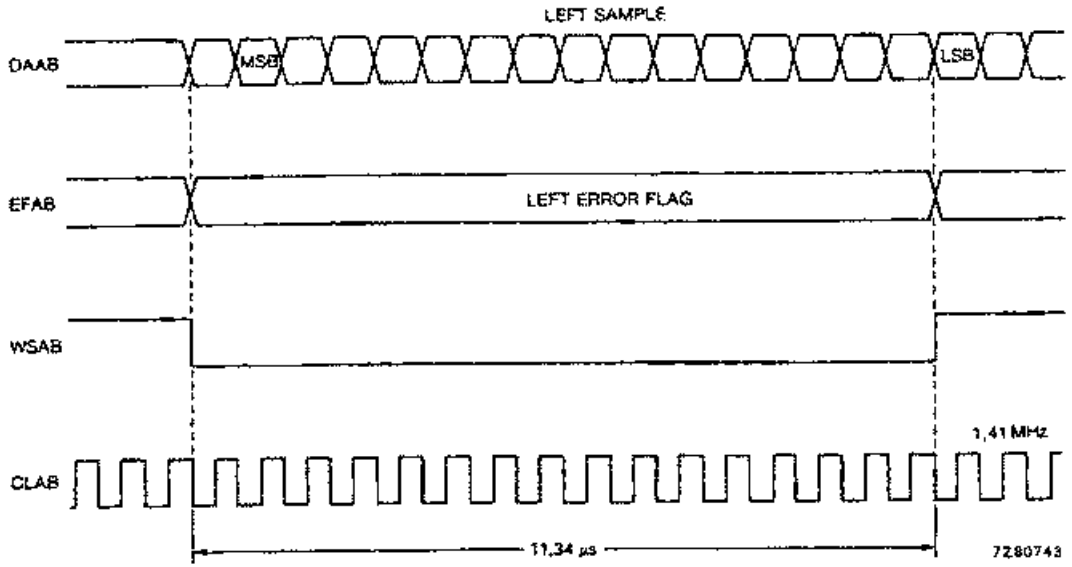


Fig. 6b Typical sample data input waveforms from A-chip (1,4 MHz).

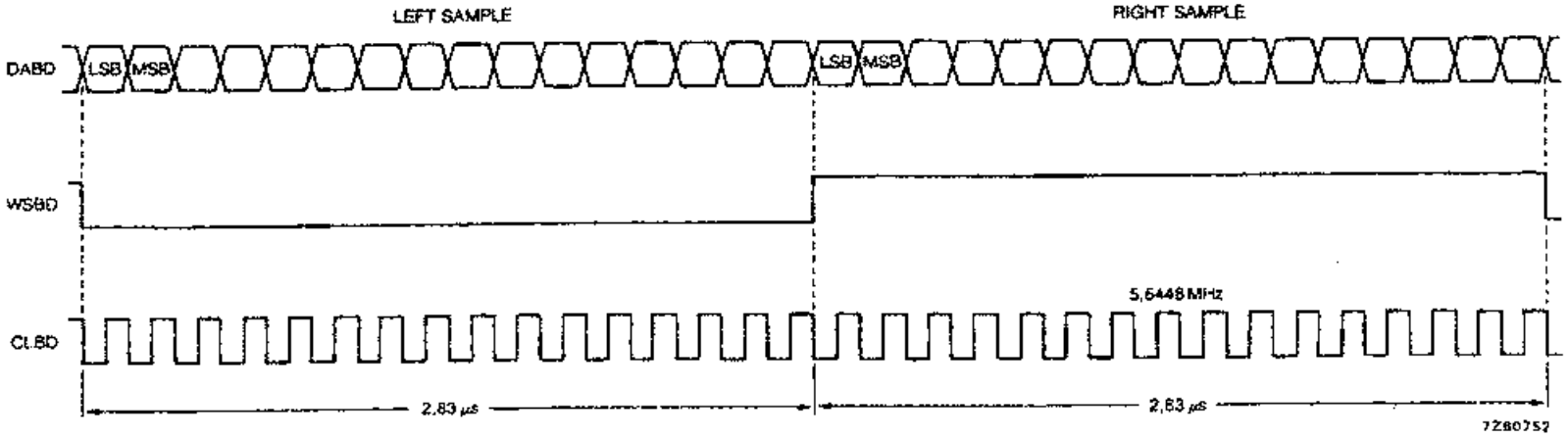
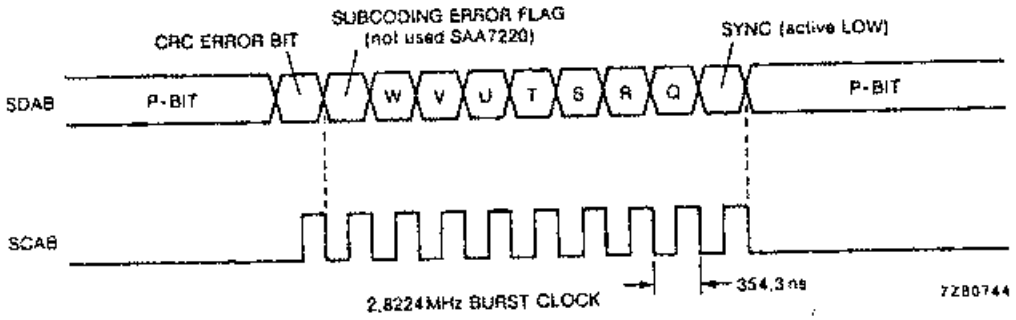


Fig. 7 Typical sample data output waveforms to DAC.



Subcode word frequency = 7,35 kHz.

Fig. 8 Typical subcode data input waveforms.

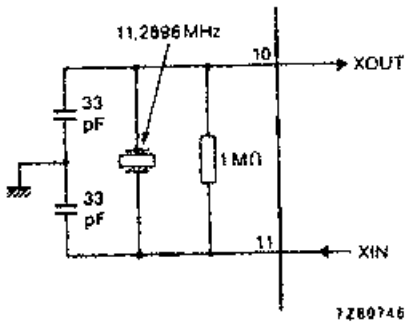


Fig. 9 Crystal oscillator circuit.

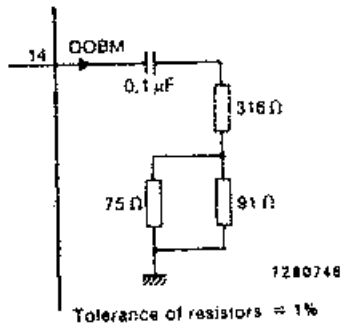


Fig. 10 Digital audio output load.

TIMING

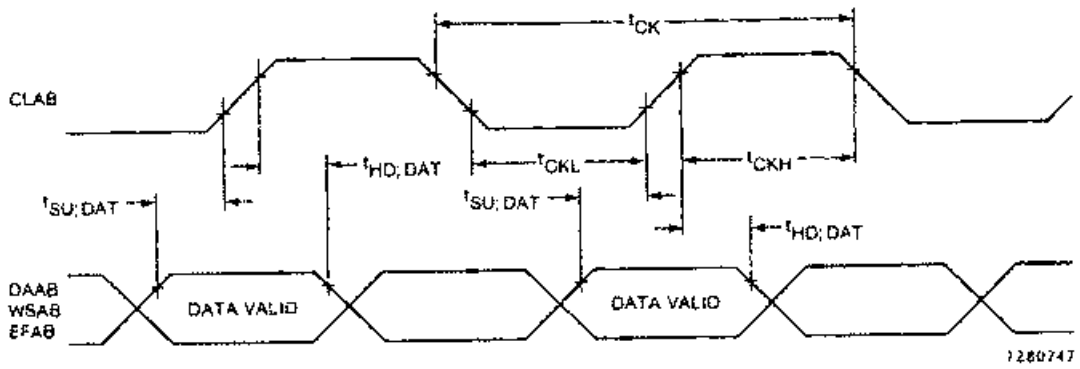


Fig. 11 Data input timings: reference levels = 0,8 V and 2,0 V.
(also applicable to subcode data input ($t_{SU;SDAT}$ and $t_{HD;SDAT}$).

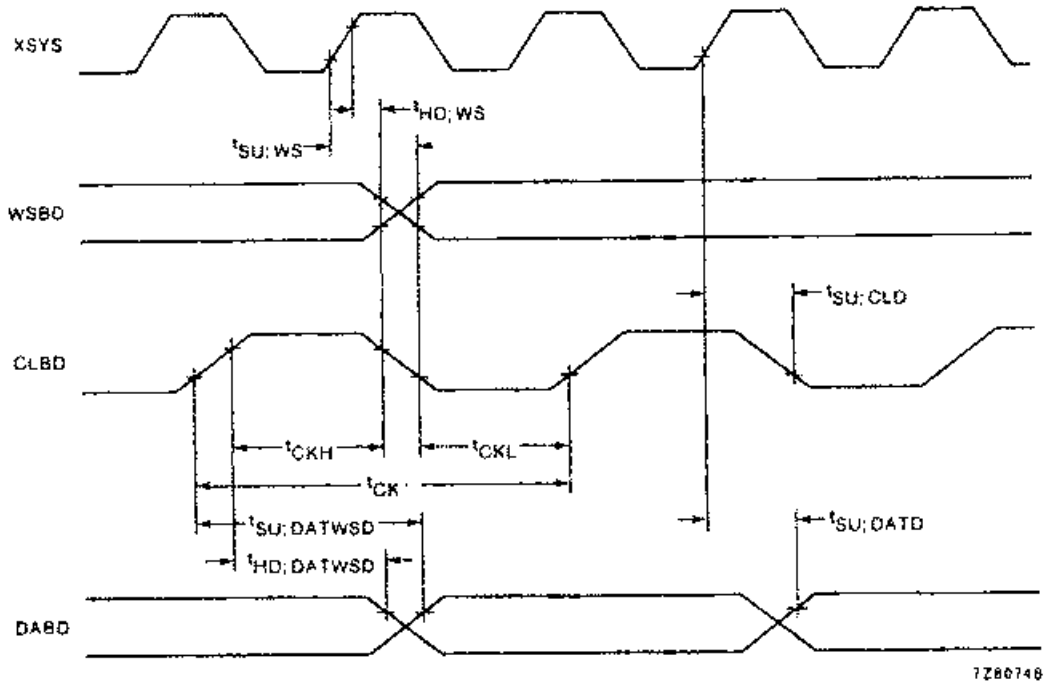


Fig. 12 Data output timings; reference levels = 0,8 V and 2,0 V.

DEVELOPMENT DATA

APPLICATION INFORMATION

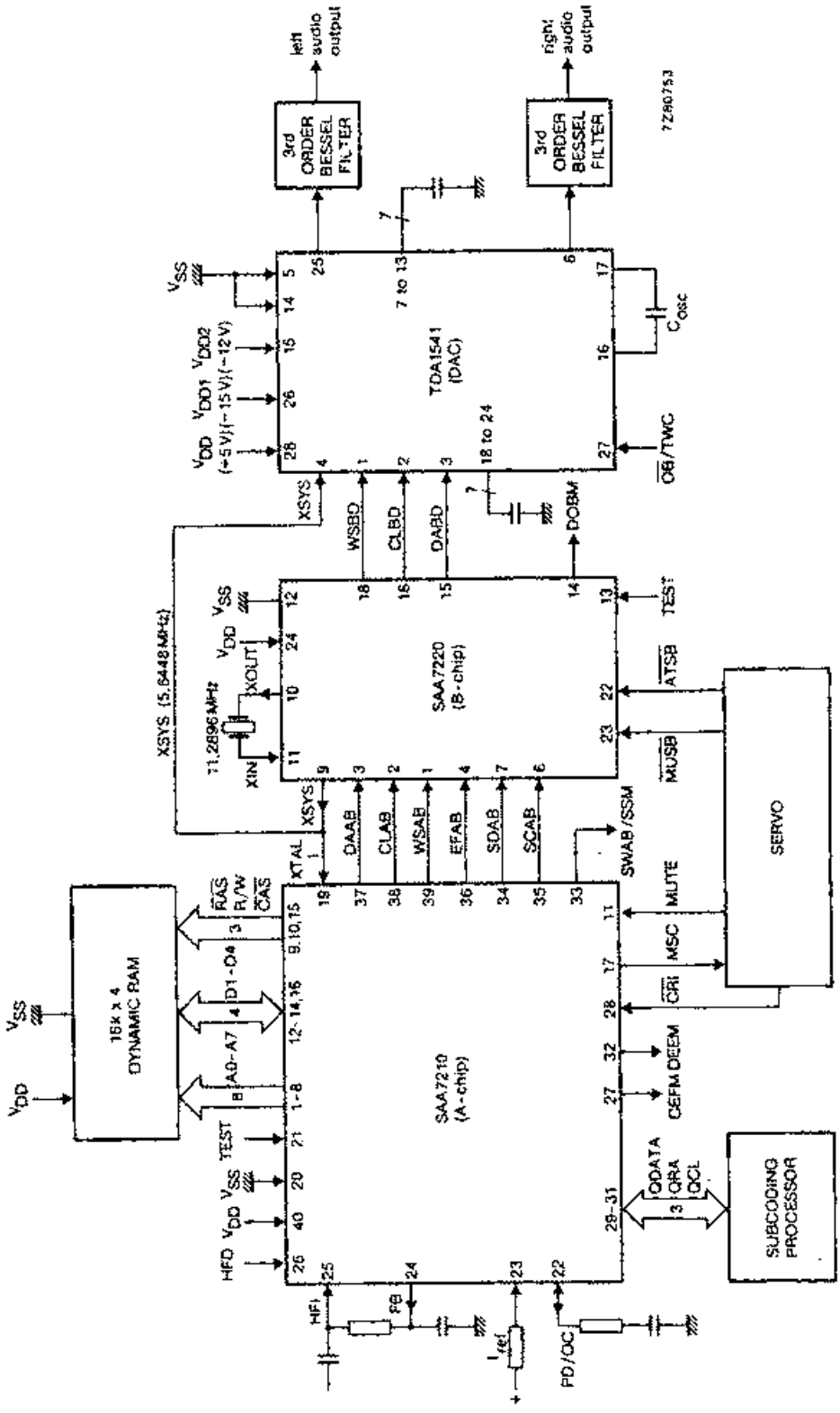
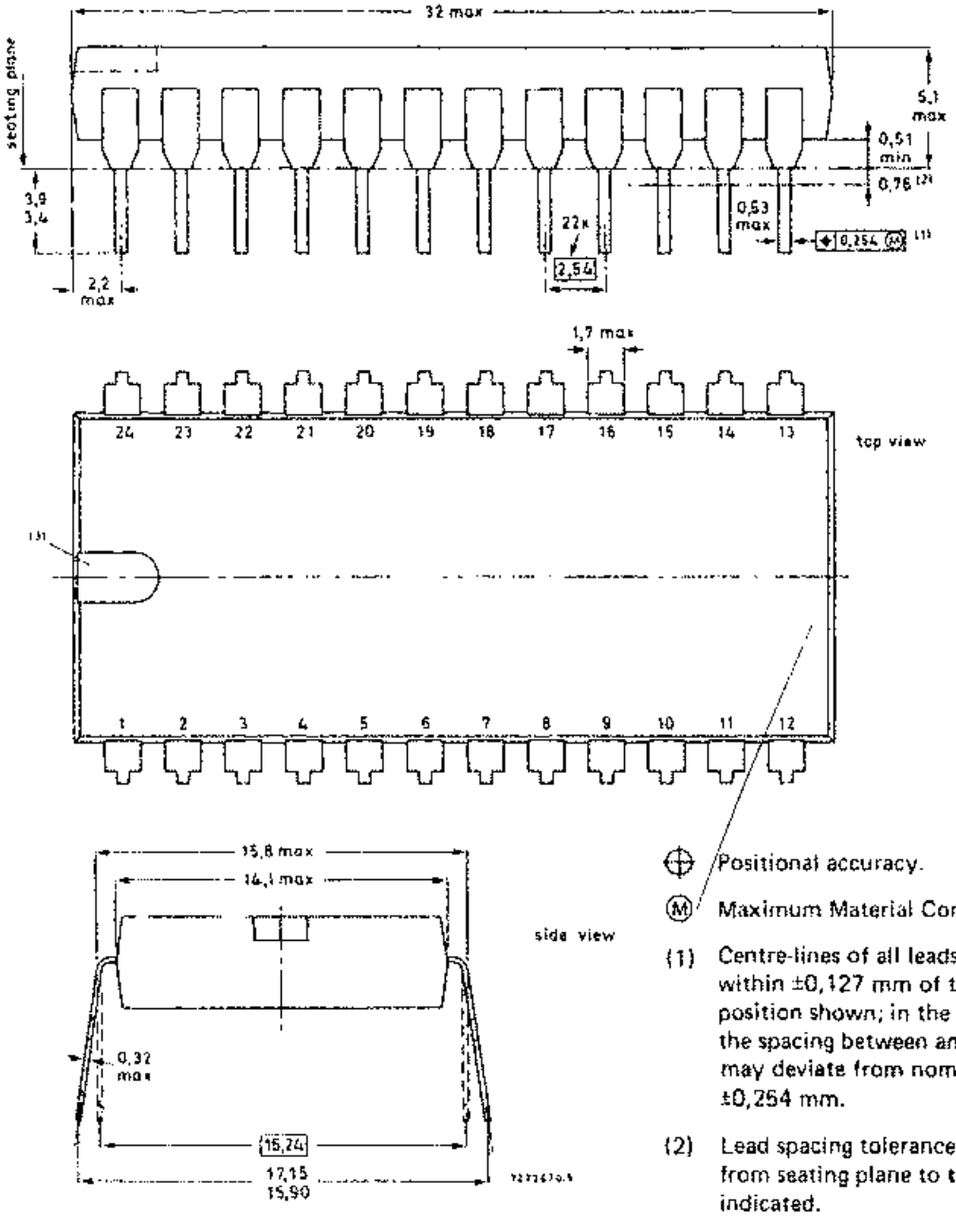


Fig. 13 System application diagram.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm