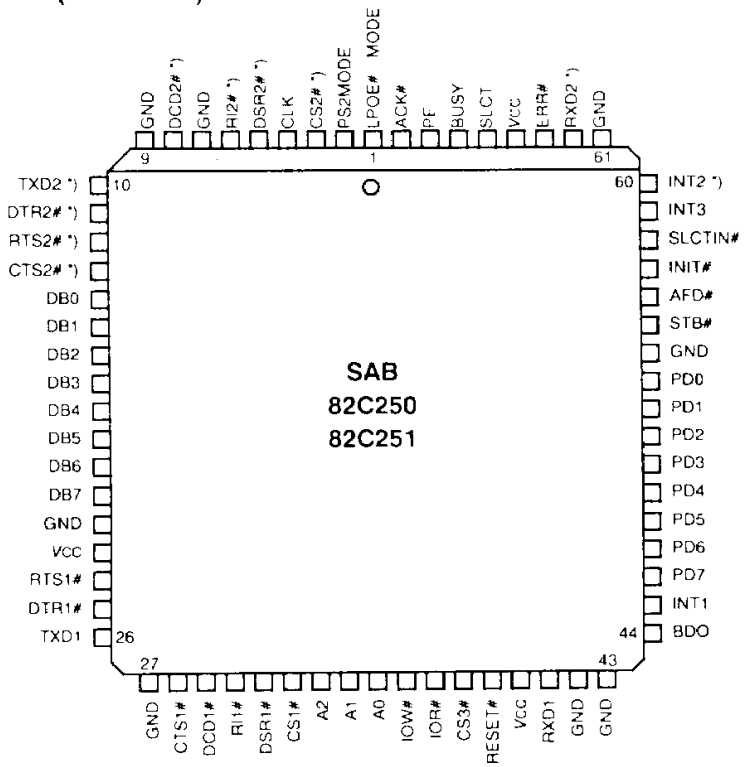
SAB 82C250/SAB 82C251
Advanced Peripheral Interface Controller

Advance Information

- SAB 82C250: Dual channel asynchronous serial controller
- SAB 82C251: One channel asynchronous serial controller
- Implementation of the standard PC-XT™ AT™ PS/2™ application
- SAB 16C450 compatible serial controller with improved 16550 AC characteristics
- 8-bit bi-directional parallel port
- Supports fully Centronics printer interface with bi-directional function (16C452 16C451-compatible mode)
- PS/2 register compatible mode for bi-directional parallel port
- Fully programmable serial interface characteristics for each serial channel
  - 5/6/7/8-bit character length
  - Parity generation and detection
  - Error reporting capabilities
  - Common external clock input for the baud rate generators
  - Baud rate up to 512 KBaud
- Mode selection by pin strapping
- I_{OL} I_{OH} for printer data pins: 24 mA -15 mA
- CMOS implementation for high speed and low power requirements
- 68-pin plastic leaded chip carrier package (PL-CC-68)

Figure 1
Pin Configuration (PL-CC-68)



*) These pins are not connected (N.C.) at the SAB 82C251

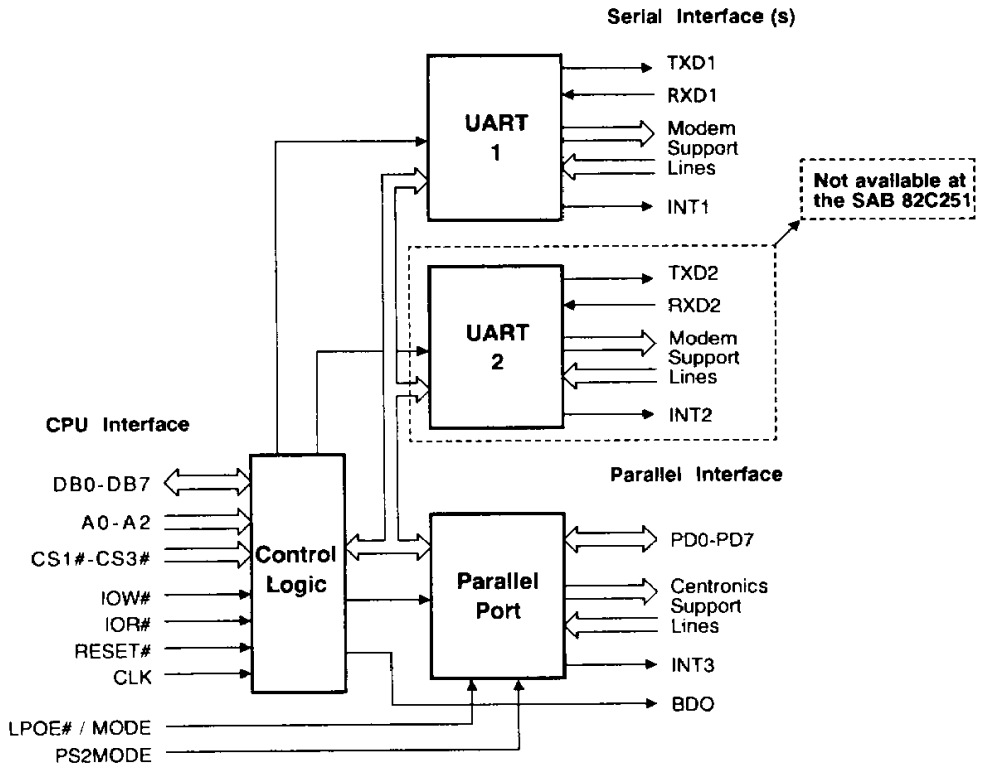
General Information

The SAB 82C250/82C251 are advanced serial/parallel interface controllers for standard and IBM PC-XT™/PC-AT™/PS/2™ compatible interface applications. Their serial channels provide the functionality of the SAB 16C450 universal asynchronous receiver/transmitter. Only one serial channel is available in the SAB 82C251.

The SAB 82C250/82C251 also provide a parallel port, which fully supports the standard Centronics printer interface, as well as the bi-directional feature of the PS/2 parallel port implementation. This feature allows full PS/2 register compatible bi-directional input/output operations in the parallel port.

The SAB 82C250/82C251 are fabricated in Siemens AC-MOS technology and are available in the 68-pin plastic-leaded-chip-carrier (PL-CC-68) package. The SAB 82C250/82C251 are compatible to the standard 16C452/16C451 serial-parallel controllers.

Figure 2
Block Diagram



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Bus Interface			
CLK	4	I	**Serial Clock:** External clock input to the baud rate generator(s) of the serial channel(s).
DB0-DB7	14-21	I/O	**Data Bus 0-7:** The data bus provides 8 bi-directional IO-lines for the transfer of data, status and control information between the SAB 82C250/82C251 and the CPU. These lines are inputs except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0-A2	35-33	I	**Address lines 0-2:** The address lines are used together with the chip select inputs to select the internal registers of the SAB 82C250/82C251.
IOW#	36	I	**IO Write Strobe#:** This is an active low input which causes the data at the data bus to be written into the selected registers of the SAB 82C250/82C251. The destination of the data depends on the state of CS1#, CS2#, CS3# and A0–A2.
IOR#	37	I	**IO Read Strobe#:** This is an active low input which causes the selected IO-device to output data to the data bus DB0-DB7. The source of the data depends on the state of CS1#, CS2#, CS3# and A0-A2.
RESET#	39	I	**RESET#:** With RESET# = low the two serial ports and the parallel port are put into an initial state.
BDO	44	O	**Bus Buffer Output:** This line goes high whenever either serial channel registers or the parallel port registers are read. This output can be used to control system bus drivers.
V_{CC}	23,40, 64	–	**Power Supply (+ 5 V)**
GND	7, 9, 22, 27, 42, 43, 54, 61	–	**Ground (0 V)**

Pin Definitions and Functions (continued)

Symbol	Pin 1)	Input (I) Output (O)	Function
Serial Interface			
RTS1# RTS2#	24 12	O	**Request To Send#**: When active (low), the UART indicates that data is ready to be transmitted. The RTS# pins are set low by writing a 1 to the appropriate bits of the modem control registers.
DTR1# DTR2#	25 11	O	**Data Terminal Ready#**: When active (low), the UART indicates that it is ready to receive data. The RTS# pins are set low by writing a 1 to the appropriate bits of the modem control registers.
TXD1 TXD2	26 10	O	**Serial Data Outputs**: These lines are the serial data outputs from the UARTs transmitter circuitry.
CTS1# CTS2#	28 13	I	**Clear To Send#**: The states of these pins are reflected in bits of the modem control registers. When CTS# = low, data can be transmitted at the TXD lines.
DCD1# DCD2#	29 8	I	**Data Carrier Detect#**: The states of these pins are reflected in bits of the modem control registers. DCD# = low indicates that the data carrier has been detected by the modem.
RI1# RI2#	30 6	I	**Ring Indicator#**: The states of these pins are reflected in bits of the modem control registers. When low, RI# = low indicates that a telephone ringing signal has been received by the modem.
DSR1# DSR2#	31 5	I	**Data Set Ready#**: The states of these pins are reflected in bits of the modem control registers. When DSR# = low, a modem is indicating that it is ready to exchange data with the associated UART.
CS1# CS2#	32 3	I	**Serial Channel Chip Select#**: CS1# and CS2# are the enable lines for the read and write control signals of the SAB 82C250/82C251 serial channels. Only one of the 3 chip select inputs may be active at a time!

1) All signals with extension "2" are not available at the SAB 82C251. The corresponding pins are not connected (N.C.) at the SAB 82C251.

Pin Definitions and Functions (continued)

Symbol	Pin [1]	Input (I) Output (O)	Function
Serial Interface			
RXD1 RXD2	41 62	I	**Serial Data Input:** These lines are the serial data inputs to the SAB 82C250/82C251 serial channels receiver circuitry.
INT1 INT2	45 60	O	**Serial Channel Interrupts:** These tristate outputs are enabled by the modem control register bits 2. An occurring interrupt condition of the serial channels will activate (set high) these interrupt lines. The interrupts are reset (low) upon an appropriate service or a reset.
Parallel Interface			
LPOE# /MODE	1	I	**Printer Output Enable#/Mode Select:** In normal mode (PS2MODE = low) this input signal enables the PD0–PD7 outputs. With PS2MODE = high, this input selects between the uni- and bi-directional printer port operation.
PS2MODE	2	I	**Enable Printer PS/2 Mode:** With high at this input, the PS/2 mode of the printer interface is selected. A low level selects normal Centronics compatible mode operation of the parallel interface.
CS3#	38	I	**Parallel Port Chip Select#:** CS3# = low enables the read and write control lines of the SAB 82C250/ 82C251 parallel port section. Only one of the 3 chips select inputs may be active at a time!
PD0–PD7	53–46	I/O	**Parallel Data Bits (0–7):** These lines provide the byte-wide input or output port of the SAB 82C250/ 82C251.
STB#	55	O	**Line Printer Strobe#:** When low, this line provides the line printer with a signal to latch data which is currently available at the parallel port.

1) All signals with extension "2" are not available at the SAB 82C251. The corresponding pins are not connected (N.C.) at the SAB 82C251.

Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
Parallel Interface			
AFD#	56	O	**Line Printer Autofeed#**: With AFD# = low the printer does a continous form feed of the paper.
INIT#	57	O	**Line Printer Initialize**: This signal (low) causes the printer to start its initialization routine.
SLCTIN#	58	O	**Line Printer Select#**: When active (low), this line selects the line printer.
INT3	59	O	**Interrupt Printer Port**: This interrupt output is activated (high) by a low ACK# signal. The function of INT3 is controlled by bit 4 of the parallel port control register.
ERR#	63	I	**Line Printer Error#**: If this input goes low, the line printer reports an error condition.
SLCT	65	I	**Line Printer Select**: This is an input line from the line printer that goes high when the printer has been selected.
BUSY	66	I	**Line Printer Busy**: This is an input line from the line printer that goes high when the printer has a local operation in progress.
PE	67	I	**Line Printer Paper Empty**: This is an input line from the line printer that goes high when the printer runs out of paper.
ACK#	68	I	**Line Printer Acknowledge**: This input goes low if a successful data transfer has occurred.

Serial Channel Description

The SAB 82C250 contains two serial channels. In the SAB 82C251, the second serial channel of the SAB 82C250 is not available. In the following text, no number extensions are used when referring to the signal names. In the SAB 82C250/82C251 the number extension "1" refers to serial channel 1. In the SAB 82C250 the number extension "2" refers to serial channel 2.

Serial Port Register Addressing

When CS1# is low, registers for serial channel 0 can be accessed, and when CS2# is low, registers for serial channel 1 can be accessed. No more than one chip select line should ever be low at a time (invalid condition). Address lines A0, A1 and A2 are used to select the appropriate register of the serial channels (Table 1). The Divisor Latch Access Bit (DLAB) in table 1 is the MSB of the Line Control Register. DLAB must be set by software to access the baud rate generator divisor latches.

Table 1
Serial Channel Register Addressing

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer Register (RBR, read) Transmitter Holding Register (THR, read)
0	0	0	1	Interrupt Enable Register (IER)
X	0	1	0	Interrupt Identification Register (IIR, read only)
X	0	1	1	Line Control Register (LCR)
X	1	0	0	Modem Control Register (MCR)
X	1	0	1	Line Status Register (LSR)
X	1	1	0	Modem Status Register (MSR)
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Register Description

Three types of internal registers are used in the serial channels of the SAB 82C250/82C251: control, status and data registers. The control registers are two divisor latches for the baud rate generator, the Line Control Register (LCR), the Interrupt Enable Register (IER), and the Modem Control Register (MCR). Two status registers are available: Line Status Register (LSR) and Modem Status Register (MSR).
The data registers are the Receiver Buffer Register (RBR), for read operations, and the Transmitter Holding Register (THR), for write operations. Table 2 shows the contents of the SAB 82C250/82C251 serial channel registers in detail.

Receiver/Transmitter Buffer Register

The Receiver Buffer Register and the Transmitter Buffer Register are data registers, which hold between five and eight bits of data. If less than eight data bits are transmitted, then the data will be right justified to the LSB. Bit 0 of a data byte is always the first serial data bit received and transmitted. The SAB 82C250/82C251 serial channel data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the serial-to-parallel and parallel-to-serial conversion.

Table 2
Summary of Registers

	Register Address				
	0 (DLAB = 0)	**0 (DLAB = 0)**	**1 (DLAB = 0)**	**2**	**3**
Bit no.	Receiver Buffer Register (read only)	Transmitter Holding Register (write only)	Interrupt Enable Register	Interrupt Identification Register (read only)	Line Control Register
	RBR	THR	IER	IIR	LCR
0	Data bit 0 [1]	Data bit 0 [1]	Received data available (RDI)	"0" if interrupt is pending (IP)	Word length select bit 0 (WSL0)
1	Data bit 1	Data bit 1	Transmitter holding register empty (THI)	Interrupt ID bit 0 (IIB0)	Word length select bit 1 (WLS1)
2	Data bit 2	Data bit 2	Receiver line status (RSI)	Interrupt ID bit 1 (IIB1)	Number of stop bits (STB)
3	Data bit 3	Data bit 3	Modem status (MSI)	0	Parity enable (PEN)
4	Data bit 4	Data bit 4	0	0	Even parity select (EPS)
5	Data bit 5	Data bit 5	0	0	Stick parity
6	Data bit 6	Data bit 6	0	0	Set break
7	Data bit 7	Data bit 7	0	0	Divisor latch access bit (DLAB)

1) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

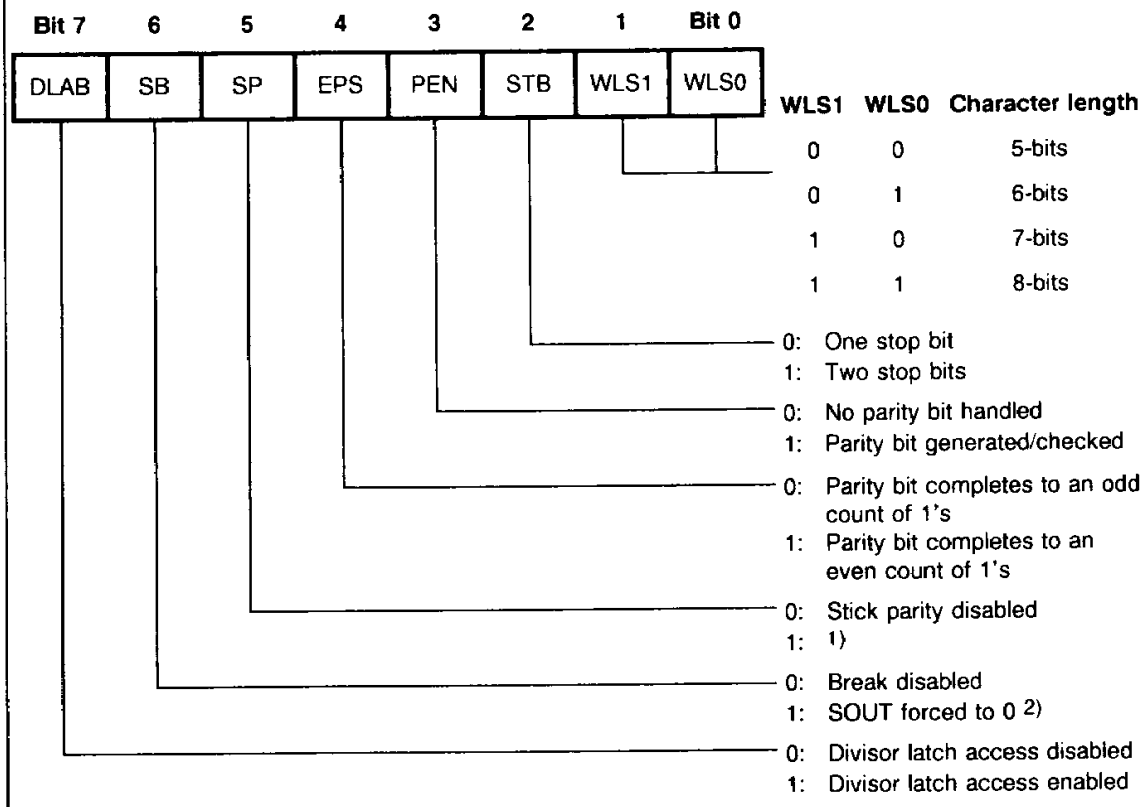
Table 2
Summary of Registers (continued)

	Register Address					
	4	**5**	**6**	**7**	**0 (DLAB = 1)**	**1 (DLAB = 1)**
Bit no.	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	MCR	LSR	MSR	SCR	DLL	DLM
0	Data terminal ready (DTR)	Data ready (DR)	Delta clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to send (RTS)	Overrun error (OE)	Delta data set ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity error (PE)	Trailing edge ring indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt Output Enable (IOE)	Framing error (FE)	Delta data carrier detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Loop (LOOP)	Break interrupt (BI)	Clear to send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter holding register (THRE)	Data set ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter empty (TEMT)	Ring indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	0	Data carrier detect (DCD)	Bit 7	Bit 7	Bit 15

Line Control Register (LCR)

The format of the asynchronous data communication exchange and the access to the divisor latch is controlled via the line control register.

Figure 3
Line Control Register



1) This bit is the stick parity bit. When bits 3, 4 and 5 are logic 1, the parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0 then the parity bit is transmitted and checked as a logic 1.

2) This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

   1. Load an all O's pad character in response to THRE.
   2. Set break after the next THRE.
   3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission is to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.

Programmable Baud Rate Generator

The serial channels of the SAB 82C250/82C251 contain a programmable baud rate generator, which is capable of taking any clock input from DC to 8.0 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the baud rate generator is 16 x the baud rate.

$$\text{Divisor} = \frac{\text{Input frequency at CLK}}{\text{Desired baud rate} \times 16}$$

Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. By loading one of the divisor latches, the 16-bit baud rate counter is immediately loaded. Tables 3, 4 and 5 provide decimal divisors to use with CLK clock frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. The maximum operating frequency of the baud rate generator is 8.0 MHz. In this case, the data rate can be 512 K baud maximum.

Table 3
Baud Rates Using 1.8432 MHz Clock

Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2 [1]	2.86

[1] Smallest allowable divisor when using corresponding clock.

Table 4
Baud Rates Using 3.072 MHz Clock

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–
56000	3 [1]	14.285

Table 5
Baud Rates Using 8 MHz Clock

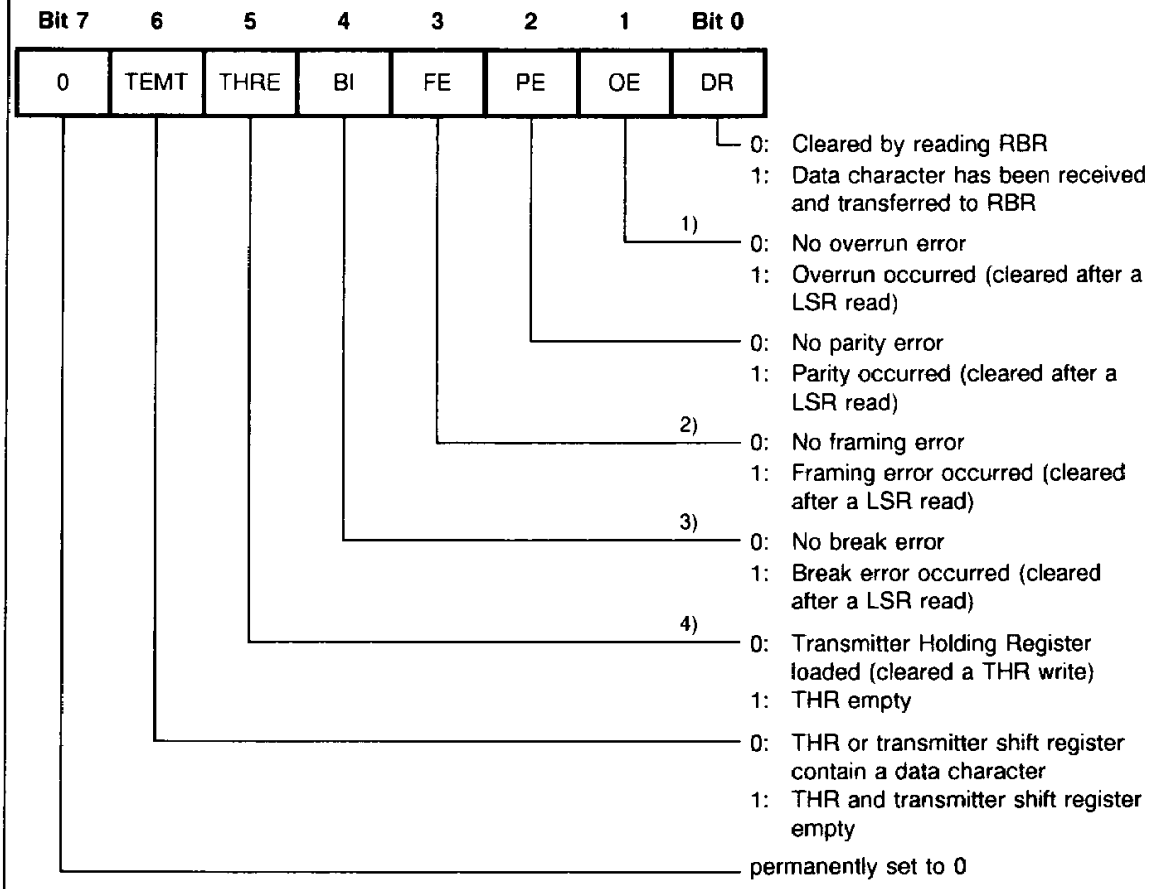
Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1 [1]	2.344

[1] Smallest allowable divisor when using corresponding clock.

Line Status Register (LSR)

This 8-bit register provides the CPU with status information concerning the data transfer.

Figure 4
Line Status Register



Bits 1 through 4 of LSR are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

1) This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the CPU before the transfer of the next character into the receiver buffer register, thus destroying the previous character.

2) The UART will try to resynchronize after a framing error. Therefore, it assumes that the framing error was due to the next start bit, samples this "start" bit twice and then takes in the "data".

3) This bit is the break interrupt (BI) indicator. BI is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (i.e., the total time of start bit + data bits + parity + stop bits).
Restarting after a break is received requires the RXD pin to be logic 1 for at least $\frac{1}{2}$-bit time.

4) Three indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the transmitter holding register empty interrupt enable is set high.

Interrupt Identification Register (IIR)

The UARTs of the SAB 82C250/82C251 have interrupt capabilities that allow interfacing to all popular microprocessors presently available.

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt identification register. The four levels of interrupt conditions in order of priority are: receiver line status, received data ready, transmitter holding register empty and modem status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Figure 5 shows the contents of the IIR.

Figure 5
Interrupt Identification Register

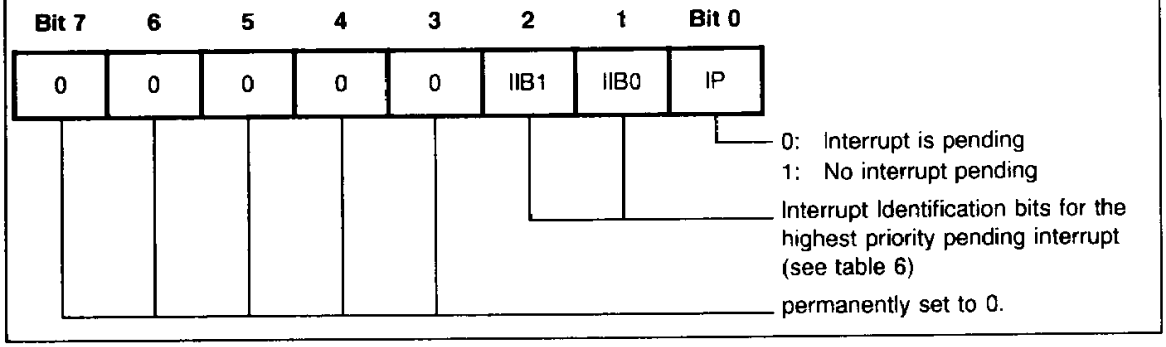


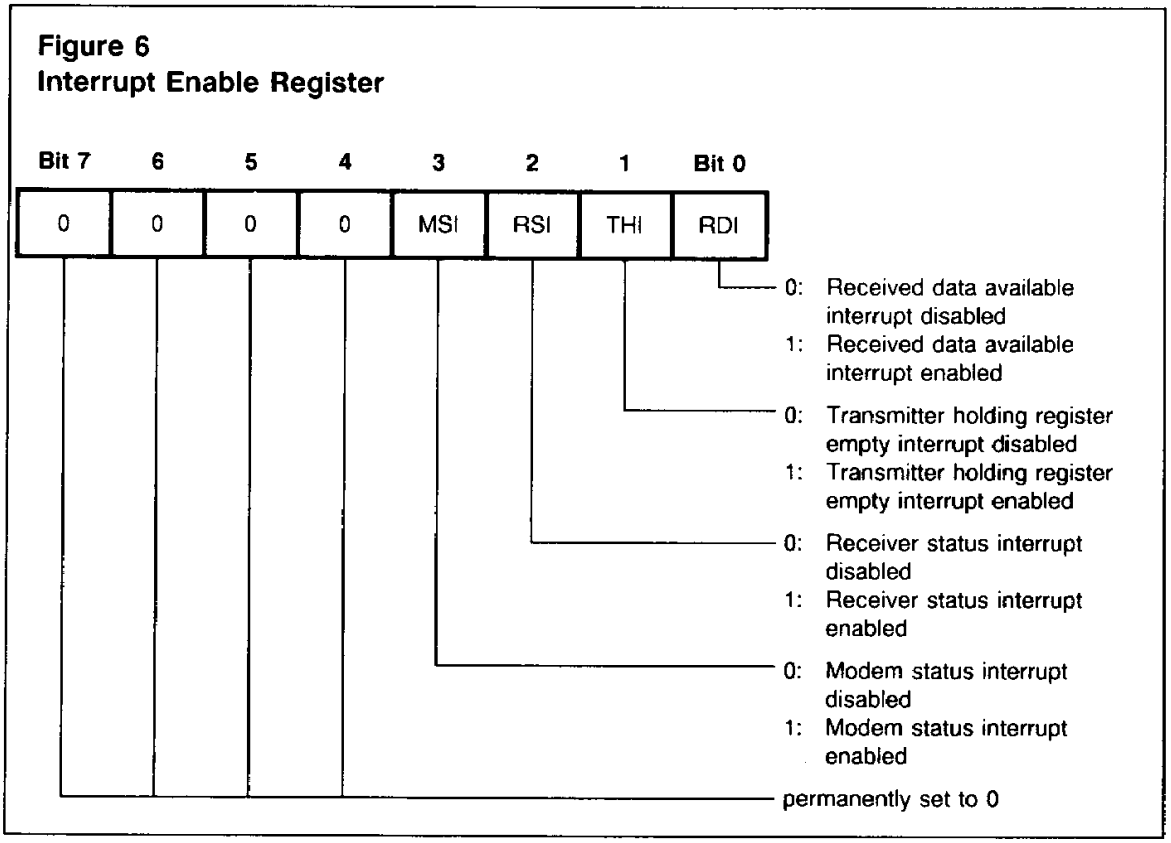
Table 6
Interrupt Control Functions

Interrupt identification register				Interrupt set and reset functions		
IIB1	IIB0	IP	Priority level	Interrupt type	Interrupt source	Interrupt reset control
0	0	1	–	None	None	–
1	1	0	Highest	Receiver line status	Overrun error or parity error or framing error or break interrupt	Reading the line status register
1	0	0	Second	Received data available	Receive data available	Reading the receiver buffer register
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading the IIR register (if source of interrupt) or Writing into the transmitter holding register
0	0	0	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect	Reading the modem status register

Interrupt Enable Register (IER)

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INT1/INT2) output signals. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, setting bits of this register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INT1/INT2 output signals. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. Figure 6 shows the contents of the IER.

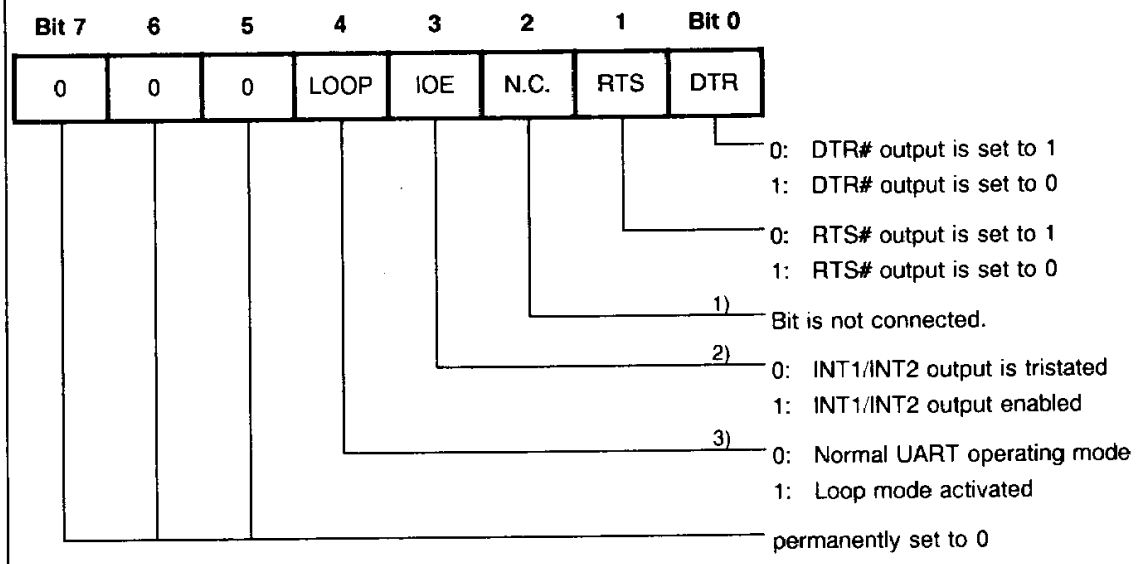
Figure 6
Interrupt Enable Register



Modem Control Register (MCR)

This register controls the interface to the Modem or data set (or a peripheral device emulating a Modem). The contents of the Modem control register are described in figure 7.

Figure 7
Modem Control Register



1) In loop mode this bit is equivalent to the MSR bit 6 (RI).

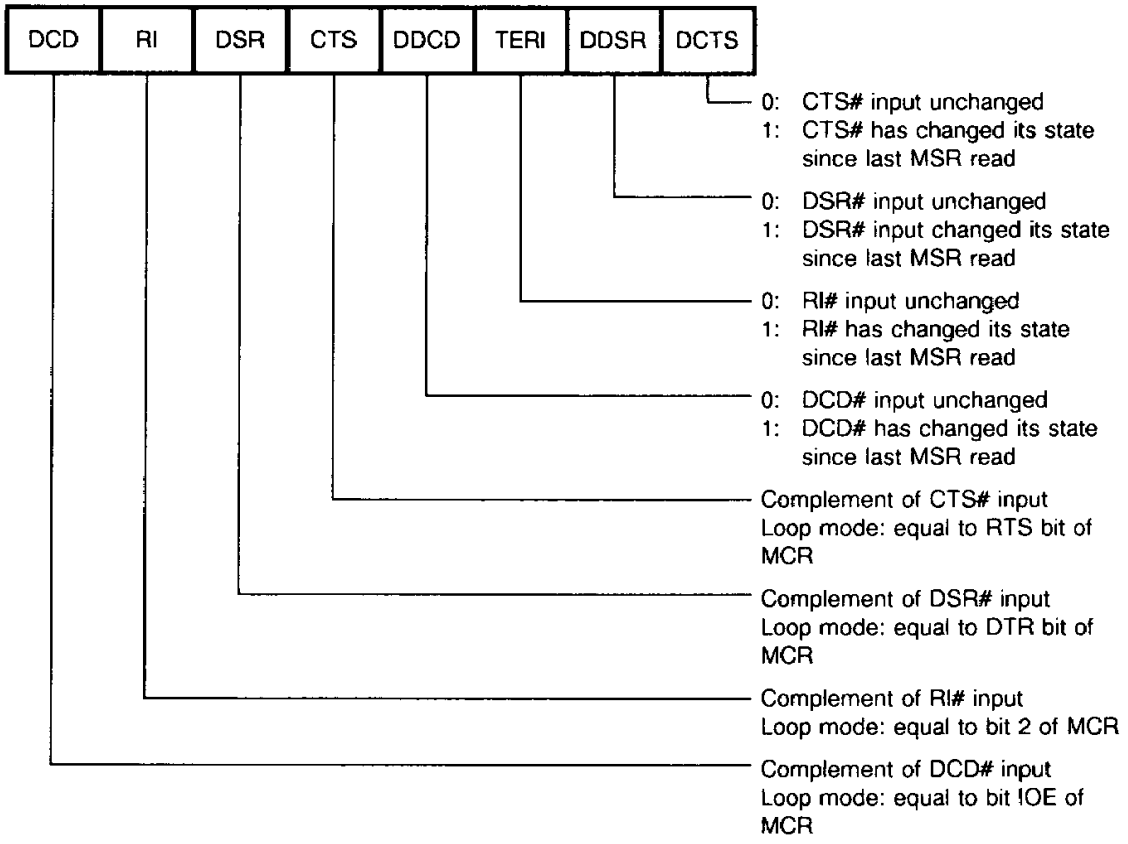
2) In loop mode this bit is equivalent to the MSR bit 7 (DCD).

3) When LOOP is set to logic 1, the following occurs: the transmitter serial output (TXD) is set the the marking (logic 1) state; the receiver serial input (RXD), is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four Modem control inputs (CTS#, DSR#, RI# and DCD#) are disconnected; and the four Modem control bits (0-3) are internally connected to the four Modem control inputs. The Modem control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received data paths of the UART. In the loop mode, the receiver and transmitter interrupts are fully operational. The Modem control interrupts are also operational, but the interrupt's sources are now the lower four bits of the Modem control register instead of the four Modem control inputs. The interrupts are still controlled by the interrupt enable register.

Modem Status Register (MSR)

This register provides the current state of the control lines from the Modem (or peripheral device) to the CPU. In addition to this current-state information, four bits of the Modem status register provide change information. These bits are set to a logic 1 whenever a control input from the Modem changes state. They are reset logic 0 whenever the CPU reads the Modem status register. Figure 8 shows the contents of the MSR.

Figure 8
Modem Status Register



Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a modem status interrupt is generated.

Scratchpad Register

This 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Reset Operation

A low level at the RESET# input pin causes the UART to reset to the condition listed in table 7.

Table 7
Register Reset Functions

Register/signal	Reset Control	Reset state
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high, bits 1 and 2 low, bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 and 6 are high
Modem Status Register	Master Reset	Bits 0-3 low, bits 4-7 input signal
SOUT	Master Reset	High
BDO	Master Reset	High
Interrupt (RCVR ERRS)	Master Reset/Read LSR	Low
Interrupt (RCVR Data Ready)	Master Reset/Read RBR	Low
Interrupt (THRE)	Master Reset/Read IIR/ Write THR	Low
Interrupt (Modem status changes)	Master Reset/Read MSR	Low
RTS#	Master Reset	High
DTR#	Master Reset	High
Interrupt output line	Master Reset	tristated

Parallel Port Description

Register Selection

The internal data, status and control registers of the parallel port are selected by two address lines, the chip select line CS3# and the read write control inputs.

Table 8
Parallel Port Register Addresses

CS3#	A1	A0	IOR#	IOW#	Operation
1	X	X	X	X	No Operation
0	0	0	1	0	Write Data Register
0	0	0	0	1	Read Data Register
0	0	1	0	1	Read Status Register
0	1	0	1	0	Write Control Register
0	1	0	0	1	Read Control Register

While CS3# is activated, CS1# and CS2# must be inactive. Other combinations of A0, A1, IOR#, and IOW# together with CS3# = 0 as shown in table 8 are illegal combinations.

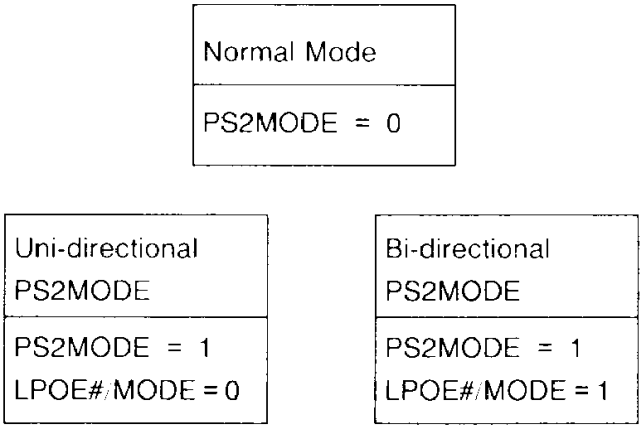
Table 9
Parallel Port Register Definition

	Register Address		
	0	1	2
Bit No.	Data Register	Status Register	Control Register
0	Data Bit 0	1	STB
1	Data Bit 1	1	AFD
2	Data Bit 2	PS2MODE = 0:1 PS2MODE = 1:IRQSTAT	INIT
3	Data Bit 3	ERROR	SLCTIN
4	Data Bit 4	SLCT	IRQEN
5	Data Bit 5	PE	PS2MODE = 0:1 PS2MODE = 1:DIR
6	Data Bit 6	ACK	1
7	Data Bit 7	BUSY	1

Parallel Port Mode Selection

The parallel port of the SAB 82C250/82C251 can work in two basic operating modes: the normal mode and the PS/2 mode. In PS/2 mode a uni-directional or bi-directional operation is possible. Two strapping pins are used to select the operating mode. With PS2MODE = 0 the normal mode is selected. In PS/2 mode, the LPOE#/MODE pin selects further, mode operations (figure 9).

Figure 9
Parallel Port Mode Selection



In the normal mode, the SAB 82C250/82C251 parallel port operates in a XT/AT and 16C452/16C451 compatible mode. The input line LPOE#/MODE acts as an output enable input for PD0-PD7. With LPOE#/MODE = 1, PD0-PD7 may be used as an 8-bit input port.

In the PS/2 mode, the parallel port is fully register compatible to the parallel port implementation of the PS/2 PC's.

Data Register

The data register is a read/write register for the 8-bit data of the parallel port. The data transfer to or from the PD0-PD7 pins is handled via this register. The source of data during a read operation of the data register depends on the selected mode of the parallel port. Either the data register itself or the data at the PD0-7 pins may be read back (figure 10).

Figure 10
Parallel Port Internal Data Path

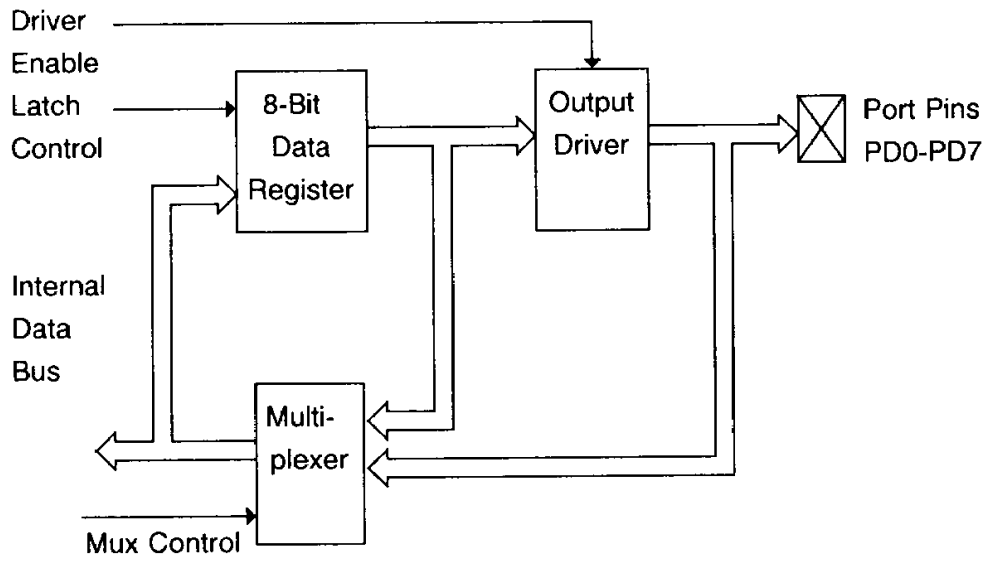


Table 10 shows all mode dependent functions of a read/write access of the parallel port data register.

The PS/2 mode is divided into an uni-directional and a bi-directional operation mode.
In the uni-directional PS/2 mode output drivers are always enabled. In this mode a read access to the data register directly returns the data register content.
In the bi-directional PS/2 mode, bit 5 of the control register (DIR) controls the direction of the data paths. If DIR is set, data at PD0-7 can be read (output driver disabled). With DIR = 0, the data register information is available at PD0-7 (output driver enabled).

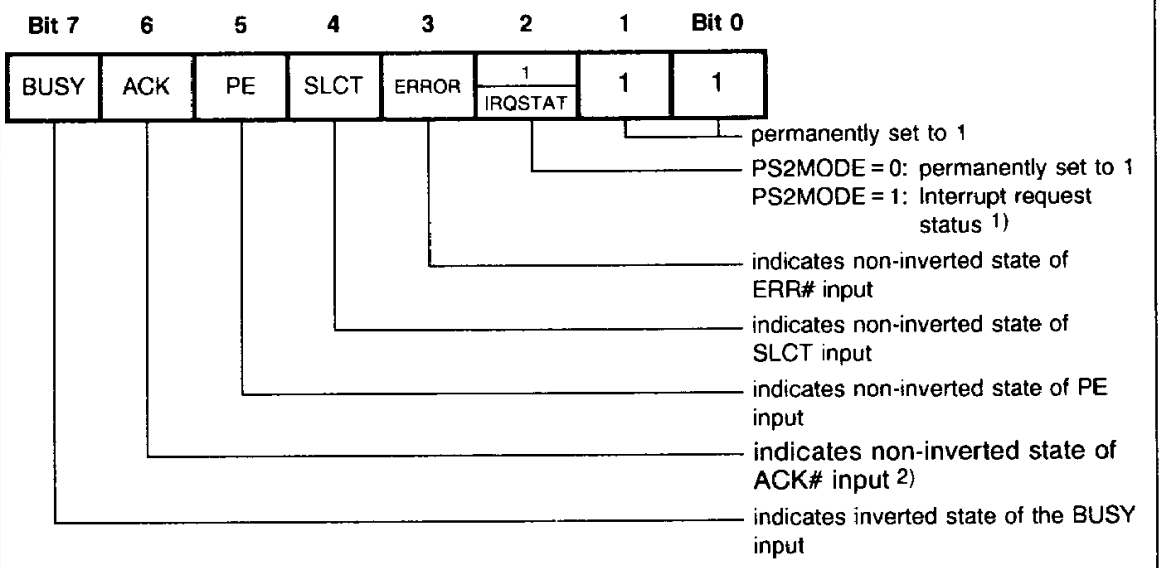
Table 10
Parallel Port Data Register Access Combinations

Mode		Pin PS2MODE	Pin LPOE#/ MODE	Bit DIR	Read Operation	Write Operation
Normal Mode		0	0	X	Read data register via the enabled output driver	Latch data in data register with output driver enabled
		0	1	X	Output driver disabled; Read data from PD0-7	Latch data in data register with output driver disabled
PS/2 Mode	Uni-directional	1	0	X	Read data of data register with output driver enabled	Latch data in data register with output driver enabled
	Bi-directional	1	1	0	Read data of data register with output driver enabled	Latch data in data register with output driver enabled
		1	1	1	Output driver disabled; Read data from PD0-7	Latch data in data register with output driver disabled

Status Register

The status register is a read-only register. A read operation of this register presents the real-time status of the parallel port interface input lines to the CPU.

Figure 11
Parallel Port Status Register



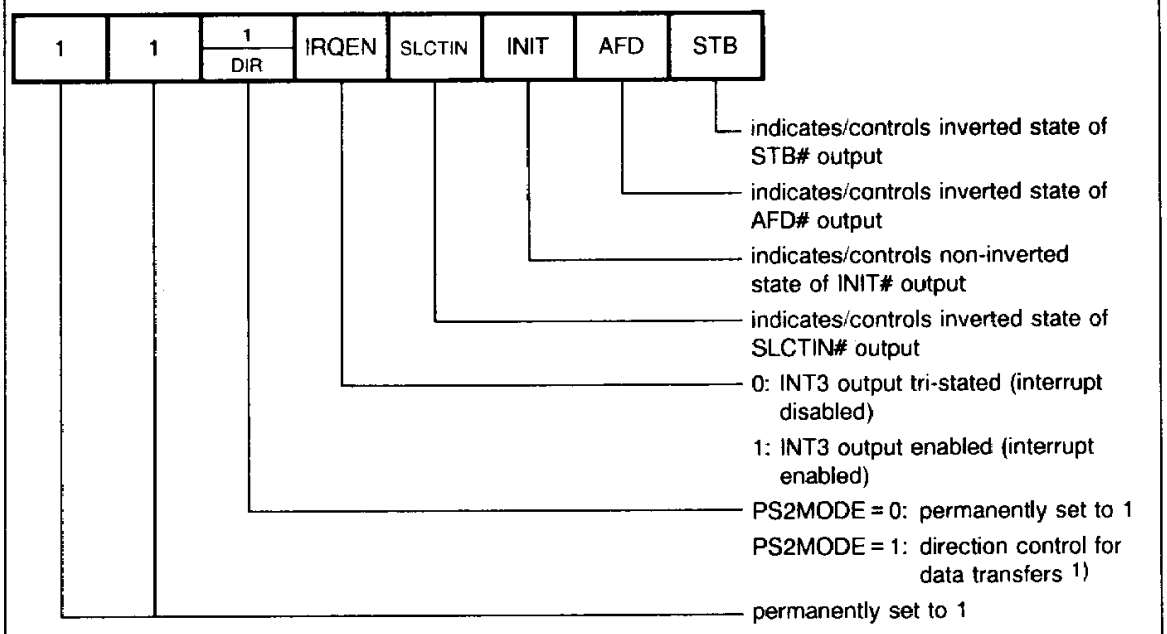
1) If PS2MODE = 1, this bit indicates an interrupt request status. IRQSTAT is cleared with every transition of the ACK# input signal, if the interrupt requests are enabled by the IRQEN bit of the control register (IRQEN = 1). If IRQSTAT = low, a read operation of the status register sets IRQSTAT back to high level. IRQSTAT is also set high by writing the control port with IRQEN = 0 (interrupt disable).

2) If parallel port interrupt is enabled (IRQEN = 1), the ACK# input is directly connected to the INT3 output.

Control Register

The control register of the parallel port may be read or written. A write operation to the control register latches the five (PS/2 mode : six) least significant bits of the write data.

Figure 12
Parallel Port Control Register



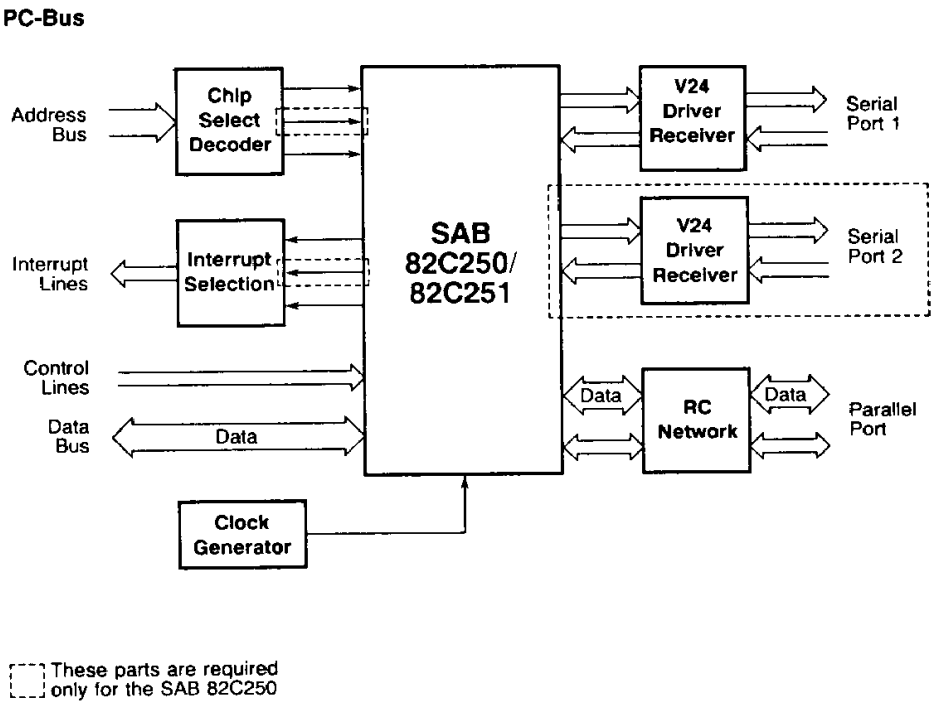
1) Details about DIR are described in table 10.

After a reset operation (RESET# = 0) the active bits of the control register are set in the following way:

STB, AFD, SLCTIN = 1

INIT, IRQEN, DIR = 0

Figure 13
SAB 82C250/82C251 Typical Application



Absolute Maximum Ratings

Ambient temperature under bias	0 to 70° C
Storage temperature	– 65 to + 150° C
Supply voltage	– 0.5 to + 70 V
Voltage on any pin with respect to ground	– 0.5 to V_{CC} + 0.5 V
Power dissipation	500 mW

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Clock input low voltage	V_{IL}	-0.5	+ 0.8	V	–
Clock input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Input low voltage	V_{IL}	-0.5	+ 0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 24 mA on PD0-PD7 I_{OL} = 10 mA on INIT#, AFD#, STB#, SLCTIN# I_{OL} = 4.0 mA on other inputs
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = -15 mA on PD0-PD7 I_{OH} = -1.5 mA on INIT#, AFD#, STB#, SLCTIN# I_{OH} = -2.5 mA on other inputs
Input leakage current	I_{IL}	–	± 10	µA	V_{CC} = 5.25 V; GND = 0 V; 0 V ≤ V_{IN} ≤ V_{CC} All other pins floating
Clock leakage current	I_{CL}	–	± 10	µA	V_{IN} = 0 V, 5.25 V

DC Characteristics (Continued)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Tristate leakage current	I_{OZ}	–	±20	µA	V_{CC} = 5.25 V; GND = 0 V; V_{OUT} = 0 V, 5.25 V 1. Chip selected 2. Chip and write mode selected
Power supply current	I_{CC}	–	20	mA	V_{CC} = 5.25 V; No loads on RXD0,1 , DSR0,1#, DCD0,1#, CTS0,1#; RI0,1# = 2.0 V; Other inputs = 0.8 V; Baud rate = 256 K; Baud rate gen. = 8 MHz

Capacitance

T_A = 25 °C; f = 1 MHz; V_{CC} = GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Clock input capacitance	C_{XIN}	–	10	pF	f_C = 1 MHz
Input capacitance	C_{IN}	–	10	pF	Unmeasured pins are returned to GND
Output capacitance	C_{OUT}	–	10	pF	Unmeasured pins are returned to GND

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ±5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Bus Interface Timing					
IOR# delay from address	t_{AR}	30	–	ns	–
IOW# delay from address	t_{AW}	30	–	ns	–
IOR# delay from chip select	t_{CSR}	30	–	ns	–
IOW# delay from chip select	t_{CSW}	30	–	ns	–
Data hold time	t_{DH}	30	–	ns	–
Data setup time	t_{DS}	30	–	ns	–
BDO delay from IOR#	t_{DD}	60	–	ns	1 TTL load
IOR# to floating data delay	t_{HZ}	0	100	ns	150 pF loading [1]
Parallel port data hold time	t_{PDS}	20	–	ns	–
Parallel port data setup time	t_{PDH}	20	–	ns	–
Address hold time from IOR#	t_{RA}	20	–	ns	–
Chip select hold time from IOR#	t_{RCS}	20	–	ns	–
IOR# strobe time	t_{RD}	125	–	ns	–
Delay from IOR# to data	t_{RWD}	–	125	ns	150 pF loading [1]
Address hold time from IOW#	t_{WA}	20	–	ns	–
Chip select hold time from IOW#	t_{WCS}	20	–	ns	–
Parallel port data valid after IOW#	t_{WOL}	–	90	ns	–
IOW# strobe width	t_{WR}	100	–	ns	–
Clock cycle time	t_{XC}	125	–	ns	–
Clock low time	t_{XH}	55	–	ns	–
Clock low time	t_{XL}	55	–	ns	–
Read cycle	R_C	280	–	ns	–
Write cycle	W_C	280	–	ns	–

[1] Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

AC Characteristics (Continued)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Receiver/Transmitter Timing					
Delay from IOR# to reset interrupt (read RBR or read LSR)	t_{RINT}	–	175	ns	150 pF loading
Delay from stop to set interrupt	t_{SINT}	–	1	t_{XC}	150 pF loading
Delay from IOW# to reset interrupt (write THR)	t_{HR}	–	175	ns	150 pF loading
Delay from IOR# to reset interrupt (write THR)	t_{IR}	–	175	ns	150 pF loading
Delay from Initial interrupt reset to transmit start	t_{IRS}	24	40	1)	–
Delay from initial write to interrupt	t_{SI}	32	48	1)	–
Delay from stop to interrupt (THRE)	t_{SINT}	8	8	1)	–
Modem Control Timing					
Delay from IOW# to output (write MCR)	t_{MDO}	–	200	ns	150 pF loading
Delay from IOW# to interrupt active/ tri-state	t_{WI}	–	200	ns	150 pF loading
Delay to reset interrupt from MODEM input	t_{SIM}	–	200	ns	150 pF loading
Delay to reset interrupt from IOR# (read MSR)	t_{RIM}	–	200	ns	150 pF loading
Reset Timing					
Output float from reset	t_{RSF}	–	100	ns	150 pF loading 2)
Output low from reset	tRSL	–	100	ns	–
Output high from reset	tRSH	–	100	ns	–
Reset pulse width	tRW	500	–	ns	–

1) The unit is the clock frequency (baud rate) which is defined by dividing the CLK input frequency by the specified divisor in the baud generator divisor latches.

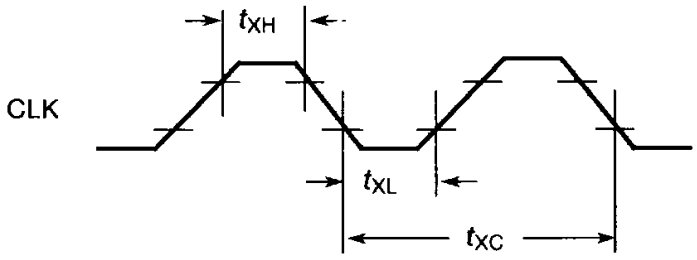
2) Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

AC Characteristics (Continued)

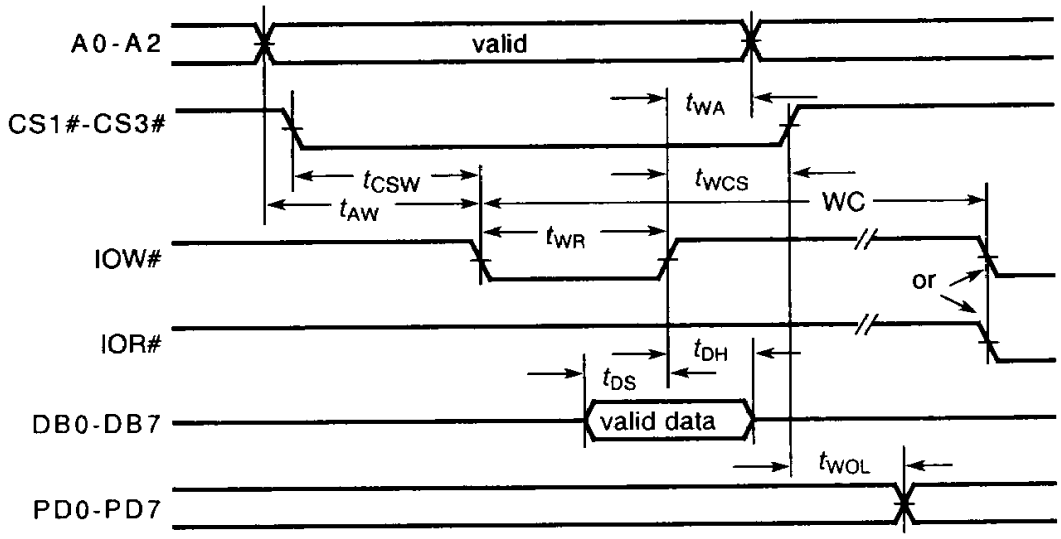
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Parallel Port Timing					
Data to STB# setup/hold time	t_{DT}	1	–	µs	–
STB# width	t_{SB}	1	500	µs	–
BUSY# start to ACK#	t_{BSA}	–	–	µs	Printer dependent
BUSY# delay from STB#	t_{BSD}	–	–	µs	Printer dependent
BUSY# width	t_{BSY}	–	–	µs	Printer dependent
ACK# width	t_{AK}	–	–	µs	Printer dependent
ACK# delay	t_{AKD}	–	–	µs	Printer dependent
INT3 delay to ACK# transition	t_{ID}	–	50	ns	–
INT3 disable time	t_{IDI}	–	50	ns	150 pF loading 1)
INT3 enable time	t_{IEN}	–	50	ns	150 pF loading 1)

1) Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

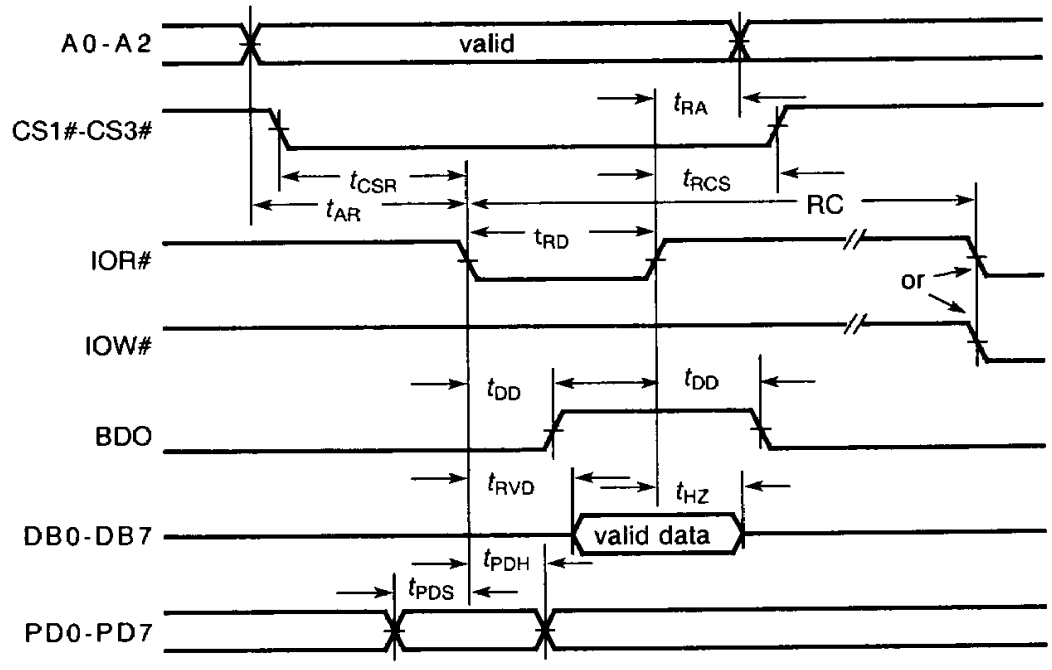
CLK Input



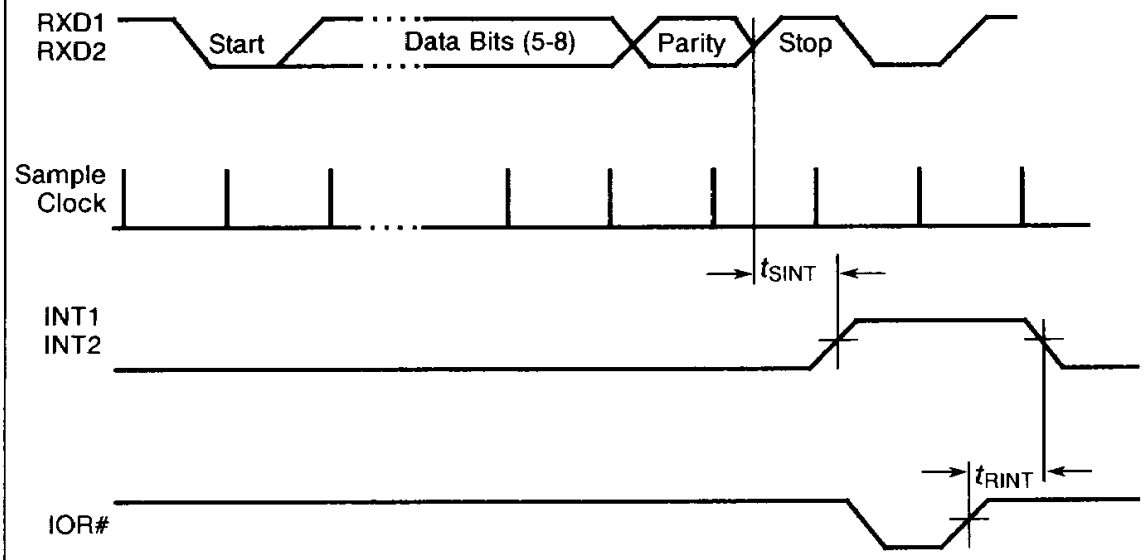
Write Cycle Timing



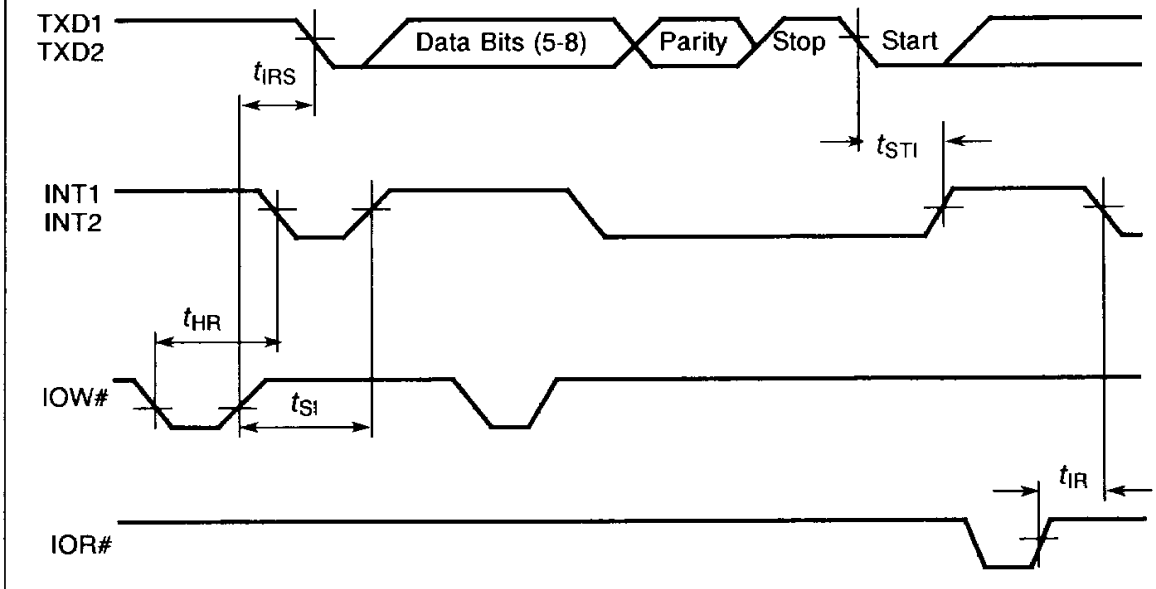
Read Cycle Timing



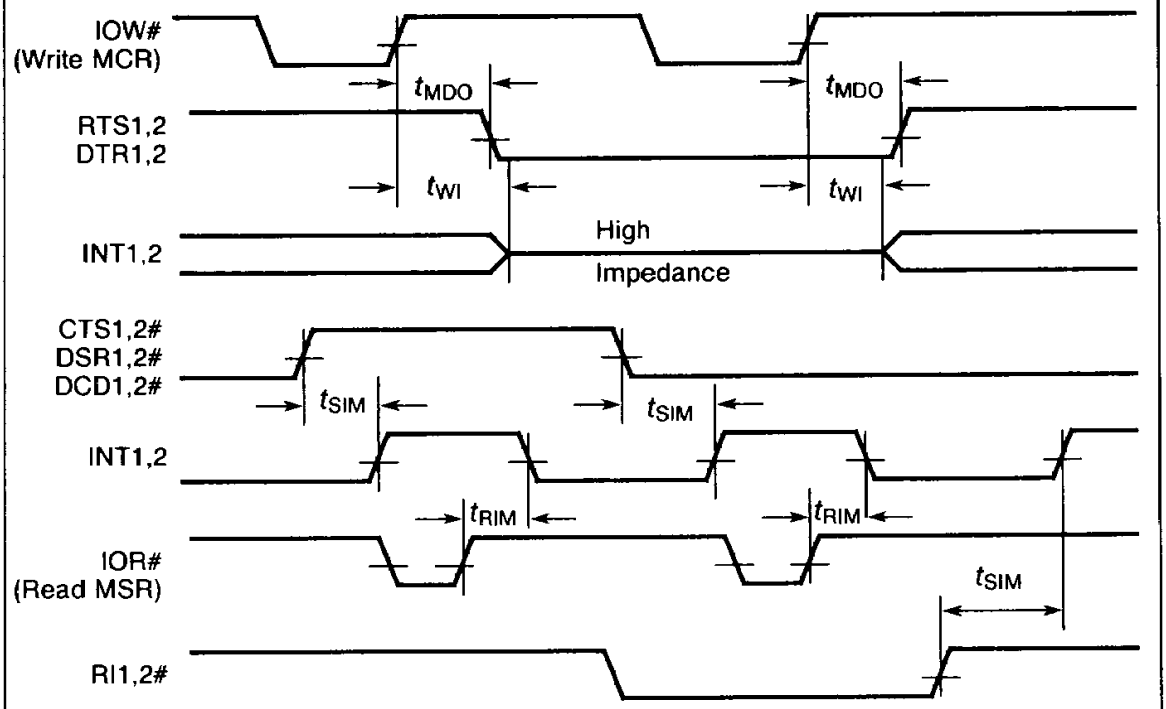
Receiver Timing



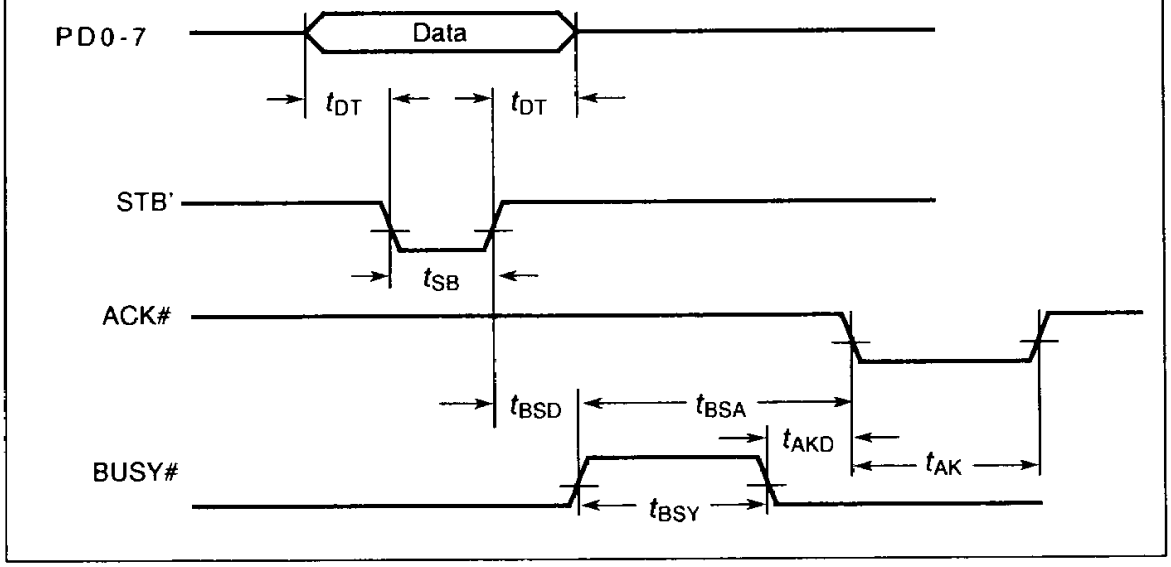
Transmitter Timing



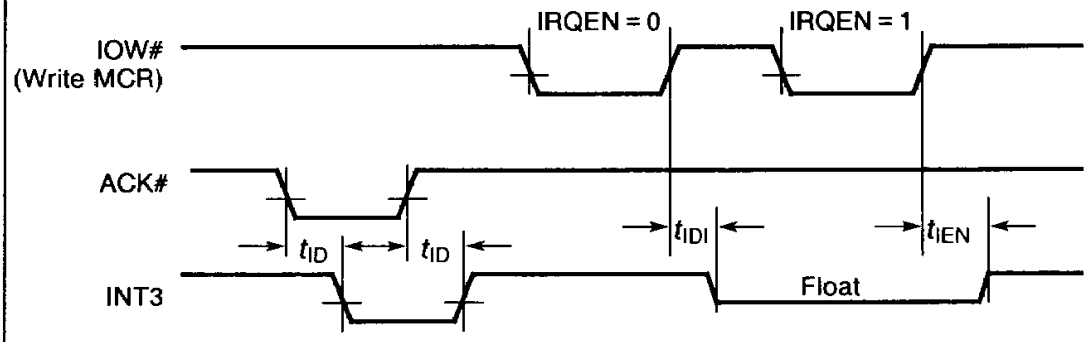
Modem Timing



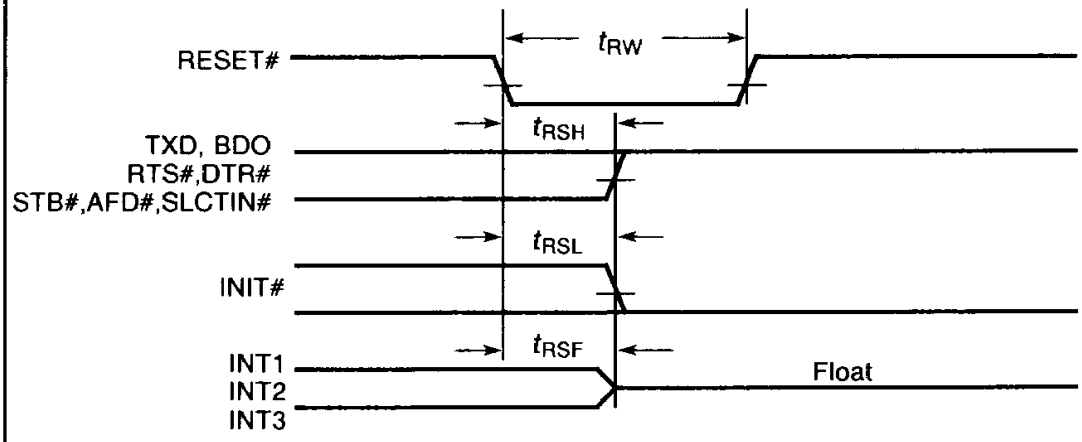
Typical Centronics Parallel Port Timing



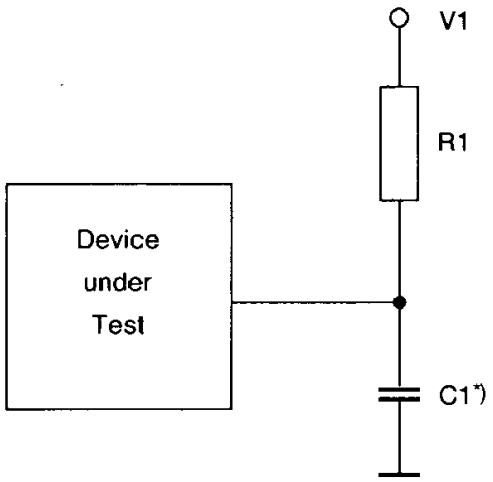
Parallel Port Interrupt Timing



Reset Timing



AC Test Circuits



Related Device Pins	V1	R1	C1
PD0 - PD7	1.63 V	51 Ω	150 pF
INIT#, AFD#, STB#, SLCTIN#	2.54 V	174 Ω	150 pF
All other Pins Pins	1.63 V	308 Ω	150 pF

*) Includes stray and jig capacitance

Ordering Information

Type	Ordering code	Package	Function
SAB 82C250-N	Q67120-P302	PL-CC-68 (SMD)	Advanced peripheral interface controller (2 serial port, 1 parallel port)
SAB 82C251-N	Q67120-P304	PL-CC-68 (SMD)	Advanced peripheral interface controller (1 serial port, 1 parallel port)